Summary

For the Phase II upgrade at the High Luminosity LHC (HL-LHC) at CERN, the ATLAS experiment is set to construct a fully silicon-based tracker. The Inner Tracker (ITk) will feature a silicon strip detector with a novel readout system engineered to manage the increased occupancy and more extreme radiation conditions anticipated. The readout architecture incorporates the ABCStar, an analog front-end chip, and the HCCStar, a control interface chip that bridges the ABCStars on the hybrid with the electronics situated off-detector.

The ABCStar ASIC, utilizing 130 nm CMOS technology, is designed to process signals from 256 sensor strips via binary readout channels. In tandem, the HCCStar ASIC serves as the digital conduit for the ITk Strips hybrids, utilized across both the endcap and barrel regions. A single HCCStar can interface with up to 11 ABCStars, collectively facilitating the detector's readout and control operations. Exposure to high-energy particle injection can lead to single event effects (SEEs) in these electronic devices, inducing bit flips and other disruptions.

The L0A/CMD/BCR (LCB) signal transfers triggers (L0A), fast-commands, register read/write (CMD) and bunch-counter-reset (BCR) to the HCCStar (and ABCStar) ASICs, and Low Priority readout request (LP) is an asynchronous request from the HCCStar to the ABCStar to read out an event from the ABCStar event buffer with low priority. LCB and LP paths are separate lines from the data path, LCB sends messages to the HCC, and LP sends the trigger decision from the HCC to the ABCs, for more information, refer to Fig. 1.

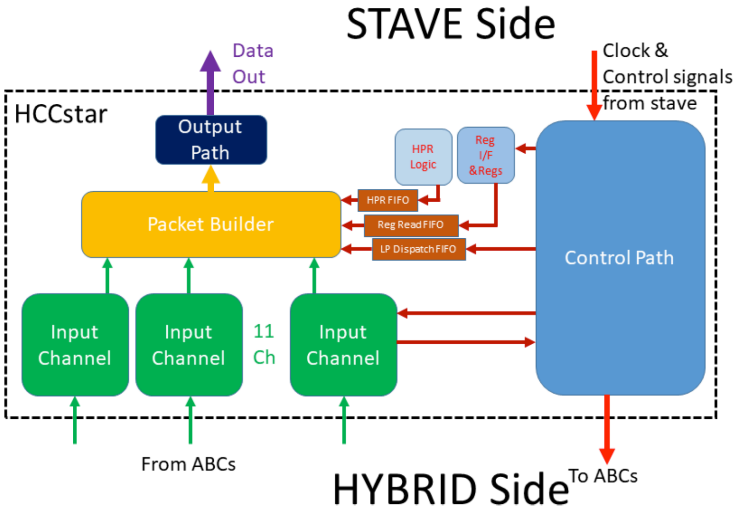

Figure 1: HCCStar Top Level Block Diagram

This paper will present results from proton irradiations of the HCCStar at the China Spallation Neutron Source (CSNS) during November 2023.

The irradiation tests have been performed before at TRIUMF in May 2022, for correctable bit flips per bit per year, the value we calculated in CSNS is consistent with the result of TRIUMF, they are both O(10), and register resets also happen in CSNS, which is consistent.

In addition, we observed the occurrence of actual SEUs in CSNS, which is not observed previously before with proton beam, and we also study the dependency of bit flips on energy by applying several different beam energy, which haven't been done before.

The significance of this work lies in the systematic study of SEE under various energy levels, which aids in a deeper understanding the performance of SEE in HCC. Additionally, this work evaluates the bit flip situation of HCC on the HL-LHC based on data from CSNS.

The challenge of this work is to minimize the impact of secondary particles on the equipment, which can lead to device failure or erroneous bit flips, because our focus is on the SEEs caused by proton beam. To address this, we placed the relevant FPGA boards and low voltage power supplies under the protection of lead bricks and within a bunker, respectively.

Certainly, there are some uncertainties encountered during this experiment, such as the issue of LP/LCB signals not being in sync. Currently, we suspect that this may be related to a poor connection in the long two twisted cable (~1.5m), but the answer to this problem depends on our future experiments.