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Advancements in 28nm CMOS Radiation Hardened IP for Particle Physics Experiments

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Quality analogue radiation-hardened design in 28nm CMOS is an iterative process best achieved through IP development. Rutherford Appleton Laboratory (RAL) ASIC Design Group has implemented two test-structure ASICs, PURNIX and YELNIX, to validate the performance of circuits up to 1GRAD TID. PURNIX includes essential building-block radiation-hardened IP, while YELNIX includes a prototype LGAD preamplifier and TDC sub-circuit options. Irradiated performance will be evaluated in collaboration with the universities of Birmingham and Oxford. In parallel, we continue our developments with an improved low-voltage amplifier architecture, low-profile 8bit-ADC, <20ps TDC and 25Gbps readout circuits. We present test results and current circuit developments.

Summary (500 words)

Rutherford Appleton Laboratory (RAL) continues to enhance its semiconductor ASIC capabilities with the development of 28nm CMOS Radiation Hardened IP for Particle Physics Experiments. Our intent is to establish reusable silicon-proven IP and expert knowledge in radiation hardened circuit design for future ASICs. This activity is intended to be complimentary to the CERN led 28nm community effort to develop a common IP library for use in developing future ASICs.

Two 28nm CMOS ASIC test structures have been fabricated named PURNIX and YELNIX. These contain a range of IP designed to operate up to 1GRAD TID, following the current recommended design techniques for radiation hardness in 28nm CMOS. Post-irradiation results will validate their effective rad-hard performance and iteratively improve existing and future IP.

The PURNIX ASIC contains essential building block radiation-hardened IPs for future ASICs. These IPs include a precision rail-to-rail amplifier, high speed amplifiers, beta-multiplier current reference, voltage reference bandgap, a 12-bit compact slope ADC, a 10-bit resistive voltage DAC and a 10-bit current mirroring DAC. The ASIC also contains high-speed digital test circuits with triple-modular-redundancy (TMR) for evaluating post-irradiation operating frequency performance and SEU robustness.

The YELNIX ASIC contains a prototype LGAD front-end readout architecture with two trial TDC solutions. The specification for this is targeted at an LGAD 15x15 pixel array with 1.3mm pixel pitch. With further development, the front-end is expected to deliver sub-20ps rms Time-of-Arrival (TOA), and a Time-Over-Threshold (TOT) with a minimum input charge of 3fC.

The RAL team is Collaborating with colleagues from the UK universities of Birmingham and Oxford to carry out radiation testing of the ASICs at the M40 Cyclotron (Birmingham) and the X-ray laboratory (Oxford) to evaluate radiation damage effects and differences due to dose rate. Single-Event-Upset (SEU) testing will also be conducted to validate TMR robustness.

We will also present our current IP under development, which includes a high-precision differential amplifier, an ultra-low-area low-power standalone 8-bit ADC for continuous internal calibration requirements, a sub-20ps TDC for the LGAD front-end, 25Gbps serializer for future ethernet development and an improved rail-to-rail amplifier with a new low-voltage architecture. The improved rail-to-rail amplifier employs a new low-voltage friendly architecture to replace the classic stacked diode technique for class AB folded cascodes, allowing reliable output current biasing and improved linearity and stability across process-voltage-temperature (PVT) corners. We have a planned tape-out date of January 2025 for this IP under development.

We will also present our work to date and the results from testing the PURNIX and YELNIX test structures along with any preliminary irradiation results.

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