Prototype of an asynchronous versatile readout

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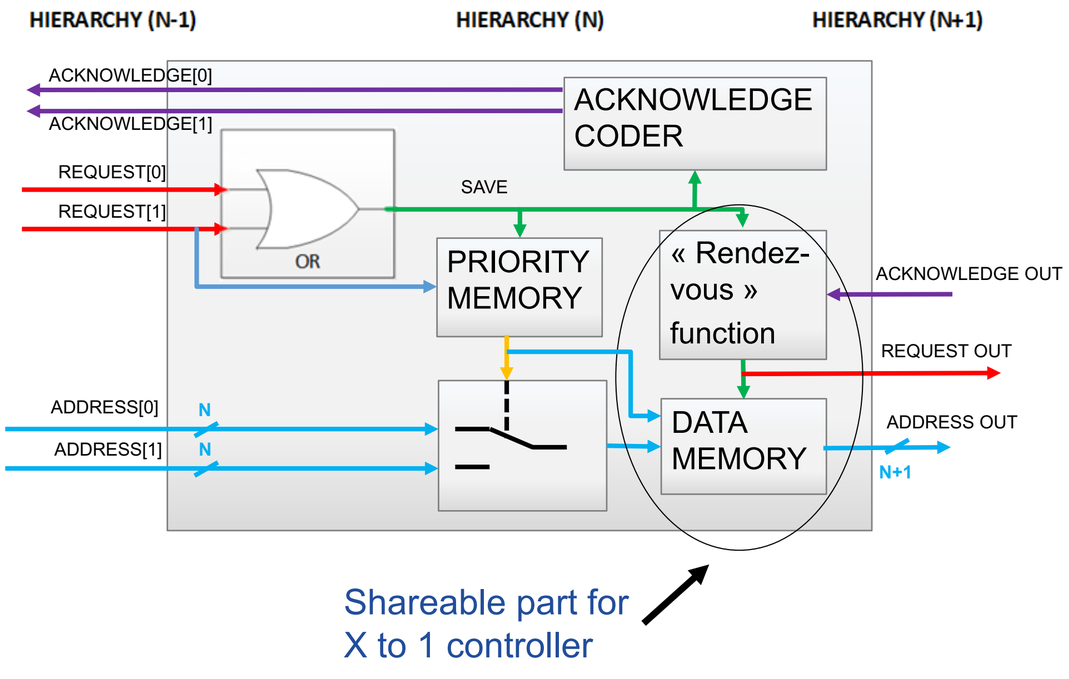
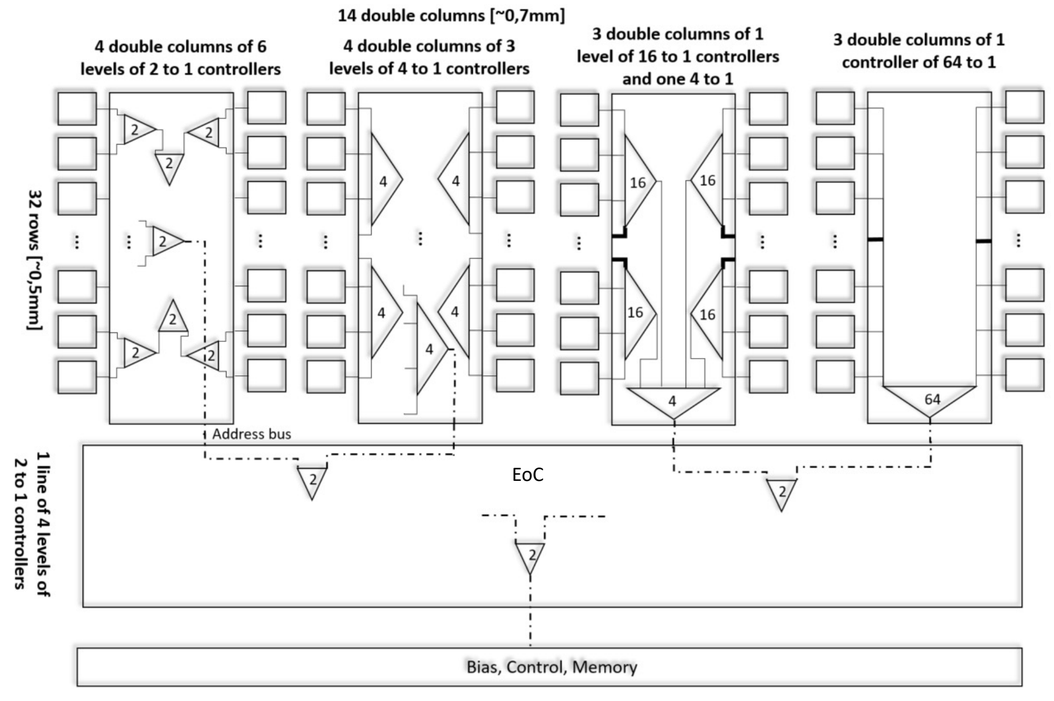
Goals:
Implementation of an **asynchronous readout** architecture for particle sensors
First demonstrator to validate power consumption and readout speed
Nanosecond resolution end-of-column timestamping with **Time of Arrival** and **Time over Threshold** capability

Asynchronous readout

Working principle (2 to 1)



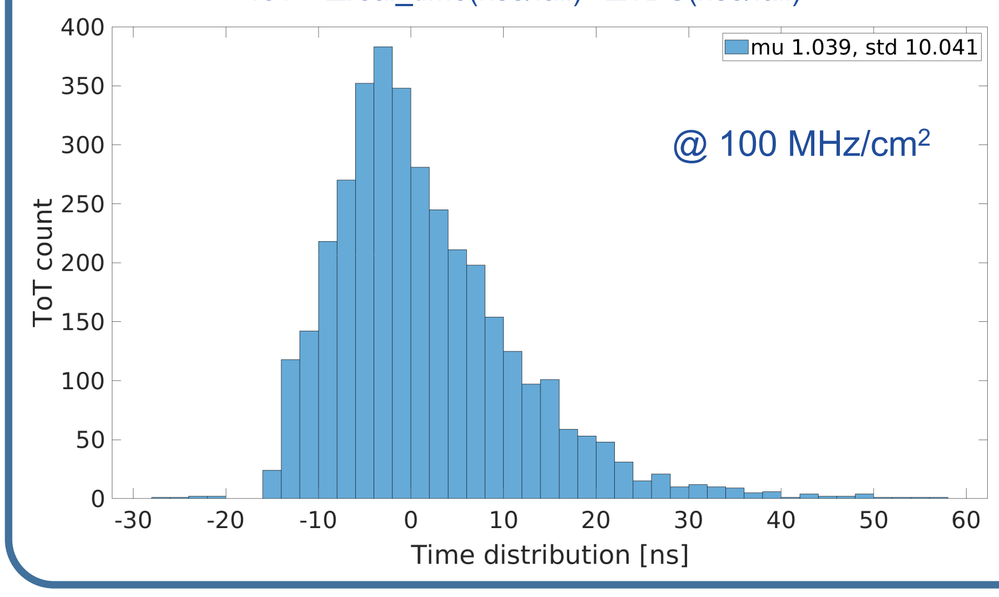
Architecture of the matrix (32x28 pixels)



Fixed Priority time Arbiter (FPA) implementation

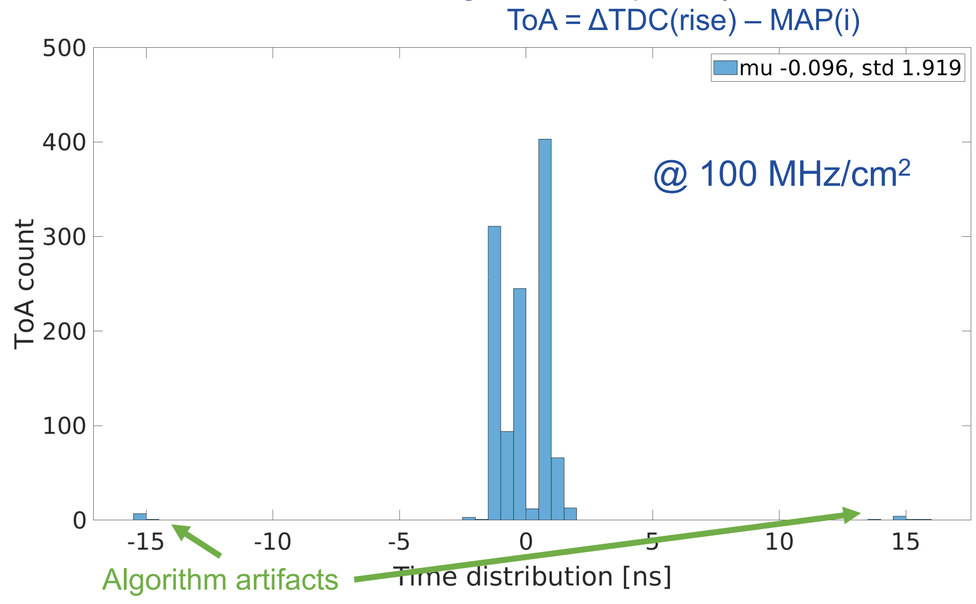
Corrected Time over Threshold error

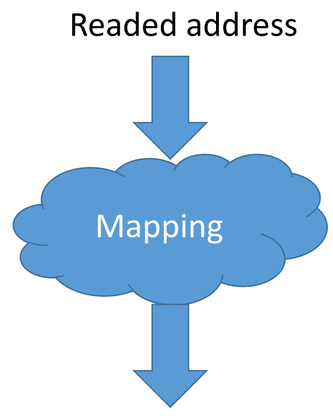
Digital readout post-layout simulations
ToT = Δreal_time(rise/fall) - ΔTDC(rise/fall)



Corrected Time of Arrival error

Digital readout post-layout simulations
ToA = ΔTDC(rise) – MAP(i)

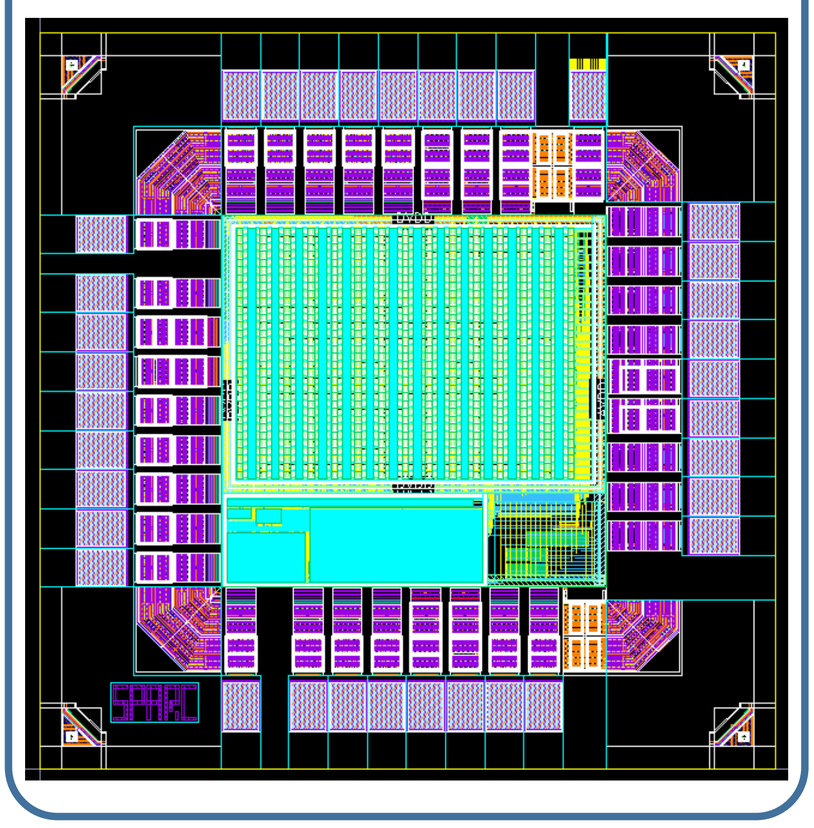




Area & power results (at 40MHz/cm²)

Controller size	Inputs	Digital Cells For 16 µm width [%]	Track usage Main direction [%]	Power density [mW/cm²]
2 to 1	64	70	17	5.2
4 to 1	64	47	16	2.8
16 to 1 + 4 to 1	64	43	16	2.6
64 to 1	64	40	16	2.3
EoC 2 to 1	16	43	23	1.8

Layout of a 1.5x1.5 mm chip build in a TPSCo 65nm



Summary

- ❑ Prototype of a full asynchronous readout
- ❑ Digital standard flow
- ❑ Pixel pitch of 24.1x16 µm
- ❑ Power consumption less than 5 mW/cm²
- ❑ Mean reading speed of 6.3 ns
- ❑ Time measurement outside the matrix:
  - ❑ ToA: few nanosecond
  - ❑ ToT: few tens of nanosecond

TWEEP 2024, University of Glasgow