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Small prototype of an asynchronous versatile readout

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Monolithic active pixel sensors are considered as the nominal choice for a large variety of particle physics experiments. Consequently, the design of pixel matrices faces a wide range of specifications.

We developed a pixel matrix read-out architecture based on the local interconnection of asynchronous N:1 time arbiters with fixed priority. This architecture is not limited by global signals and can achieve high bandwidth with a fully column-parallel stream. Layouts of a small prototype of 32x32 pixels were completed in a 65 nm CMOS imaging process, for various combinations of controllers with ratios from 64:1-2:1 with a pixel size of 25x16µm2.

Summary (500 words)

Nowadays, Monolithic Active Pixel Sensors (MAPS) are considered as the nominal choice for a large variety of particle physics experiments. Consequently, the design of pixel matrices faces a wide range of specifications. That impacts in particular the matrix read-out strategy, which is highly constrained in terms of power consumption, layout area, time-stramping ability, and hit rate. Asynchronous logic seems promising in this respect, being naturally data-driven and power-sparing.

We developed a pixel matrix read-out architecture based on the local interconnection of asynchronous N:1 time arbiters with fixed priority. This architecture is not limited by global signals and can achieve high bandwidth with a fully column-parallel stream. Layouts of a small prototype of 32x32 pixels matrix were completed in a 65 nm CMOS imaging process, for various combinations of controllers 64 to 1, 16 to 1 (completed by a 4 to 1), 4 to 1 and 2 to 1 with a pixel size of 25x16 µm2. The line readout is a 2 to 1 with 16 double column inputs chosen for its high bandwidth.

This contribution will present the matrix read-out performances obtained on simulation for a real circuit. Simulations results will be presented at the maximal rates to show the suitable controller size as function of the experiment requirements. Power simulations will be done to validate the linearity regarding the hit rate and see a possible reduction against synchronous readouts. Finally, single event upset could be simulated to evaluate the radiation hardness of the Müller gate and of the global architecture. The requirement targeted will be a rate of 100MHz/cm²/s, a power consumption close to 10 mW/cm² (as for ALICE ITS2 inner tracker) and a mean time to read an address of 12 ns with +/- 1 ns.

A last contribution will be a timestamping at the end of the matrix because the asynchronous architecture did not come with an integration. The possibility to timestamp every hit at the end of the matrix with an expected time resolution of 2 ns for the reconstruction will be studied. Multiple modes are developed to timestamp only the first hit (hit OR function), all address or both. The data travelling time can be reconstructed offline predict the arrival time to estimate precisely the fired time of each pixels. The readout is expected to be very fast and treat only one cluster per hit OR, so no overlap.

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