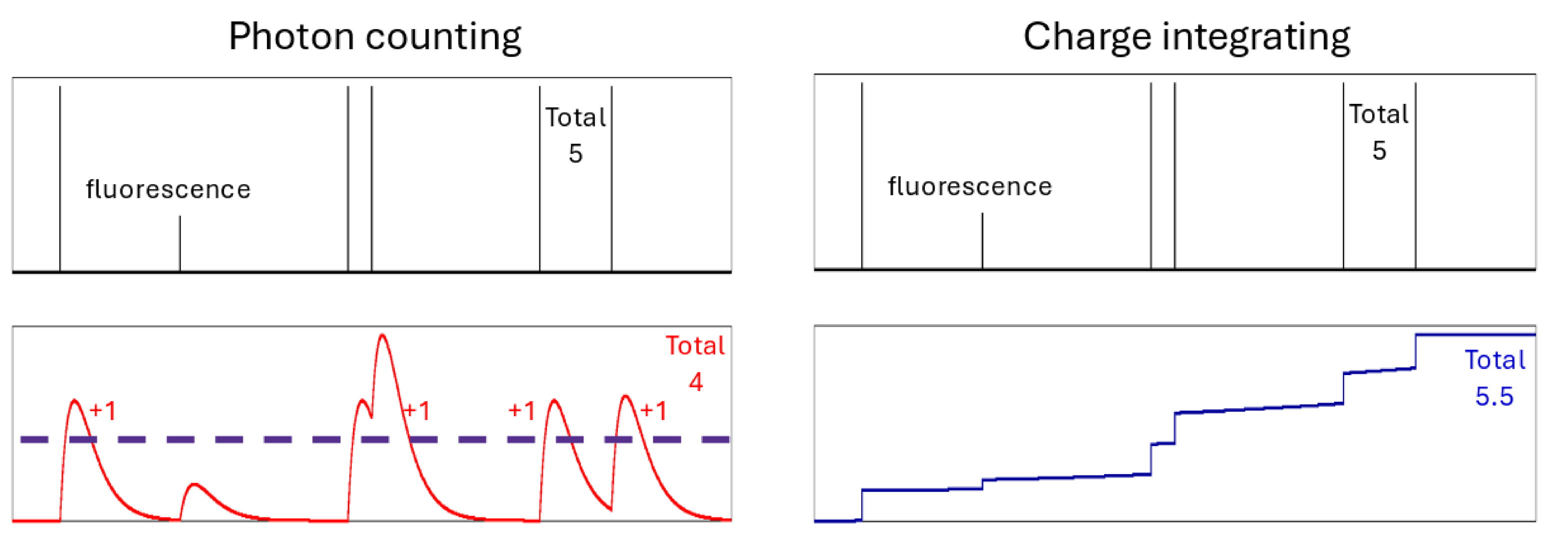
PSI Center for Photon Science

Digitizing the Output of Charge-Integrating X-Ray Detectors – ADC Design towards JUNGFRAU2.0

Patrick Sieberer[1], F. Baruffaldi, A. Bergamaschi[1], M. Brückner[1], M. Carulla[1], R. Dinapoli[1], S. Ebner[1], K. Ferjaoui[1], E. Fröjdh[1], D. Greiffenberg[1], S. Hasanaj[1], J. Heymes[1], V. Hinger[1], T. King[1], P. Kozlowski[1], C. Lopez-Cuenca[1], D. Mezza[1], K. Moustakas[1], A. Mozzanica[1], J. Navrátil, K.A. Paton[1], C. Ruder[1], B. Schmitt[1], D. Thattil[1], X. Xie[1], J. Zhang[1]

[1]Paul Scherrer Institut (PSI) Email: patrick.sieberer@psi.ch

How do we measure photons?

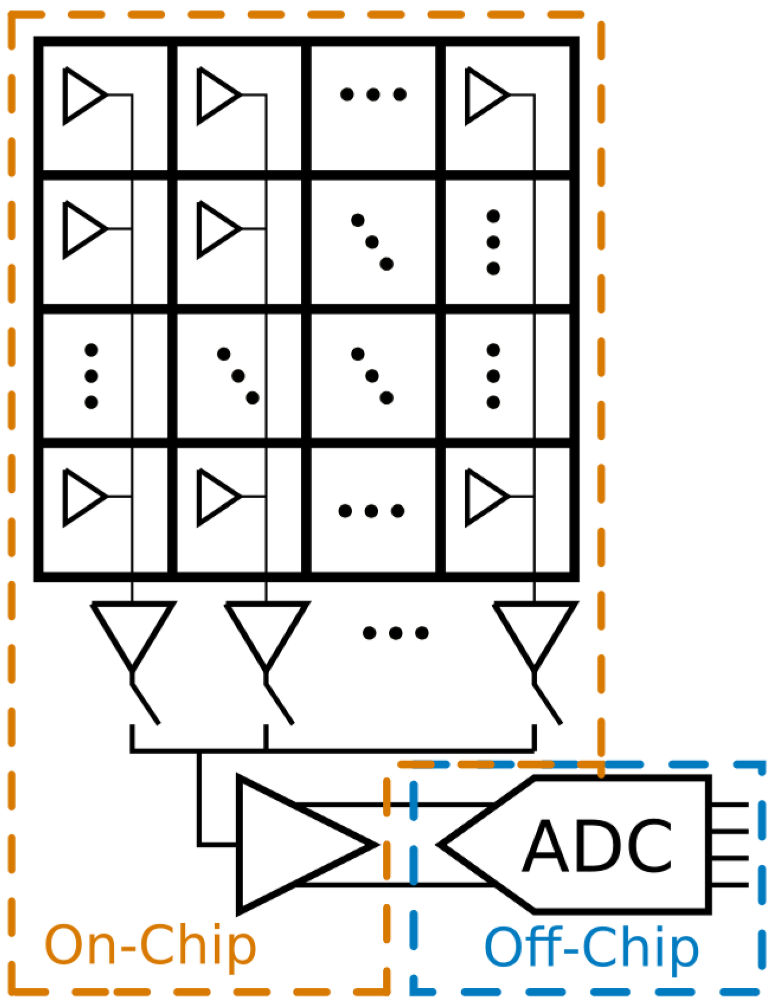


Noiseless + large dynamic range	Compromise between noise & dynamic range
Well established calibration	**Calibration difficult**
Fluorescence suppression	No fluorescence suppression
May pile-up (=loss of photon) at high hit rates (~1MHz/pixel), not suitable for pulsed sources (FELs)	**No pile-up, but might saturate**
No soft X-ray detection (peaks in noise level)	Detection of multiple soft X-rays possible
Number of photons as direct output	Number of photons by dividing total charge by the charge of a single photon

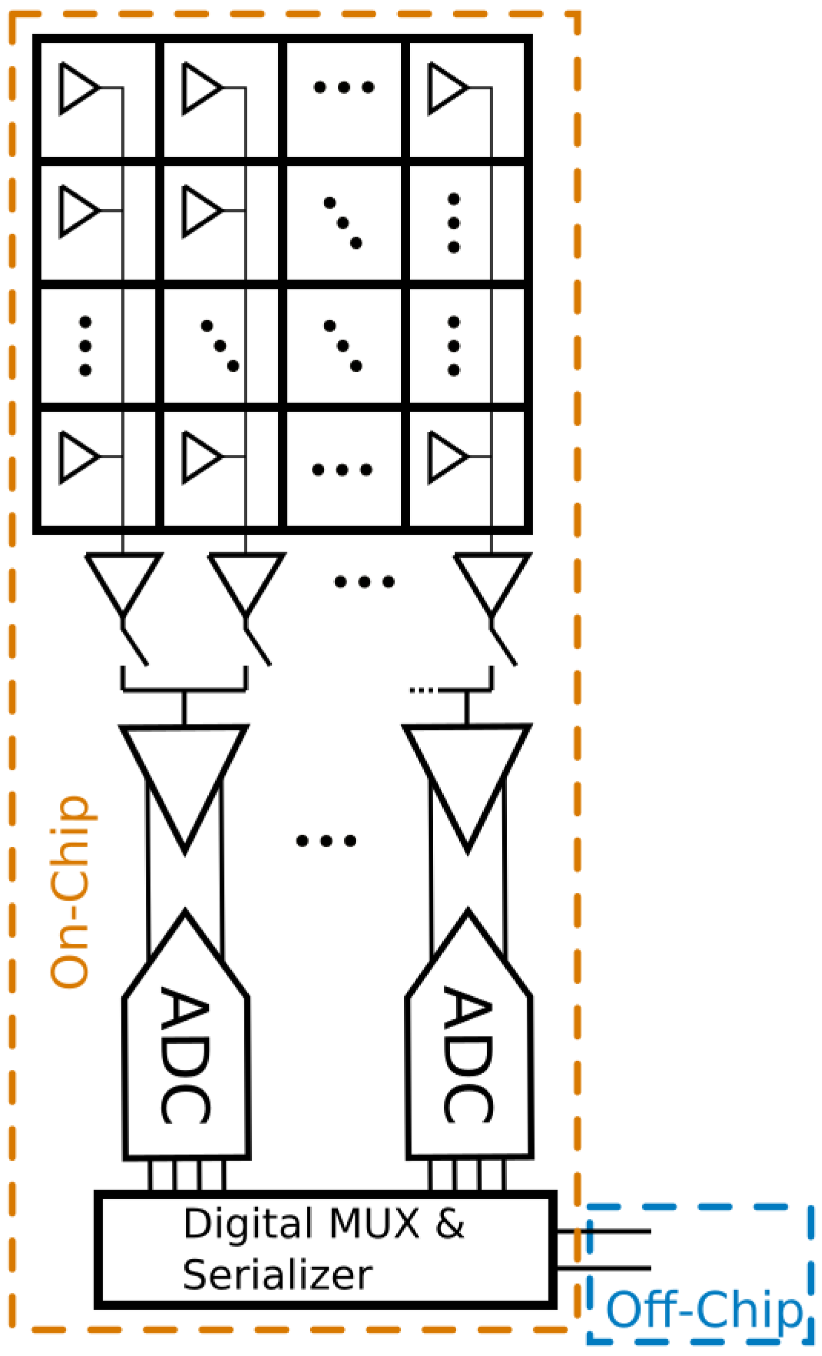
Rate limitation of photon counting detectors due to pile-up already a problem at 3rd generation synchrotrons and XFELs [1].

- Rate limitation will worsen at 4th generation synchrotrons
- Charge-integrating detectors overcome rate limitations

The future charge-integrating JUNGFRAU2.0 detector for high-rate synchrotron experiments



Data flow and digitization of JUNGRAU1.2



Data flow and digitization of JUNGRAU2.0

High speed analog buffers (>100MHz) are difficult to design

- → **More ADCs** (not faster ones!) are required

Numbers of outpus pads are limited

- → **On-Chip ADCs** together with a high speed (>3GHz) links as a solution

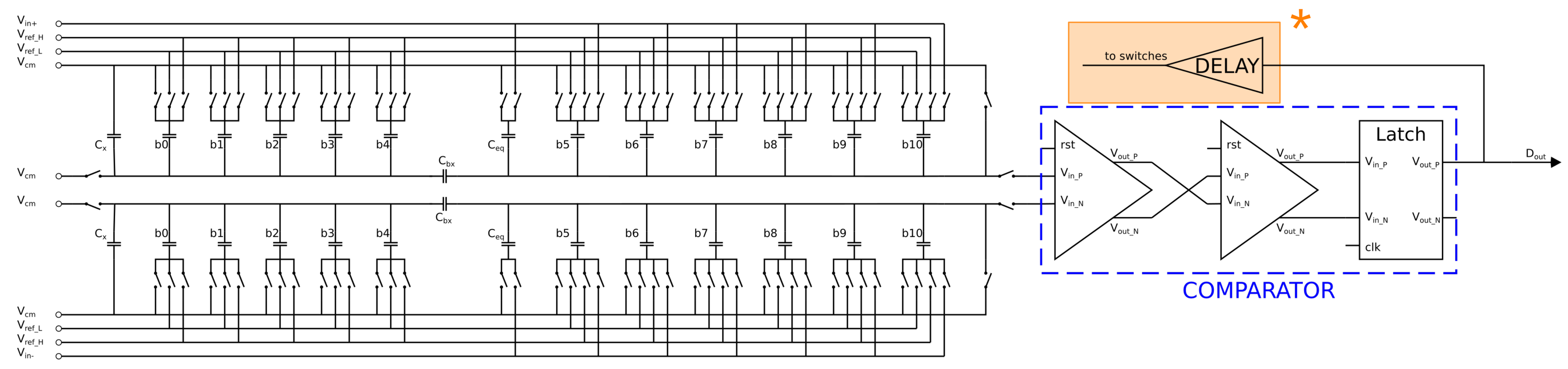
Details of the current JUNGFRAU1.2 chip in [2].

References

[1] A. Bergamaschi, A. Mozzanica and B. Schmitt. XFEL detectors. [online]. Available: https://www.nature.com/articles/s42254-020-0200-x
[2] Characterization results of the JUNGFRAU full scale readout ASIC. A. Mozzanica et al 2016 JINST 11 C02047
[3] Design and first tests of the Gotthard-II readout ASIC for the European X-ray Free-Electron Laser. J. Zhang et al 2021 JINST 16 P04015

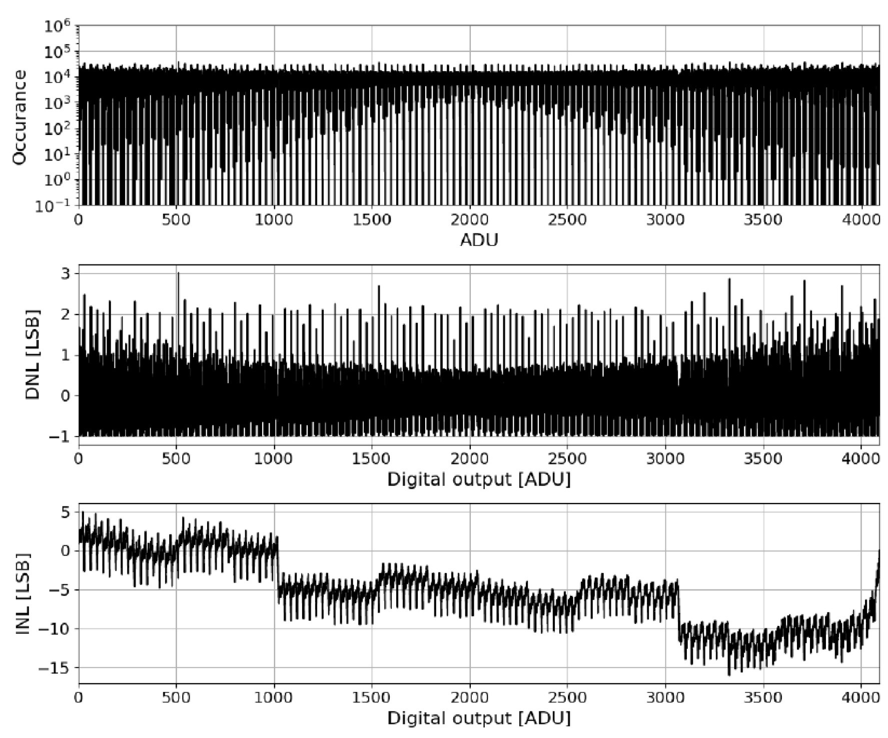
ADC-SAR-05: • UMC 110nm • Submitted Jun 2024 • Expected Oct 2024

SAR architecture: trade-off between power and speed



- 12-bit binary-weighted **s**uccessive **a**pproximation **r**egister (SAR) ADC
- Fully asynchronous control with configurable delay time between bits
- Differential, rail-to-rail design

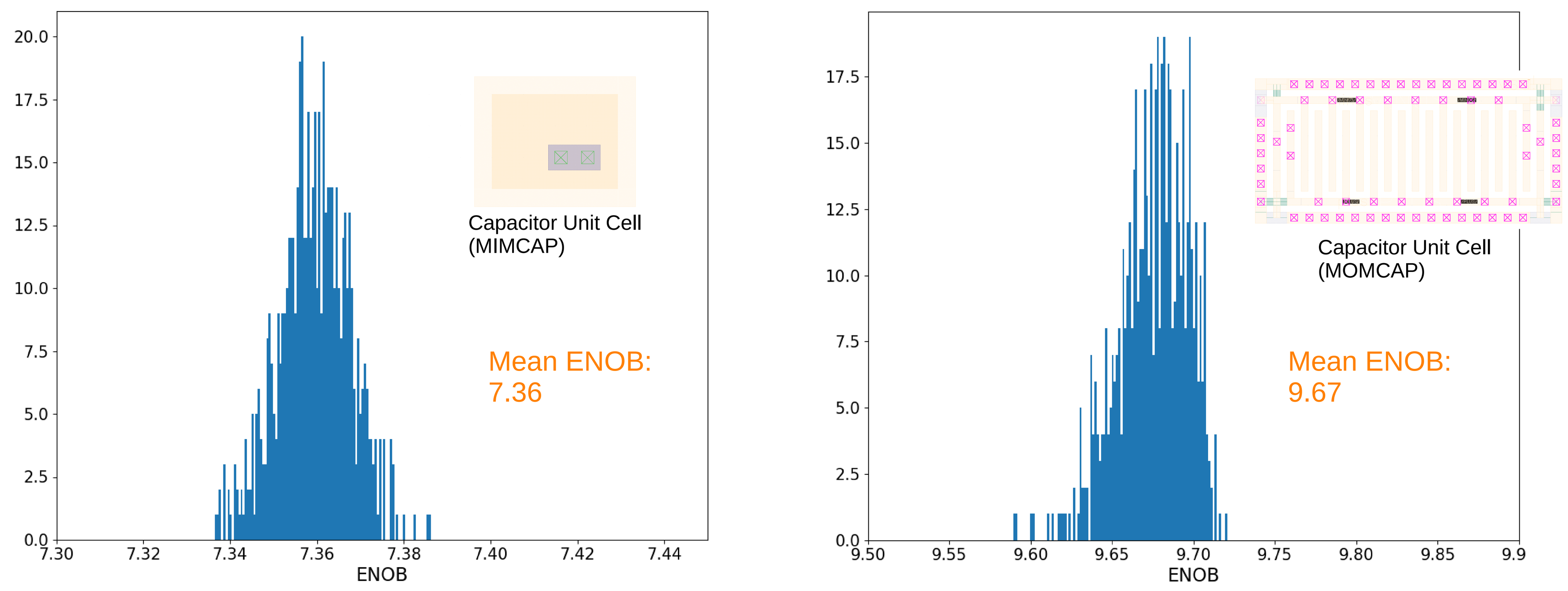
Measurements of predecessor ADC-SAR-04



- Target sample rate: 20MHz
- Poor performance for very low + high ADU counts (on the edge of signal range)
  - Most likely due to **insufficient settling time of the signal** while loading it to the capacitor array
- Poor linearity (DNL > 1) including missing and stuck codes.
  - Most likely due to capacitor **mismatch in the capacitor array**

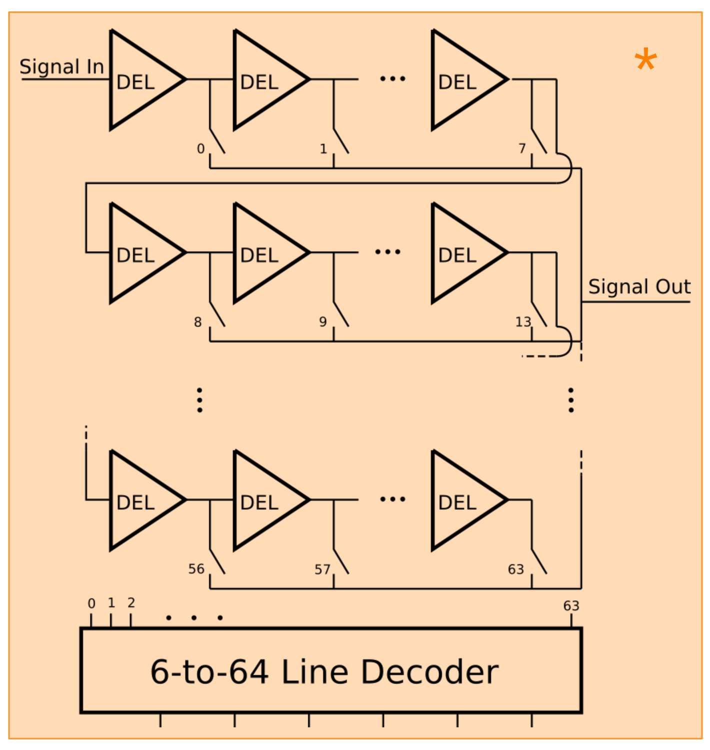
The results show raw data. As shown in [3], calibration can significantly improve the results to an ENOB of 10.

Design of ADC-SAR-05



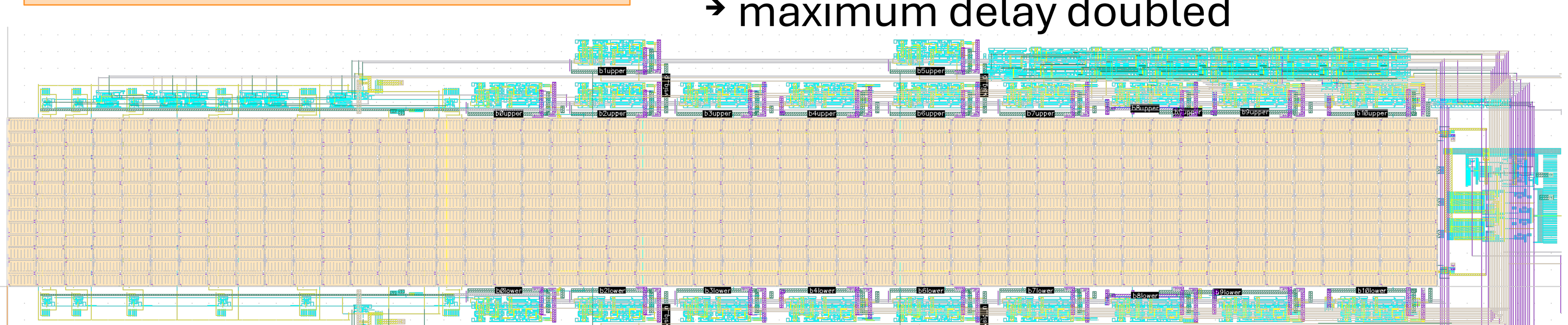
ADC-SAR-04 Capacitor Array *ADC-SAR-05 Capacitor Array*

New unit cell (and layout) of the capacitor array **improves the mismatch** contribution to the ENOB by ~2 bits. Figures show a Monte-Carlo simulation for the random mismatch (given by the foundry) including static mismatch due to parasitic coupling (extracted from layout).



New timing control with much more flexibility and testing features including

- **Separation of signal-charging phase and comparison phase to improve performance on edge of input range**
- Highly granular asynchronous delay chain for each bit (left)
  - → Control comparison time for each bit separately to push for maximum rate
  - → 6 bit granularity instead of 3
  - → ~250ps unit delay
  - → maximum delay doubled



Layout of ADC-SAR-05