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Design of a 12-Bit SAR-ADC for Charge Integrating Pixel Detectors

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JUNGFRAU is a state-of-the-art charge-integrating detector for imaging experiments at synchrotrons and free-electron lasers. It is currently limited to a frame rate of 2.2 kHz. With the goal to increase the frame rate of the detector to > 10 kHz, we have designed a 3.125 Gbps high-speed serial readout recently. Thus, the development of a fast Analog-To-Digital Converter ADC has become our main objective. This poster focuses on design features of the new ADC prototype along simulations and measurements of the GOTTHARD-II ASIC's ADC taken as reference for our new development.

Summary (500 words)

Analog-to-Digital Converters (ADCs) for charge-integrating hybrid pixel detectors (HPDs) can be designed using three different strategies:
1 In-pixel ADCs offer high output rates but are constrained by pixel size, typically supporting slope-based implementation with limited resolution, around 8 bits.
2 Column or shared column ADCs, placed next to the pixel matrix, relax area and power constraints, enabling advanced designs with high resolution (>10 bits). However, multiple pixels connected to a single ADC require a high sampling rate, potentially increasing periphery area and creating larger gaps between tiled modules in large-area HPDs.
3 Off-chip ADCs on a separate readout ASIC have minimal limitations on area and power, offering possibilities for very advanced designs. However, practical limitations arise due to complex readout boards and analog signal integrity considerations.
The photon science detector group at PSI is developing a multi Mega-Samples per second (MS/s), 12-bit ADC based on UMC110 technology for the charge-integrating JUNGFRAU detector [1], aiming for a frame rate exceeding 10 kHz. Requirements for the area and power of the ADC are still under evaluation, targeting a sampling rate of 20 MS/s with a Differential Non-Linearity (DNL) less than 1 Least Significant Bit (LSB) and an Effective Number of Bits (ENOB) equal to or greater than 11. A shared column implementation has been chosen to meet the demands for high speed and resolution.
The poster will introduce the currently designed prototype named ADC-SAR-05. It is based on the ADC used in the GOTTHARD-II ASIC [2], which meets the 20 MS/s requirement with an ENOB of around 10. The new prototype aims to simplify the calibration procedure and improve the ENOB.
A Split Capacitive Digital-to-Analog Conversion Successive Approximation Register (SAR) architecture is utilized in which different capacitors are employed alongside flexible control logic to optimize mismatch and increase ENOB. New features and variants will be presented, along with measurements and simulations from previous ADCs, concluding the factors driving the new design.
ADC-SAR-05 is scheduled for submission in early June 2024 and is expected to be produced by early September 2024. The first test results of this new prototype ADC will be shared and will aid the refinement of our subsequent designs

[1] Characterization results of the JUNGFRAU full scale readout ASIC, A. Mozzanica et al 2016 JINST 11 C02047
[2] Design and first tests of the Gotthard-II readout ASIC for the European X-ray Free-Electron Laser, J. Zhang et al 2021 JINST 16 P04015

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