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High voltage monolithic pixel sensor in 55 nm technology

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The Monolithic Active Pixel Sensor (MAPS) implemented in high-voltage CMOS (HVCMOS) technology is one of the most sophisticated detectors for detecting high-energy particles. Over the past decade, the development of HVCMOS sensors has primarily focused on technology nodes ranging from 180 nm to 130 nm. To explore performance improvements in smaller technology nodes, a prototype of the next-generation HVCMOS sensor has been done using 55 nm high-voltage technology. This technology offers the benefits of smaller feature size and reduced power consumption. The prototype sensor chip was produced in a Multi Project Wafer (MPW) run. It is being tested currently.

Summary (500 words)

Along with the concept design and continuous optimization, many outstanding results have been presented in the past ten years for high energy physics experiment with 180nm to 130 nm technologies. In this article, a next generation of silicon tracking de-tectors using 55 nm technology has been presented.
This chip is designed as a prototype to evaluate the technical route. The prototype chip is mainly consisting of a pixel matrix, a digital readout module and auxiliary mod-ules, such as bias voltage circuits and level shifters. The pixel matrix is the most signif-icant part for particle detecting. It is composed of 26 x 26 pixels and each pixel size is 25 μm x 25μm. In detail, the pixel circuit contains a CSA, a feedback circuit, compara-tor with a tune-DAC and output stages.
In this prototype, both analog and digital readout interface are designed in order to make test and verification on various readout techniques. The left 2 columns are dedicated as digital readout while the other columns are in analog readout. Within either analog or digital readout part, all the pixels are divided into 4 groups where the group name A, B, C, D are assigned to the pixels on 4 corner directions in a 2 x 2 square pixel area. All pixels with the same group name share a common readout bus, resulting in 4 readout buses in each analog or digital readout part. This readout group division method can make sure any adjacent pixels are assigned to different groups and corresponded with different readout buses. When a particle hit on the pixel border area, it can be detected and readout by different readout buses at the same time without overlap. Meanwhile, the number of address lines is largely decreased than previous design by readout bus sharing.
In analog readout, the pixel addresses are recognized by different address reference voltage given by internal DACs. In digital readout, the pixel addresses are binary en-coded. Additionally, the digital readout module calculates the hit timestamp and packages the address information together. It finally serializes the data package and uploads it via serial interface. The internal state machine can be configured with dif-ferent deadtime after a certain hit for data rate controlling and in test pattern genera-tion mode for debugging.
The functionality test as well as time of arrival have been demonstrated by simulation. The forthcoming test results are anticipated to offer vital insights, serving as essential benchmarks for the future advancement of HV-CMOS pixel sensors for tracker.

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