Development of ASIC for CoRDIA, a future camera for pioneering x-ray sources.

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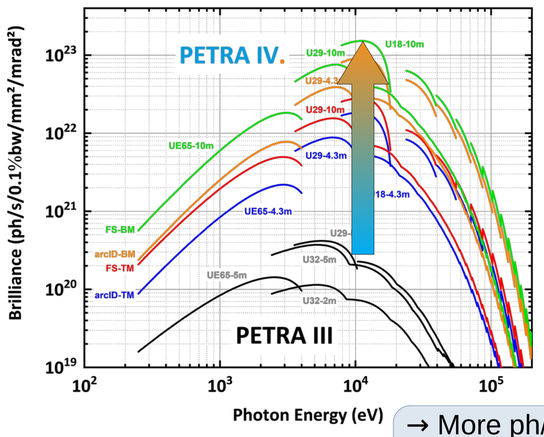
Detector Challenges from Next Generation Synchrotron Sources

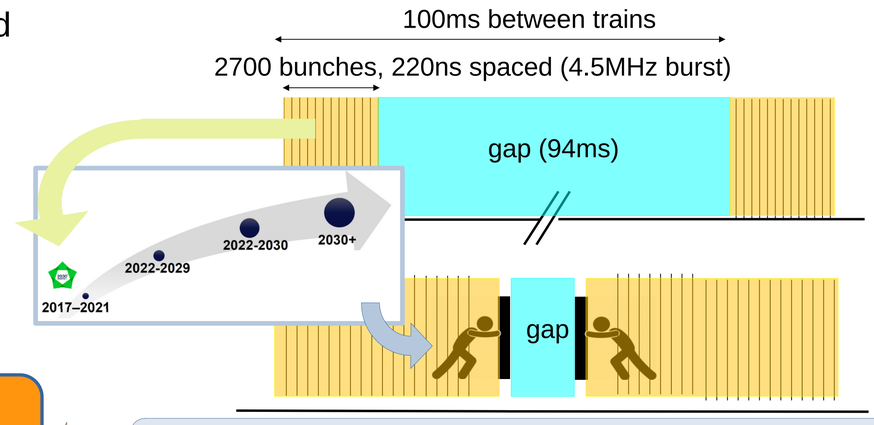
Example: PETRA III →PETRA IV upgrade at DESY



- Upgrade of Synchrotron Rings to the diffraction-limited regime
- Increase in Brilliance by 2 to 4 orders of magnitude
- Higher photon flux on sample by the same order of magnitude
- >10^2 times more photons/s on the detector
  - Increase of the detector's dynamic range by the same order of magnitude or
  - Increase of the frame rate

→ More ph/s on the detector
→ Frame rate requirements in some experiments increase from kHz to >100 kHz

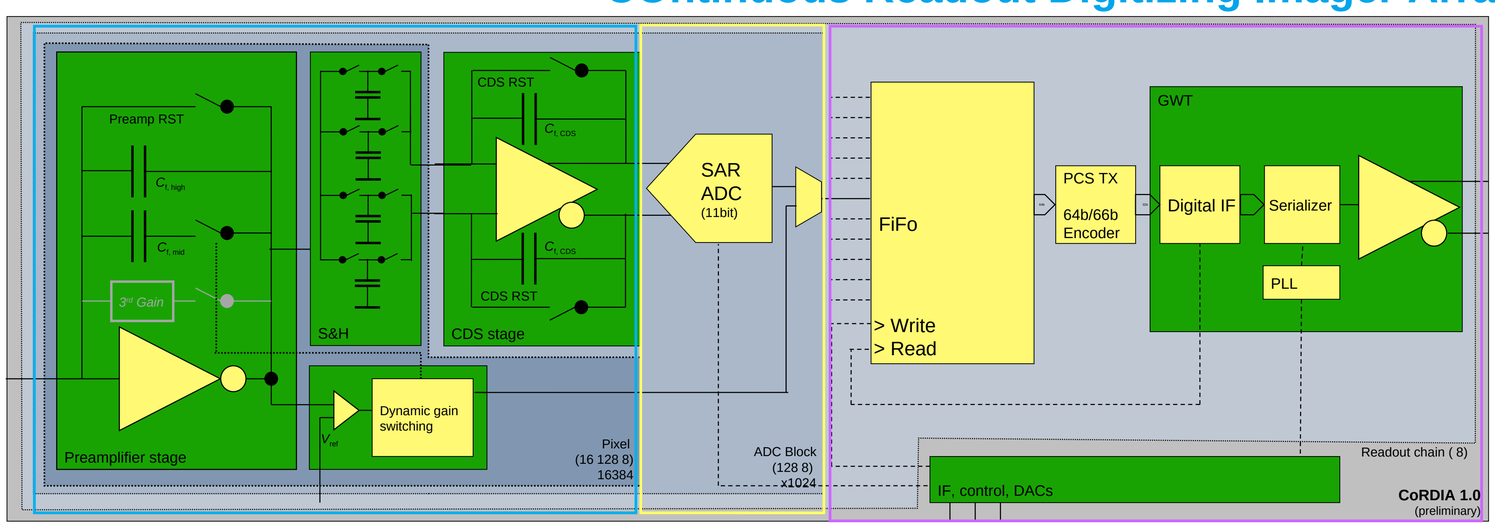
Example: EuXFEL Roadmap

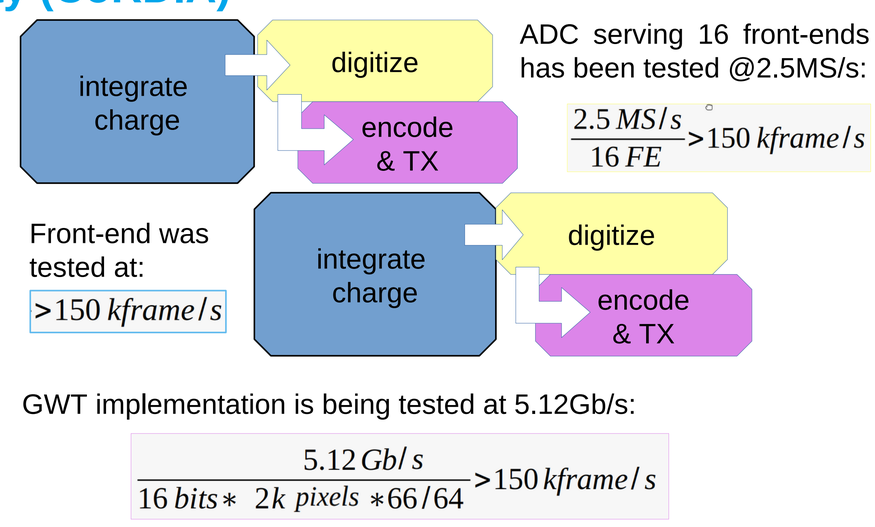


Traditional burst mode operation is no longer the optimal choice
→ continuous readout in excess of 100kHz needed

Common need for:
- **Continuous readout**
- **> 100kHz frame rate**

COntinuous Readout Digitizing Imager Array (CoRDIA)





ADC serving 16 front-ends has been tested @2.5MS/s:

$$\frac{2.5\,MS/s}{16\,FE} > 150\,kframe/s$$

Front-end was tested at:

$>150\,kframe/s$

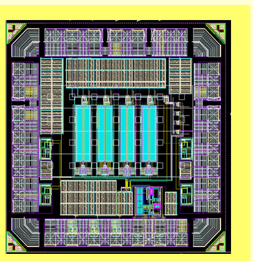
GWT implementation is being tested at 5.12Gb/s:

$$\frac{5.12\,Gb/s}{16\,bits * \ 2k\ pixels\ * 66/64} > 150\,kframe/s$$

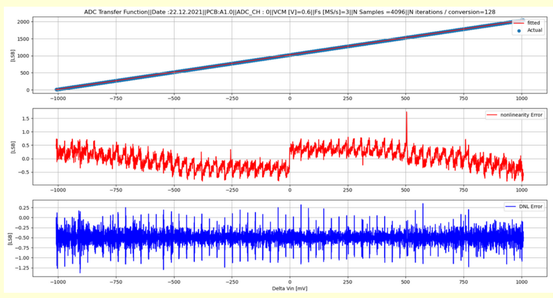
Design Goals

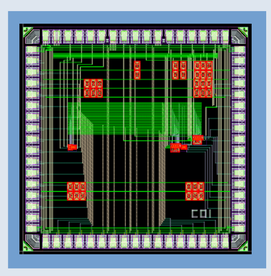
- Pixel size 110µm × 110µm
- ≥ 10k photon Dynamic Range
  - = 1.5 ×10^9 photons/pixel/s
- Continuous Frame Rate f_{FR} ≈ 150kHz (≥100kHz)
- TSVs for gapless tile assembly
- Single-photon sensitive (@ ≤12keV)
- TSMC 65 nm (CERN design kit) technology
- On-chip digitization @ ≥ 10 ENOB
- Dead-time free pipelined operation
- Dynamic gain switching (à la AGIPD)
- Compatibility with high-Z sensors

ASIC Prototypes and test results

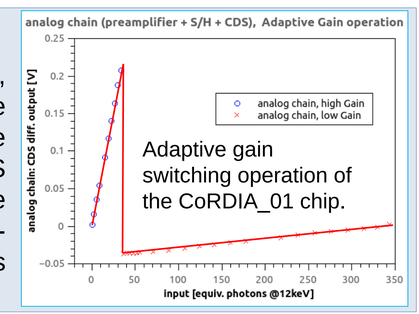


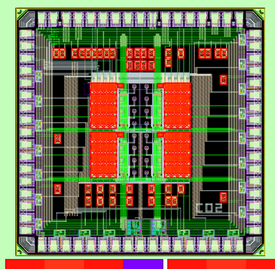
2021: HSI_ADC01 prototype. Designed, manufactured, tested. Used to to evaluate ADC variants based on SAR architecture (exploring redundancy and switching options), and confirm the image sampling capability at the expected frame rate



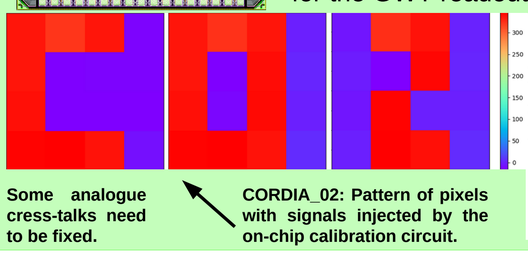


2021: CoRDIA_01 prototype. Designed, manufactured, tested. Used to validate at the expected frame rate the Adaptive Gain circuit, CDS block, the circuit to alternate between two readout sub-chains (to achieve continuous Write-Reading)



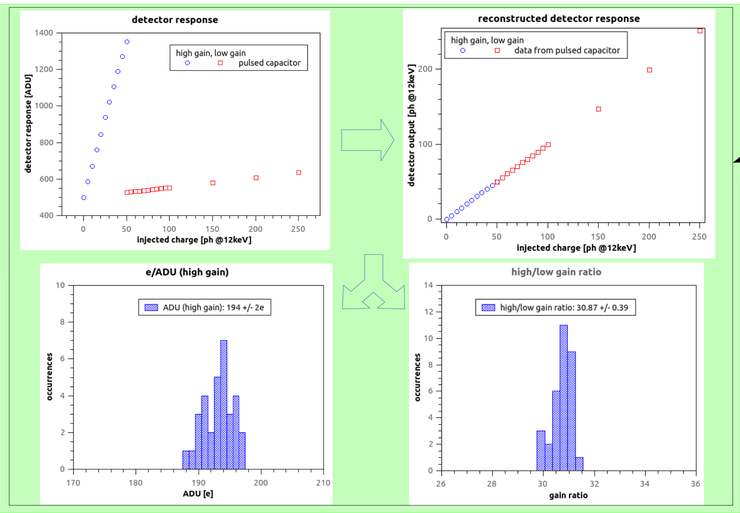


2022: CoRDIA_02 prototype. Designed, manufactured, tested. Implements 4 'Superpixels' - layout blocks consisting of 16 pixel front-ends feeding an ADC. These are building blocks for larger chips and include bump bond pads to the sensor, and the space for the GWT readout structure.



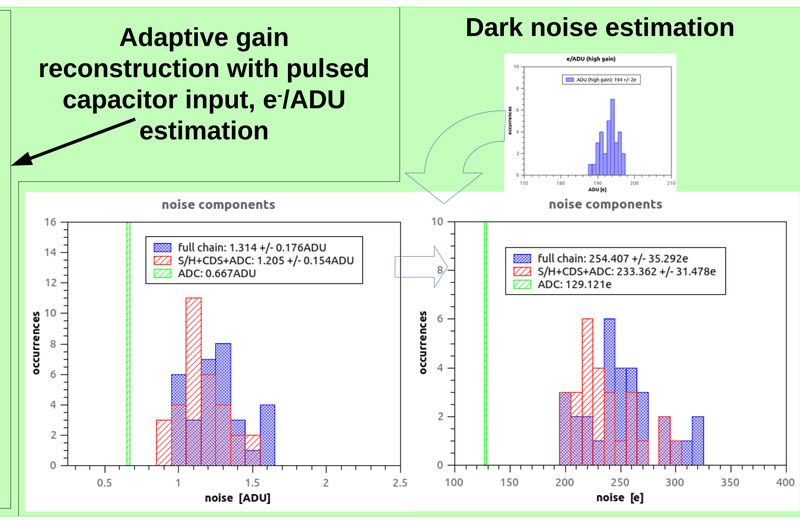
Some analogue cress-talks need to be fixed.

CORDIA_02: Pattern of pixels with signals injected by the on-chip calibration circuit.

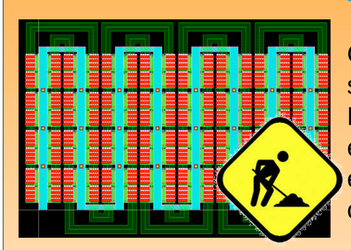


Adaptive gain reconstruction with pulsed capacitor input, e⁻/ADU estimation

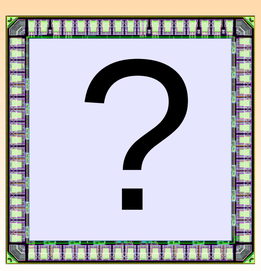
Dark noise estimation



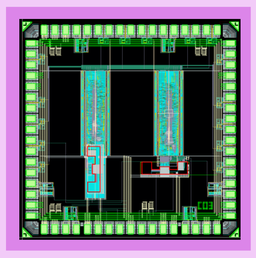
Outlook



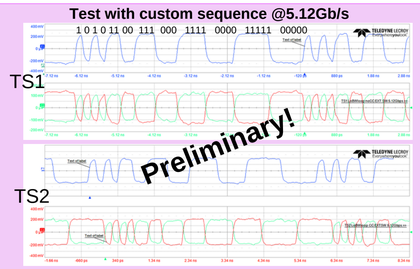
CoRDIA_0**x** prototype-to-come: small-sized ~2k pixel array. Design in progress. Floorplan as a meandering structure to emulate full-size chip size "column" (to estimate eventual drops before full-size chip engineering run).

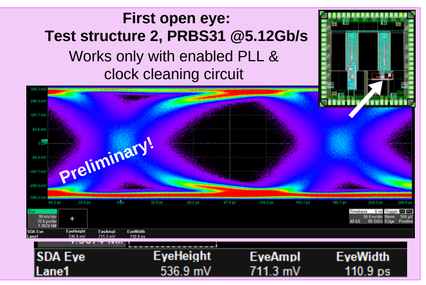


CoRDIA_0**y** prototype-to-come: similar to CoRDIA_02 design with improved analogue "superpixel" layout and possibly additional experimental circuits like digital periphery and alternative building blocks.



2023: CoRDIA_03 prototype. Designed. Manufacturing in progress. *Test in progress!* The goal is to explore/validate variants of the PCS+GWT circuits, optimized to the CoRDIA data flow and overall layout constraints.





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