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Development of ASIC for CoRDIA, a future camera for pioneering x-ray sources

The CoRDIA X-ray detector is a development targeting experiments at modern diffraction-limited synchrotron rings and free-electron lasers operating either in continuous wave or quasi-continuous long burst modes with photon bunch frequencies up to a few 100kHz. It's a hybrid detector with sensitive tiles formed by a read-out ASIC bump bonded to a sensor. Since 2020 4 prototype ASICs were manufactured on order to validate and characterize the single circuit building blocks as well as to prove the concept of the complete detector. Test results, ASIC design details and plans will be presented.

Summary (500 words)

Current developments among the world's largest X-ray facilities, mainly synchrotron rings and free-electron lasers, foresee an upgrade to either Continuous Wave (CW) or slow burst timing modes with a bunch frequencies up to a few 100kHz. This trend along with an aim towards higher photon energies requires novel x-ray detectors that could bridge the gap between the kHz-CW and MHz-burst mode operation regimes. The Continuous Readout Digitizing Imager Array (CoRDIA) is a new hybrid pixel detector being developed to fulfill the requirements of modern photon science emerging from the before-mentioned environment.
CoRDIA is a hybrid pixel detector implementing bump-bonding between the pixels of an Application-Specific Integrated Circuit (ASIC) and a semiconductor sensor. The goal is to provide single photon sensitivity at energies above 12 keV with a dynamic range up to a few 1000 photons and the capability to use High-Z materials within pixels of about 100x100 µm size. The CoRDIA ASIC utilizes an AGIPD-like [1] adaptive gain approach at the front-end but the output data is digitized. The Charge-Sensitive Amplifiers (CSA) each followed by 2 Sample and Hold (S/H) stages allow processing the acquired image during the acquisition of another, thus enabling pipelined operation at ˜150kHz. The analogue front-ends of 16 pixels are multiplexed into a fully differential Correlated Double-Sampling (CDS) stage feeding an 11-bit 2.5MS/s Successive Approximation Register (SAR) Analogue-to-Digital Converter (ADC). This structure forms a "super-pixel", which is then replicated over the ASIC. Data of each 128 ADCs is transferred off the ASIC by a Physical Coding Sublayer Gigabit Wire Transmitter (PCS-GWT) initially designed by Nikhef for the Timepix4 ASIC [2]. The ASIC is being designed in TSMC 65nm technology implementing some RD53 [3] recommendations to improve radiation tolerance. Four Multi-Project Wafer (MPW) prototype ASICs ("HSI_ADC01", "CoRDIA_01-03") were produced during 2021-2023. The 5th prototype "CoRDIA_04"is expected to be submitted next year, and will followed by the full-size chip CoRDIA_10.
The first prototype (CoRDIA_01, 2021) was manufactured to validate the analog front-ends. At the same time a second manufactured prototype (HSI_ADC01, 2021) included several ADC variants. The testing results of both chips were discussed at TWEPP-2023 [4]. A third prototype (CoRDIA_02, 2022) containing 4 "super-pixel"structures, composed from 16 front-ends connected to an ADC, has been designed in order to verify the pipelined image processing. Test results and quantitative characteristics will be presented. A 4th prototype (CoRDIA_03, 2024) with implementations of the PCS-GWT is currently under test, first results will be available. A prototype ASIC of the full readout chain (CoRDIA_04), bondable to a sensor, is being developed and the design details will be discussed.

[1] A. Allahgholi et al. The Adaptive Gain Integrating Pixel Detector at the European XFEL. J Synchrotron Radiat. 2019 Jan 1;26(Pt 1):74-82. doi: 10.1107/S1600577518016077. Epub 2019 Jan 1. PMID: 30655470; PMCID: PMC6337892.
[2] X. Llopart et al 2022 JINST 17 C01044

[3] RD53 Collaboration, “The RD53A Integrated Circuit,”CERN-RD53-PUB-17-001 (2017).
[4] A. Marras et al 2024 JINST 19 C03006

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