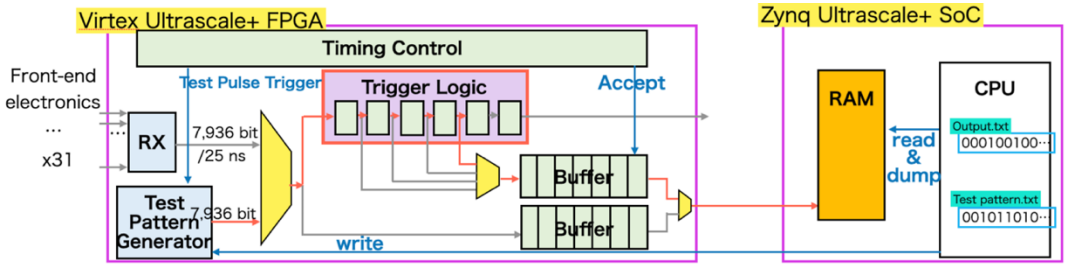

Figure 1: Schematic diagram for the implementation around Zynq SoC

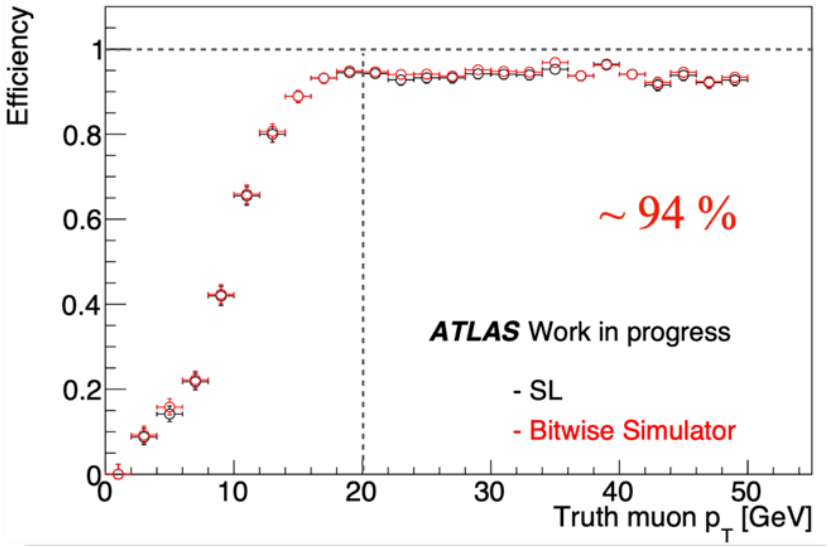

Figure 2: Efficiency estimation between outputs of actual hardware data processing and software-based simulation