Contribution ID: **132** Type: **Oral**

Applications of PixESL framework on pixel detectors for High Energy Physics experiments

Wednesday 2 October 2024 15:30 (20 minutes)

PixESL is a virtual prototyping framework tailored for forthcoming particle detectors. It aims to enable high-level abstraction for describing detectors developed in High Energy Physics experiments, simulating the entire chain from particle interaction to data packet readout. This contribution describes three different models developed in the PixESL framework for pixel detector applications: a timing-oriented pixel design including an analog front-end and in-pixel clustering, a data-driven pixel array readout architecture, and a triggered pixel array readout architecture. The first two models are inspired by the LHCb VeLo upgrade II, while the third one by the CMS ITk Phase-II upgrade design (RD53c).

Summary (500 words)

In the industry, high-level modelling serves as a standard method for enhancing system designs at early stages. Acknowledging its effectiveness, advocating for adopting such a technique in HEP becomes imperative to improve the optimization and refinement of electronic systems. To address this need, we introduced PixESL: a SystemC framework designed to model the readout chain comprehensively, spanning from front-end chips to detector back-ends.

This contribution marks the framework's initial implementation, encompassing the modelling of analog front-ends (AFE), asynchronous and synchronous digital logic, and data-driven or triggered readout architectures. In addition, it describes the application of these models as a golden reference for the verification environment.

PixESL employs the Electronic System-Level (ESL) design approach and incorporates SystemC and C++ classes to model both analog-mixed signal and digital circuitry, enabling the creation of a component library for architecture generation. Python-based scripts analyse simulation data, offering performance estimation and visualization that can be used for architecture optimization.

In this contribution, we report three models including the simulation results to demonstrate the capabilities of the proposed approach:

Timing-oriented pixel front-end: based on the LHCb VeLo upgrade II requirements, it features a matrix of 256x256 pixels. The modelling of the AFE replicates the behaviour of the analog and mixed-signal simulation. The digital front-end model includes the asynchronous logic, clustering, and data processing of a pixel. The framework builds the matrix, with 24 neighbouring connections each, in tens of seconds and simulates around 16k hits per second with a memory footprint of 3.5 GB showing a ˜50x faster simulation time compared to RTL.

Data-driven readout network: based on the same LHCb Velo upgrade II requirements, it combines the readout network model with the pixel model. The framework provides a complete simulation platform of the electronic system starting from the output of the physical Monte-Carlo simulation, and modelling both the analog front-end and digital back-end. This allows the user to build a reference model and evaluate the sources of inefficiencies. By using this model in a verification environment, the user can distinguish between RTL design bugs/inconsistencies and architecture inefficiencies. The readout simulation takes 15 seconds for 1000 BX cycles with 5 seconds of build time.

Triggered readout network: based on the CMS ITk Phase-II upgrade, it studies the pixel array readout of the RD53c architecture. For this purpose, PixESL includes C++ classes and SystemC modules able to model

triggered readout architectures such as a trigger table and a specialized trigger layer. The model simulation results show a lossless operation up to trigger rates around 7 MHz, well above specification, pointing to possible architecture optimization. The readout simulation takes longer than the previous one (x2) due to the triggered architecture but with a similar build time.

In conclusion, the PixESL enables comprehensive analysis and optimization of electronic system components and their interactions. By simulating the entire chain early in the project lifecycle, designers can identify potential bottlenecks, evaluate design trade-offs, and refine specifications to meet the experiment's requirements within the given power budget and resource constraints.

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Session Classification: Programmable Logic, Design and Verification Tools and Methods

Track Classification: Programmable Logic, Design and Verification Tools and Methods