# A Low-Cost, Low-Power Media Converter Solution for Next-Generation Detector Readout Systems

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HEP data acquisition systems are often built from high-end FPGAs. As such systems scale in the HL-LHC era, severe underutilization of FPGA transceivers can occur because frontend links prioritize radiation hardness and power consumption over raw data bandwidth. This work evaluates recently introduced low-power, low-cost FPGA devices as an alternative building block for future readout architectures. We implement a readout backend on FPGA where the frontend protocol is based on the Low-Power GigaBit Transceiver (lpGBT) and the readout protocol is based on 10 Gigabit Ethernet, using the LHCb Run 4 RICH detector as a practical case study.

**Summary**

The next-generation of detectors in Large Hadron Collider (LHC) experiments will require higher bandwidth readouts, widely using radiation-hard Low Power GigaBit Transceiver (lpGBT) links. Current designs rely on expensive, high performance FPGAs to interface with the readout systems. However, our design offers a compact, resource-efficient smart media converter aiming at translating lpGBT to Ethernet.

Within our converter architecture, each lpGBT link feeds a pipeline where lpGBT words are buffered to form a packet with configurable size to reduce the impact of UDP/IP header overhead. Packets are subsequently transmitted on a dedicated 10 Gigabit Ethernet (10GbE) link. The choice of 10GbE aligns with lpGBT data rates and is compatible with most low-cost FPGA transceiver speeds and hard IPs, ensuring both compatibility and cost effectiveness. Notably, the entire data pipeline has been constructed using open-source, vendor-independent cores, enhancing portability across different FPGA devices.
A key feature of our media converter is the integration of a soft microcontroller unit (MCU), facilitating remote control, monitoring, and configuration via MQTT over a dedicated 1GbE interface.

This design represents a significant improvement in terms of flexibility, scalability, and modularity compared to existing systems. It is well-suited to a range of applications, from basic testbench and test beam setups, where direct interfacing with a network interface card is feasible, to large-scale detector systems, where multiple converters can be aggregated using off-the-shelf Ethernet switches.

The hardware implementation and testing phase utilized an AMD Artix Ultrascale+ DevKit, capable of accommodating up to four lpGBT links. Results demonstrate that full throughput of 9 Gbps can be achieved with packet sizes exceeding 3kB, with no backpressure. The low resource usage indicates the possibility of adding some basic data processing on device.

Emulation of a frontend is done using a Zynq Ultrascale+ and a VLDB+ board, simulating the LHCb Run 4 RICH readout (fastRICH) data encoding. Once the real frontend ASIC will be available, the test harness will already be available and tested, reducing the time needed for setup and debugging.

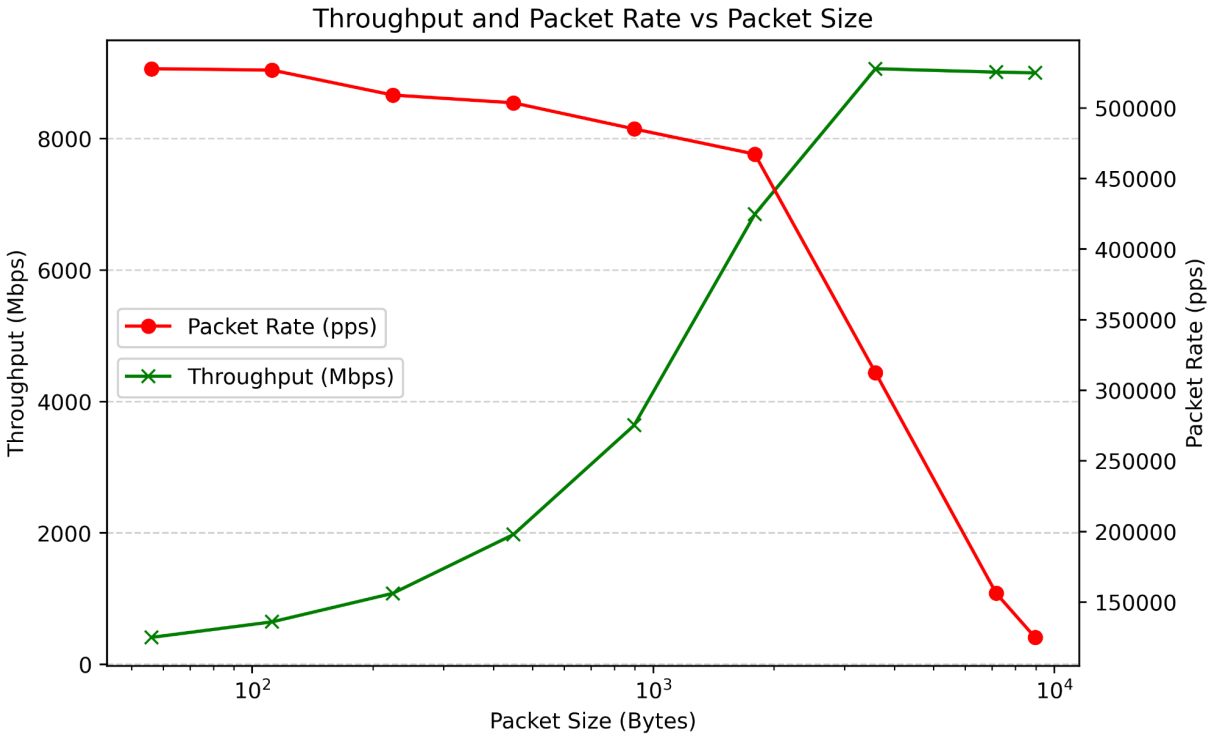


**Figure 1.** Measured throughput and packet rate as a function of packet sizes. With sizes smaller than 3584 bytes, the packet rate saturates the host processing capability. Packet loss is avoided by increasing the packet size.