Functional verification methodology for OBELIX, the monolithic active pixel sensor for the proposed upgrade of the Belle II vertex detector at SuperKEKB

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Abstract This contribution presents the methodology and verification strategy for OBELIX, the monolithic active pixel CMOS sensor designed for the proposed upgrade of the Belle II vertex detector. Leveraging a dual verification approach with COCOTB and UVM, we ensure the integrity of OBELIX's digital logic. This methodology addresses the complexities of ASIC design, which includes an 896x464 pixel matrix with 7 bits Time-over-Threshold (ToT) resolution per pixel and implements a trigger logic with two stages of memory. Through comparative analysis, we enhance error detection during the design phase, thereby bolstering confidence in OBELIX's functionality.

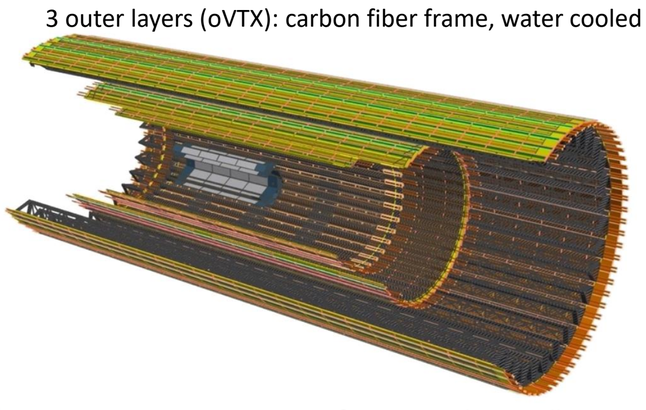
Belle II Vertex Detector (VTX) Upgrade Proposal

Detector Upgrade

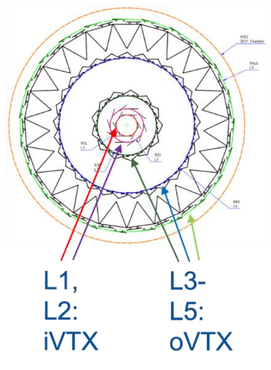
- Belle II experiment is taking data at the SuperKEKB e^+- e^- collider (Japan);
- **Collider upgrade** in ~**2028**: **Luminosity** from **0.47x10^{35}** to **6x10^{35}** cm^{-2}s^{-1} ➡ worst beam background
- Needs for a better tracker: lower occupancy and fake-rate;
- Currently 2 Layers of pixel sensor + 3 layers of silicon strip ➡ **5 Layers** of Deployed Monolithic Active Pixels Sensors (**DMAPS**)

2 innermost layers (iVTX): all-silicon, self supported, air cooled (0.2 % X_0)
3 outer layers (oVTX): carbon fiber frame, water cooled (0.3 – 0.8 % X_0)

Total material budget ≤ 2.0 % X_0



Installation during the collider upgrade

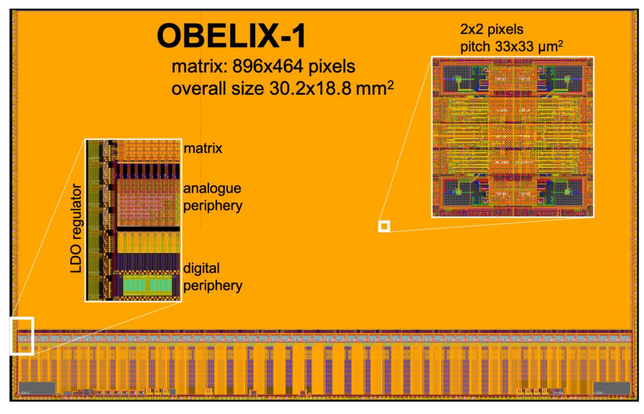


More information about Belle II upgrade is in arxiv:2406.19421

OBELIX

TJ-Monopix2 sensor
(Developed for ATLAS-ITK: doi: 10.1016/j.nima.2020.164460) ➡ forerunner for OBELIX

Specifications	
Fine time stamping	~5 ns for hit rate <10 MHz/cm^2
Hit rate max for 100% eff.	120 MHz/cm^2
Trigger handling	30 kHz with 10 μs latency
Trigger output	~10 ns resolution with low granularity
Power	120-200 mW/cm^2
Time stamping	50-100 ns
Bandwidth	320 MHz



The OBELIX design is described in more detail in poster No. **154**: "*Design of the OBELIX Monolithic CMOS Pixel Sensor for an Upgrade of the Belle II Vertex Detector*" by Roua Boudagga.

OBELIX Functional Verification Architecture

UVM (Universal Verification Methodology)

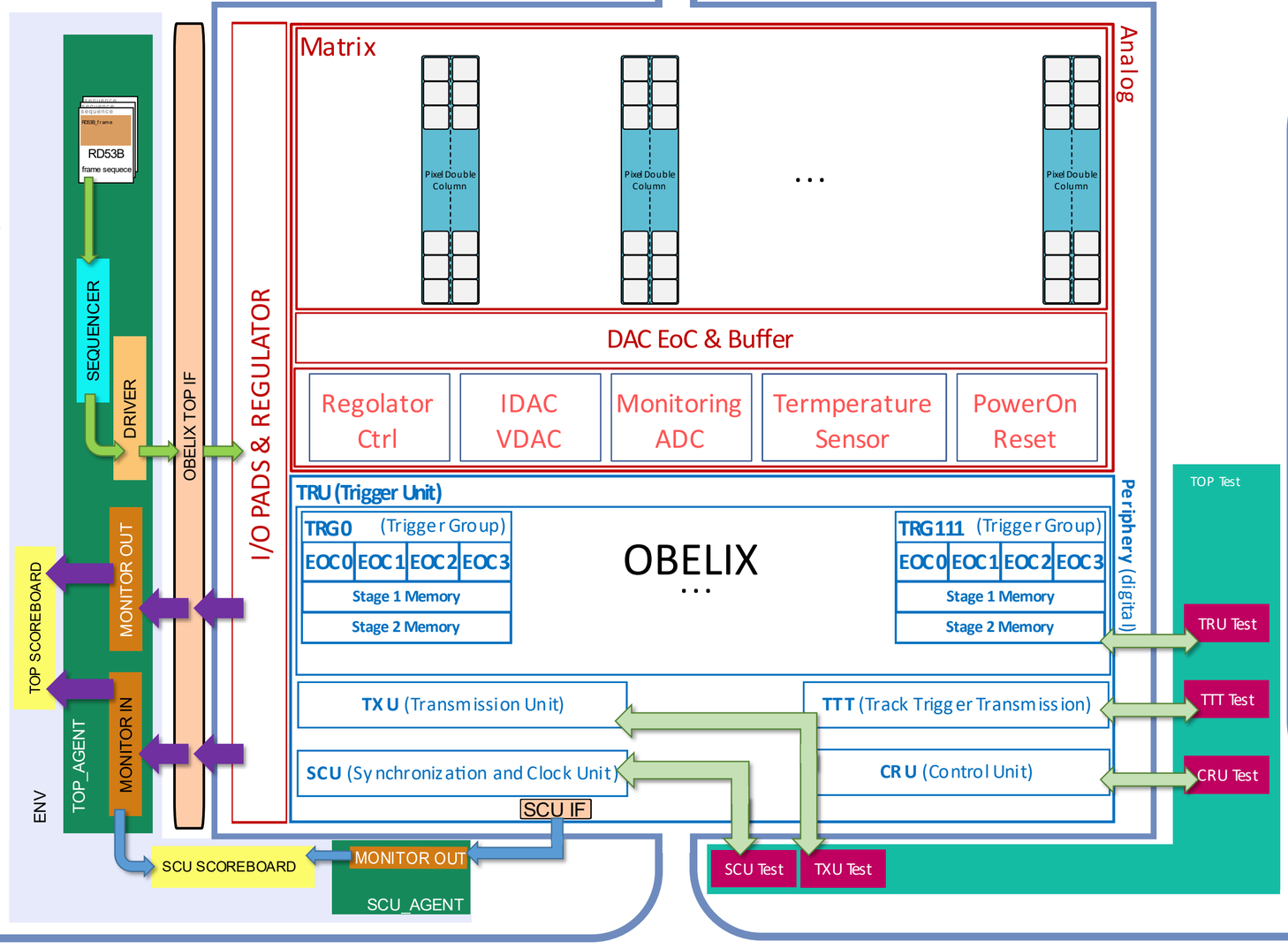
- **Based on SystemVerilog**;
- Highly structured in a hierarchical manner;
- Separate development with respect to the design, to reduce bias;
- **Verification plan** outlining OBELIX features to be scrutinized from a top view design prospective;
- **Metric-driven verification utilizing code and functional coverage**;
- System operation emulation approach;
- Access to inner blocks of the design from the top module without changing the design (using the *bind* construct), e.g., Synchronization and Clock Unit;
- **Constrained random** RD53B protocol compliant input frame generation;
- Test-specific **parametrized constraint activation** (via *plusargs* command line argument);
- Hits collection emulated via the injection circuit;
- In the TOP_SCOREBOARD, the reference model is computed by decoding the command and payload RD53B input frame received from the MONITOR_IN, and decoding the 8b10b stream received from the MONITOR_OUT of the TOP_AGENT.

UVM top output data flow
UVM top input data flow
UVM scu output data flow

COCOTB (COrouting COsimulation TestBench)

- **Based on Python**;
- **Easier to access and more intuitive compared to UVM**;
- The tests for OBELIX are developed by the designer to verify each module.;
- **Fully integrated with CI/CD GitLab workflow**;
- Based on multiple tests for specific aspects of the design;
- Open-Source;
- **Easily integrable with the test acquisition system**.

COCOTB data flow



ResetL		0%
WrReg		100%
RdReg		100%
RegAddrCmd	[8:0]	100%
RegDataCmd	[15:0]	100%
RegData	[15:0]	75%
RegDataRdy		100%
IBIAS	[7:0]	0%
ITHR	[7:0]	0%
ICASN	[7:0]	0%
IDB	[7:0]	0%
ITUNE	[7:0]	75%
ICOMP	[7:0]	75%
IDEL	[7:0]	25%
IRAM	[7:0]	50%
VRESET_N	[7:0]	0%
VRESET_HV	[7:0]	0%
VCASP	[7:0]	0%
VCASC	[7:0]	0%
VCLIP	[7:0]	0%
VPULSE	[7:0]	0%
IR2R	[7:0]	87.5%
LDO_VDDAL	[7:0]	37.5%
LDO_VDDAR	[7:0]	12.5%
LDO_VDDD	[7:0]	12.5%
LDO_VPC	[7:0]	25%
MON_I_MUX	[3:0]	0%

Example of coverage data:
It enables a quantitative assessment of the portions of the design covered by the tests performed. This allows for the selection of stimulation constraints or test cases that explore different areas of the design's state space, working towards coverage closure.

Summary

The verification strategy for the OBELIX ASIC involves a dual approach to ensure robust functionality. COCOTB, written in Python, was used during the development phase to validate individual blocks of the digital logic. Afterwards, it is also being applied to verify the full chip periphery. The Universal Verification Methodology (UVM), implemented in SystemVerilog, is used to orchestrate top-level validation through a structured verification plan, focusing on chip control and configuration paths. This dual approach enhances error detection by enabling comparative analysis of results. The created framework is reusable for verifying the OBELIX-2 successor, ensuring efficient adaptation for future developments.

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