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FPGA Emulation of the Digital Readout of a HV-CMOS sensor chip: MightyPix for LHCb Upgrade II

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MightyPix is the first iteration of a High-Voltage CMOS (HV-CMOS) sensor chip developed for the LHCb Mighty Tracker. The digital readout of this chip is compatible to LHCb specifications. To verify the digital functionality of the chip in an LHCb environment, an emulator has been developed . This setup comprises the FPGA, CERN's developed VLDB, some custom interface boards and support electronics. The emulated design can be used for testing the DAQ chain, firmware and I2C communication between lpGBT and emulated chip. The data transmission from lpgbt to emulated chip over I2C is successfully done and observed on the oscilloscope.

Summary (500 words)

The Mighty Tracker is a proposed LHCb Upgrade II system, that incorporate both the scintillating fibres (Sci-Fi) in the outer region and the silicon in central region. The inner central part of current Sci-Fi is replaced with a high-radiation-tolerant monolithic HV-CMOS detector called MightyPix . The MightyPix chip is required to be compatible with LHCb specifications: 40 MHz clock, use lpGBT protocol and meet Timing and Fast Control (TFC) & Experiment Control System (ECS) commands. The first prototype of this chip featuring a CMOS amplifier and comparator in the pixel design was delivered in 2023 and is currently being evaluated. An FPGA chip emulation framework is being developed to test and verify the chip's digital readout. The functionality of chip can be replicated on an FPGA emulated chip to verify the chip electronics within LHCb environment and protocols. The emulation set up is used to test the DAQ chain, data generator, and firmware. To validate these functions, an FPGA chip emulation setup has been constructed. The setup comprises- Mercury Kintex-7 series FPGA, MIO3 adapter board - a custom interface board developed by University of Bonn and Versatile Link Demonstrator Board (VLDB) , an evaluation kit developed by CERN which has (Low Power Gigabit Transceiver)lpgbt, Versatile link Transceiver(VTRX) and DC-DC mounted on it. To configure the lpgbt a Raspberry Pi and piGBT web application is used. A bi-directional logic level converter is added to the setup due to voltage incompatibility between lpgbt(1.2V) and emulated FPGA(1.8V). This allows to establish the I2C communication between emulated FPGA chip (slave) and lpGBT (master).

To initiate I2C communication, a trial communication is setup between the lpGBT (master) and VTRX (slave), both mounted on the VLDB board to check the basic configuration and functionality of the lpGBT. Once its verified, the VTRX slave is replaced with the emulated chip. Subsequently some files from the lpGBT library, are installed on the Raspberry Pi to provide I2C functional commands.

After completing the initial settings and coding for the correct slave and register addresses in the piGBT software, the new program is uploaded on the emulated FPGA. To verify the functionality of the emulated chip, Serial Clock line(SCL)-40MHz and Serial Data line(SDA) with the I2C acknowledgement(ACK) can be observed on the logic analyser screen as well as oscilloscope.

Once the chip has been configured correctly, new files and programs to transmit digital output data are added to the system, such that data from the emulated chip can be compared to the data from real chip. The next goal is to test TFC commands in the chip using lpgbt protocol and later incorporate the real MightyPix chip in the setup using a chip carrier board to test the DAQ chain and implement all these functions on a real chip.

This talk will cover a brief introduction about the MightyPix chip and FPGA chip emulation including the setup, its importance, problems faced and their solutions, along with some results. Additionally, some insights into the short-term and long-term plan will be discussed.

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