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Development of the firmware logic validation system using the FPGA accelerator

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Validation of the recent FPGA firmware logic used in particle physics is being hard, since the implemented logic becomes larger and more complex with increasing FPGA resources. In order to address efficiently, we have developed a firmware validation system using the FPGA accelerator produced by FPGA vendors. We have established a system by developing the interface with CPU of host computer, which receives and sends various size of input/output data. The concept and details of implementation of the developed system will be presented.

Summary (500 words)

Validation of firmware logic used in particle physics is being hard, since the implemented logic becomes larger and more complex with increasing FPGA resources. The logic validation is mandatory for the successful experiments, hence the efficient validation is crucial to enhance the development speed of the logic. We have applied the FPGA accelerator, which is attracting attention as one of heterogeneous computing device, to a firmware verification system.

The logic is often implemented on the original dedicated board. The logic validation is difficult by using this board directly, since there are many tasks to prepare data and to transfer it between FPGA, and to verify the output. Moreover, this needs one more computers to handle data and the verification, thus the validation speed is limited due to input and output bandwidth with the computer. In addition, this approach requires the developer to have the board which is recently very expensive, to validate the logic in hand. The FPGA accelerators can solve these problems. In one computer, an accelerator board connected via the PCIe interface can receive data generated by CPU of host computer, return the output after passing through the logic, compare with the expected response.

We have developed a system to facilitate smooth communication between the CPU and the accelerator. In this time, we utilized Alveo U200 produced by Xilinx/AMD. Although the U200 has the same resource as the Virtex UltraScale XCVU9P, it is more cost-effective than the XCVU9P chip because of the commercial device and the restricting I/O pins.

Communication between DDR on the accelerator board and FPGA is performed by the AXI interface. The AXI interface has the number of data bits, the special treatment is needed to handle bigger input/output data bits. The developed system converts from the data on the DDR to a input format of the validated logic. Read out from the logic is also be converted to a format that can be handle by the AXI interface.

The developed system uses less than 0.1% of the U200 resources, which it results the large logic can be implemented. The input/output speed depends on the size of the data, but 500 bits of data can be input to the firmware logic approximately 100,000 times per second. Therefore, large firmware logic can be validated at the high speed using any patterns such as generated in Monte-Carlo simulation and realistic data.

The developed system is applicable to the different types of firmware and for the experiments.

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