Building up to the CMS HGCAL DAQ

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On behalf of the CMS collaboration

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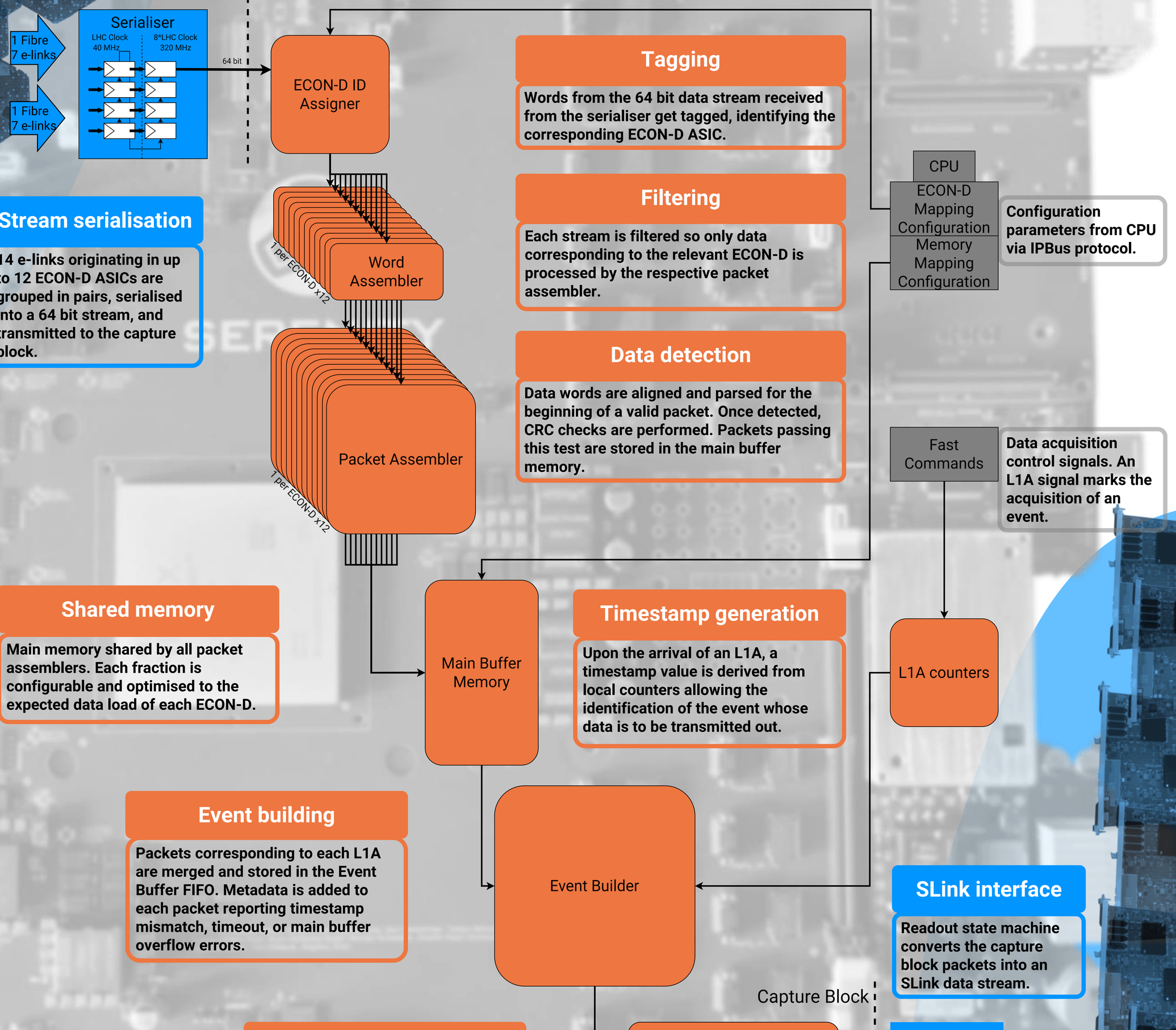
The CMS Collaboration will replace its current endcap calorimeters with a new high granularity calorimeter (HGCAL) for operations at the HL-LHC. The HGCAL back-end DAQ system comprises 96 FPGA-based ATCA boards, each processing data from 108 input optical fibres operating at 10 Gb/s. This poster describes in detail the architecture and prototyping of the elementary readout unit in the back-end DAQ system of the HGCAL. We then describe its integration and performance in a full detector test system. The resulting system provides an average data acquisition throughput at the detector's nominal rate of 750 thousand events per second.

30’000 ASICs to read out



Stream serialisation

14 e-links originating in up to 12 ECON-D ASICs are grouped in pairs, serialised into a 64 bit stream, and transmitted to the capture block.

Tagging

Words from the 64 bit data stream received from the serialiser get tagged, identifying the corresponding ECON-D ASIC.

Filtering

Each stream is filtered so only data corresponding to the relevant ECON-D is processed by the respective packet assembler.

Data detection

Data words are aligned and parsed for the beginning of a valid packet. Once detected, CRC checks are performed. Packets passing this test are stored in the main buffer memory.

Configuration parameters from CPU via IPBus protocol.

Data acquisition control signals. An L1A signal marks the acquisition of an event.

Shared memory

Main memory shared by all packet assemblers. Each fraction is configurable and optimised to the expected data load of each ECON-D.

Timestamp generation

Upon the arrival of an L1A, a timestamp value is derived from local counters allowing the identification of the event whose data is to be transmitted out.

Event building

Packets corresponding to each L1A are merged and stored in the Event Buffer FIFO. Metadata is added to each packet reporting timestamp mismatch, timeout, or main buffer overflow errors.

SLink interface

Readout state machine converts the capture block packets into an SLink data stream.

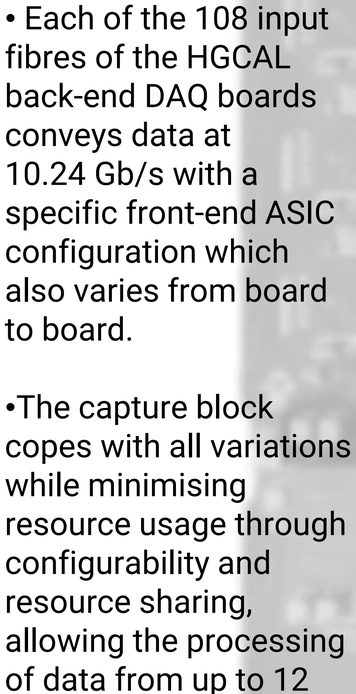
Dispatching

Capture Block interface exposing data packets (and respective size) ready to be transmitted to the SLink output.

The elementary HGCAL DAQ unit, the capture block

- Each of the 108 input fibres of the HGCAL back-end DAQ boards conveys data at 10.24 Gb/s with a specific front-end ASIC configuration which also varies from board to board.

- The capture block copes with all variations while minimising resource usage through configurability and resource sharing, allowing the processing of data from up to 12 ECON-D front-end ASICs across 14 data e-links (2 fibres).

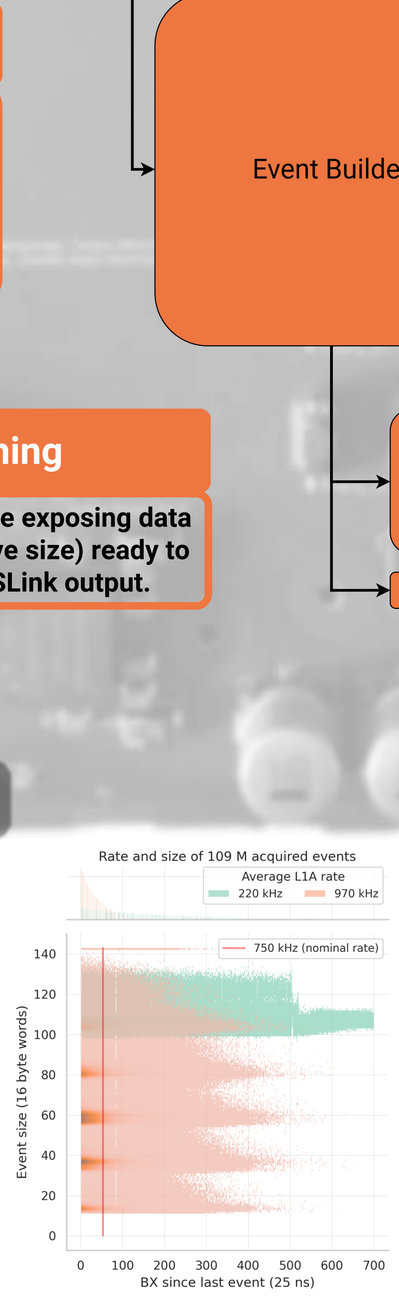


Vivado design implementation targeting a VU7P FPGA for a beamtest in August 2024. The two implemented capture blocks are highlighted in orange.

On-going Work

- Scaling up this small system up to the final size of 54 capture blocks per VU13P FPGA is the next challenge ahead.

- Heavy focus on load balanced data transmission across the FPGA.



Performance

- Two capture blocks were integrated into a test system used at a beamtest experiment at CERN’s north area, having undergone validation with real beam data!

1150 SLinks to feed

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