Contribution ID: **30** Type: **Poster**

Back-end DAQ system prototype testing and integration on a full detector test system for the CMS HGCAL detector

Tuesday 1 October 2024 17:00 (20 minutes)

The CMS Collaboration will replace its current endcap calorimeters with a new high granularity calorimeter (HGCAL) for operations at the HL-LHC. The HGCAL back-end DAQ system comprises 96 FPGA-based ATCA boards, each processing data from 108 input optical fibres operating at 10 Gb/s. This paper describes in detail the architecture and prototyping of the elementary readout unit in the back-end DAQ system of the HGCAL. We then describe its integration and performance in a full detector test system. The resulting system provides an average data acquisition throughput at the detector's nominal rate of 750 thousand events per second.

Summary (500 words)

The envisaged CMS HGCAL back-end DAQ system consists of 96 FPGA-based ATCA boards each of which processes data from 108 fibre optic links operating at 10.24 Gb/s. The incoming data undergo an event-building process and the aggregated data are transmitted to the central CMS system via 12 fibre optic links, operating at 25 Gb/s. A first complete prototype test system was assembled to validate the HGCAL interfaces throughout the entire data chain. This system includes a single ATCA board prototype and 2 input fibre optic links conveying DAQ data from the front-end electronics. The hardware loaded in the FPGA includes a reduced version of the back-end DAQ, the mini DAQ (mDAQ), which processes the data of a scaled-down HGCAL front-end.

The mDAQ has two components: a serialiser and a capture block, the elementary DAQ unit of the HCGAL back-end. The capture block is responsible for performing event building from data received from up to 12 front-end concentrator ASICs, spread across up to 14 serial e-links in a configurable manner. This is achieved by splitting the incoming data stream into up to 12 separate streams, each corresponding to a single data concentrator ASIC. For each of these streams, data packets are detected using a dedicated header word and validated by doing CRC error checks in each packet header word. Afterwards, valid packets from the different ASICs belonging to the same event are merged into a single back-end DAQ packet and transmitted out. The mDAQ was successfully integrated into a test system used in laboratory and beam test environments, allowing the first hardware prototyping of the back-end DAQ system of HGCAL. The mDAQ managed to handle not only the nominal CMS Phase 2 average trigger rate of 750 kHz but also explored and validated corner cases such as the processing of single-word ASIC packets and error handling. The Back-end DAQ system prototype is undergoing horizontal scaling towards the dimensions of the final HGCAL back-end DAQ system comprising 54 capture blocks. It is anticipated that the outputs of these 54 blocks will be partially combined into the 12 link 25Gb/s output streams through an interconnect router providing load balancing.

This paper describes in detail the architecture of the mDAQ and its role in the overall back-end DAQ system of the HGCAL. Furthermore, its prototyping and testing are also discussed, having culminated in the assessment of its performance through its integration in a full detector test system in both laboratory and beam-test environments. The results show a performance compliant with the phase 2 upgrade requirement of an average throughput of 750 thousand events per second.

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Session Classification: Tuesday posters session

Track Classification: Programmable Logic, Design and Verification Tools and Methods