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Feature Extraction on the TRD readout FPGA with HLS in the mCBM Experiment

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The CBM experiment uses a free streaming DAQ with interaction rates up to 10MHz resulting in data rates, which exceed storage capabilities, necessitating online processing. The SPADIC ASIC of the CBM-TRD provides hit messages with oscilloscope-like sampling of the detector data, encoding valuable information. To speed up data unpacking and free up computing time, feature extraction is moved to the readout FPGA. In the mCBM experiment, this approach is tested, demonstrating the benefits of HLS and C++ template programming for algorithm development. Results show resolution improvements and significant reductions in data volume and unpacking speed at the computing cluster.

Summary (500 words)

The CBM (Compressed Baryonic Matter) experiment at FAIR will focus on rare probes of the QCD phase diagram at high net-baryon densities. Planned interaction rates of up to 10MHz and a free-streaming DAQ result in data rates that exceed temporary storage capabilities. Therefore, the data needs to be processed online, and only interesting events will be written to storage.

The front-end ASIC of the CBM-TRD, the SPADIC, provides self-triggered timestamped hit messages that contain an oscilloscope-like sampling of the detector data. The transmitted signal shape encodes a lot of information, such as the ADC baseline level, the deposited charge on a detector pad, or the shift of the ASIC trigger time with respect to the pad response function of the detector, given by the sampling time of the ASIC. However, decoding and extracting this information in software in real-time requires significant computing time, taking away valuable time from track reconstruction. Moving the extraction of the aforementioned features to the readout FPGA would speed up the unpacking of the data and remove the computing time needed to reconstruct the encoded information.

To test the various components required for CBM, a small-scale version of the experiment called mCBM was constructed. However, even mCBM has reached a point where it is no longer possible to store the raw data produced by the TRD front-end ASIC on disk. Therefore, the mCBM experiment is an excellent opportunity to develop and test the implementation of feature extraction algorithms on the readout FPGA in a real-world scenario.

In this submission, I will present the encoding and feature extraction algorithms implemented using High-Level Synthesis (HLS) and the results obtained in mCBM beam tests. I will demonstrate how HLS simplifies the development of algorithms for high throughput applications and how C++ template programming can enhance the performance and reusability of HLS algorithms, using the SPADIC hit message decoder as an example. The algorithm for reconstructing the time shift from the signal shape will be discussed in detail, and results showing resolution improvements will be presented.

Further down the chain at the computing cluster, the implementation of the feature extraction algorithms on the FPGA, reduces the incoming data volume from the FPGA by over 50% and improves the unpacking speed by over 500%.

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