

# Optimized Rad-Hard DC/DC Converters for HEP Applications

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This R&D has been made possible thanks to the  
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# Introduction



On-detector DC-DC converters are utilized to minimize the losses in the distribution lines and reduce material requirements.

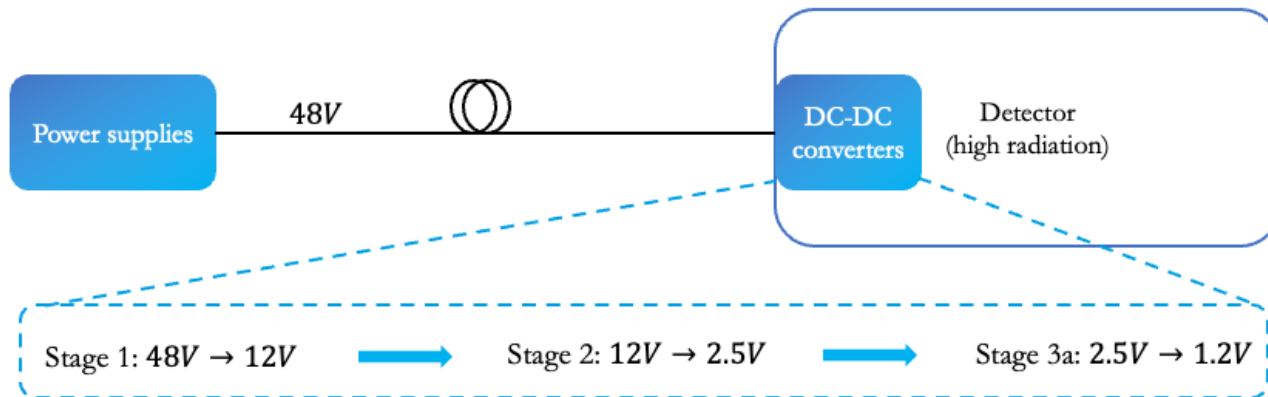
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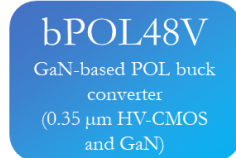
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Stage 1:  $V_{in} = 15 - 48V$



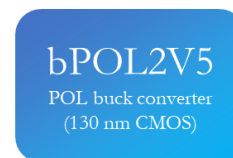
0.75 – 24V, 12A

Stage 2:  $V_{in} = 5.5 - 12V$



0.63 – 5V, 4A

Stage 3:  $V_{in} = 2.1 - 2.5V$



0.6 – 1.5V, 3A

# Introduction



Development of novel and efficient powering schemes:

- Increasing power demand
- Reduction in size and weight of cabling, power supplies and cooling

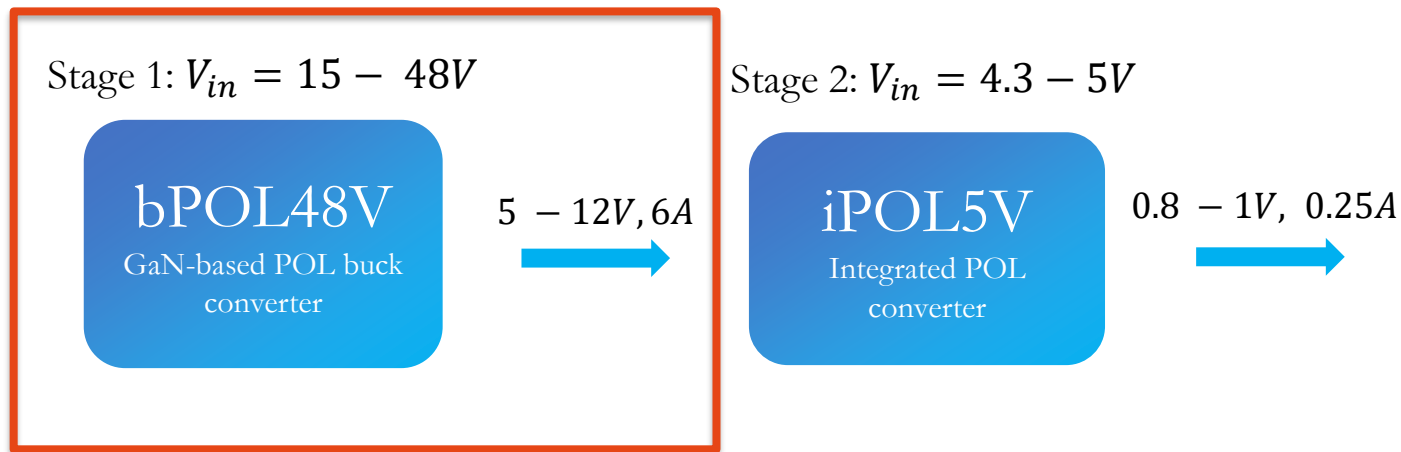
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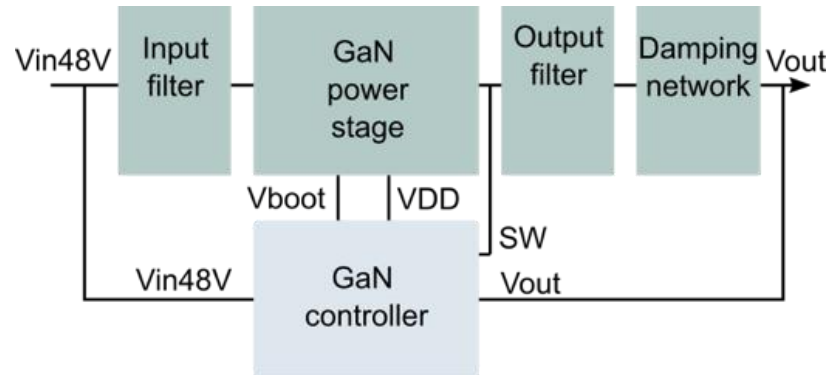


Focus of this presentation

# bPOL48V

bPOL48V:

- GaN\_Controller: Custom CERN ASIC
- EPC2152: Integrated GaN power stage
- Input filter
- Output filter



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# Preceding bPOL48V Design

High-Current Module:

- Input voltage: 48 V
- Output voltage: 12 V
- Output current: 12 A
- Volume: 56899 mm<sup>2</sup>



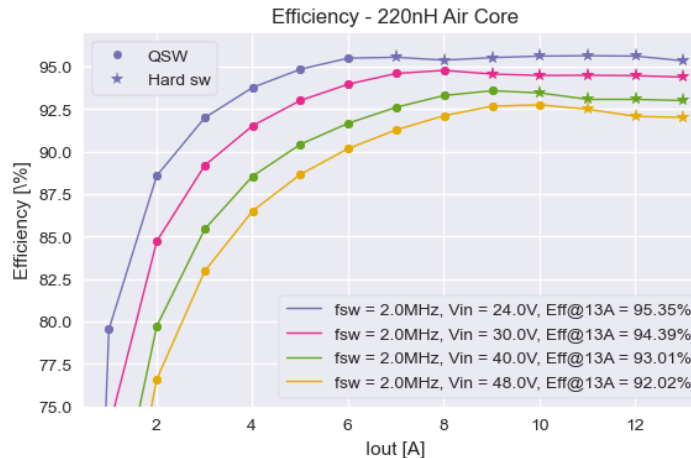
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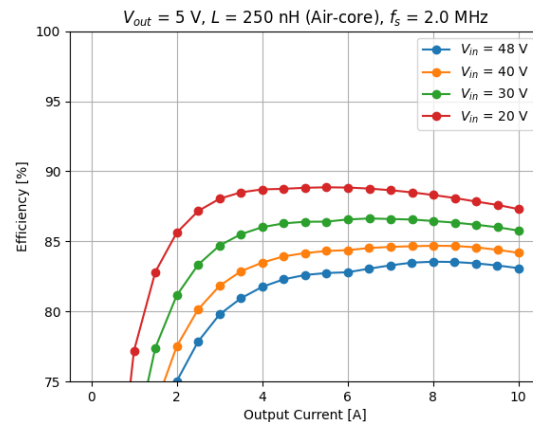
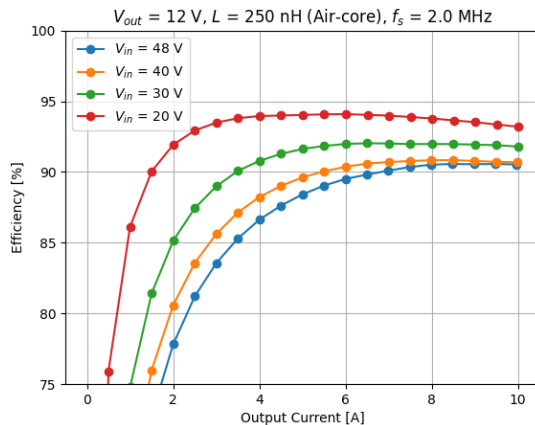
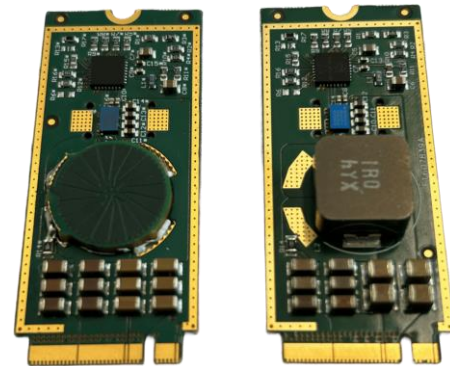


# Compact bPOL48V Module



High-Current Module:

- Input voltage: 48 V
- Output voltage: 5 - 12 V
- Output current: 10 A
- Volume: 3960 mm<sup>2</sup>



Available for purchase and as reference design!

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# Optimization Framework



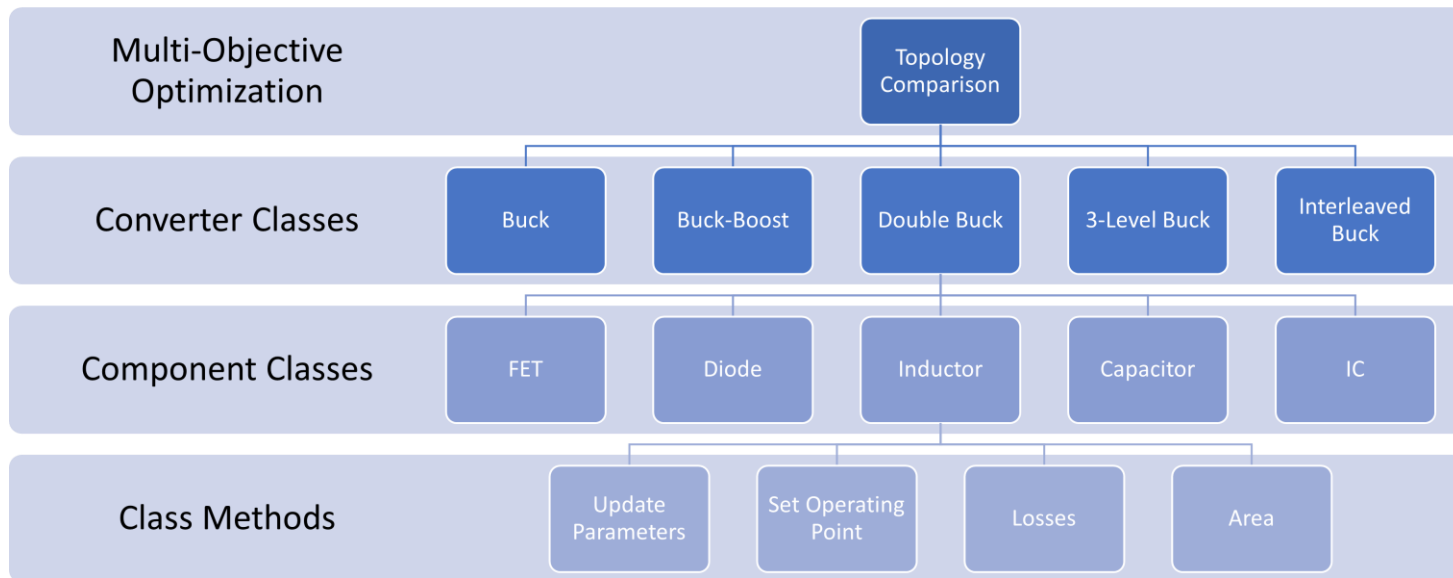
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# Optimization Framework



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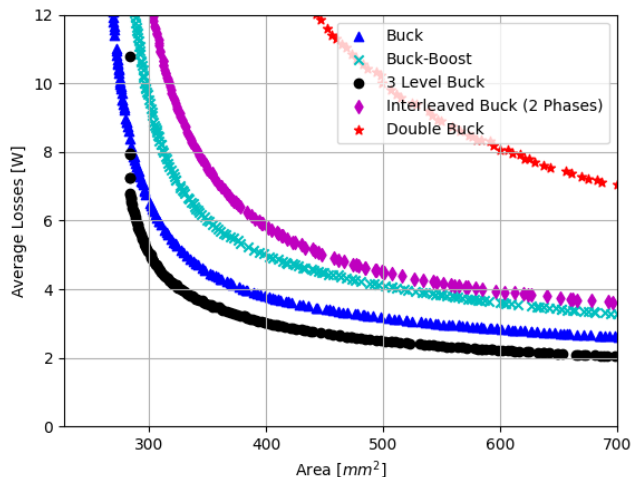
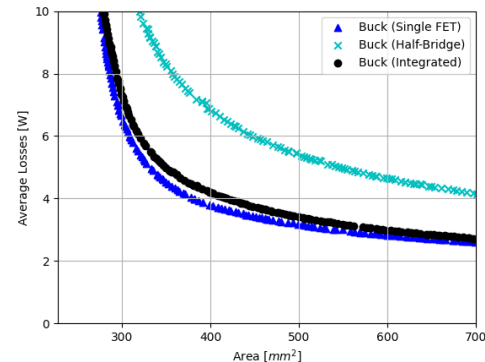
- Component classes: FET, Diodes, Diodes, Capacitors, ICs
  - Attributes: Parameters, operating conditions
  - Methods: Losses, occupied area
- Converter classes:
  - Attributes: Input voltage, output voltage, output power
  - Methods: Operating conditions, sizing capacitors
- Multi-Objective Optimization:
  - Input variables: Devices, switching frequency, inductance, capacitance
  - Minimization: Losses, occupied area (pareto front)

# Optimization Framework: Results



## High-Current Module:

- Input voltage: 48 V
- Output voltage: 5 V
- Output current: 10 A
- Voltage ripple: 1%



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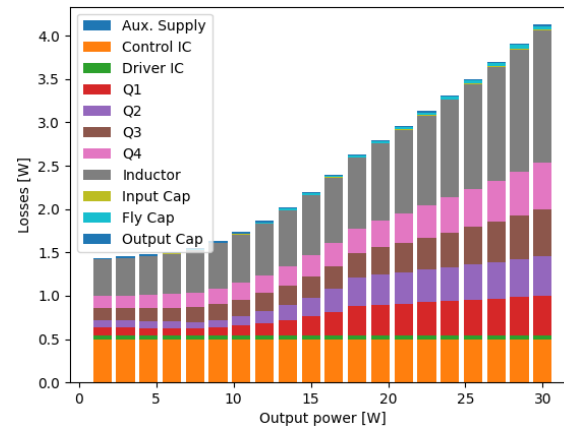
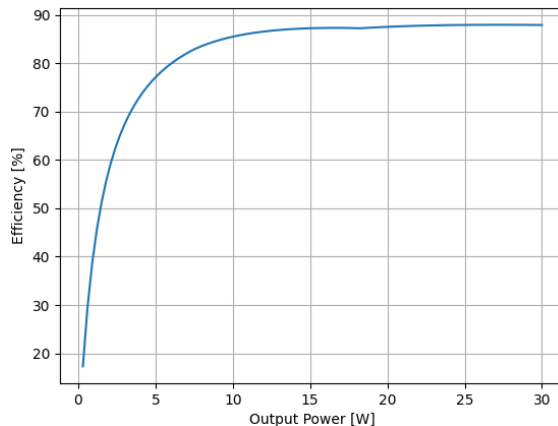
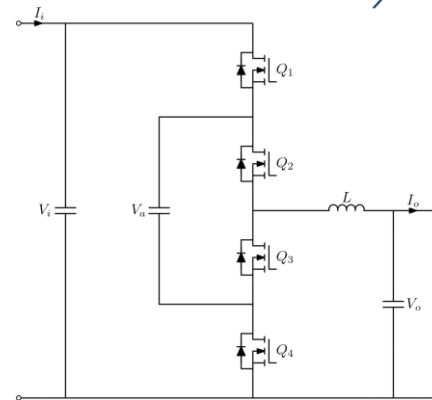
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# Optimization Framework: 3-Level



- $f_s = 1.3 \text{ MHz}$
- $L = 211 \text{ nH}$
- Area = 225 mm<sup>2</sup>
- High side: EPC2214
- Low Side: EPC7002



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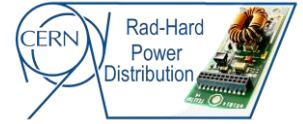
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# Experimental Verification: Topologies



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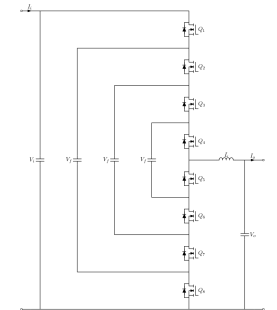
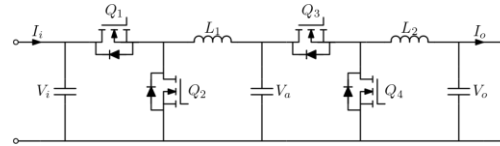
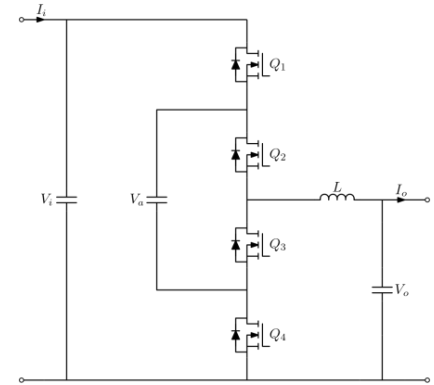
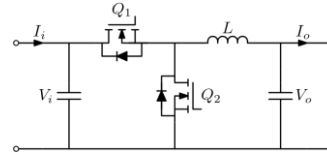
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- Buck
- 3-Level Buck
- Double Buck
- 5-Level Buck



# Experimental Verification: Prototypes

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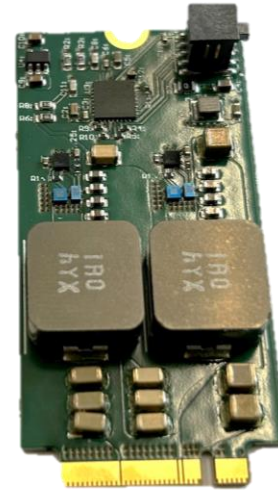
**Experimental**

Conclusions

Buck



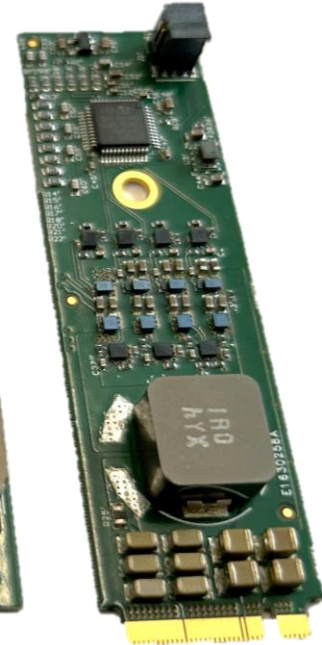
Double Buck



3-Level Buck

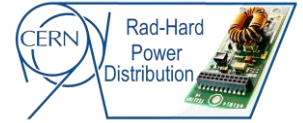


5-Level Buck



All prototypes are designed with an STM32 microcontroller, commercial GaN switches, and commercial drivers.

# Experimental Verification: Results



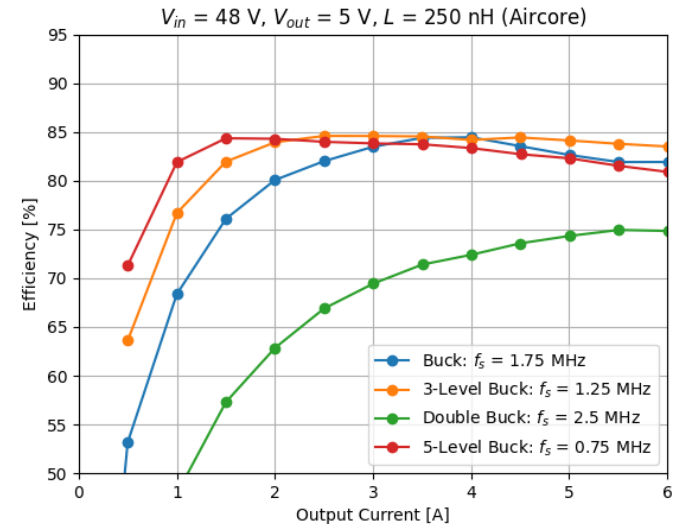
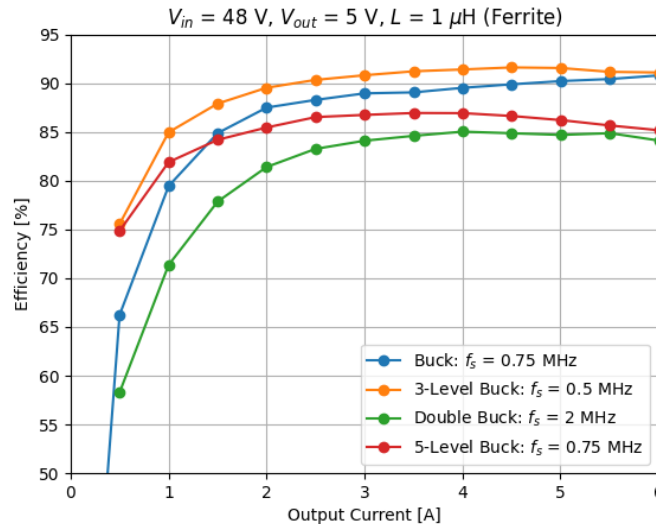
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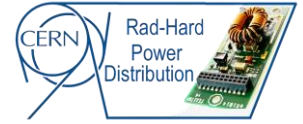
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Each prototype's switching frequency was individually optimized.

# Experimental Verification: 48 V to 1 V



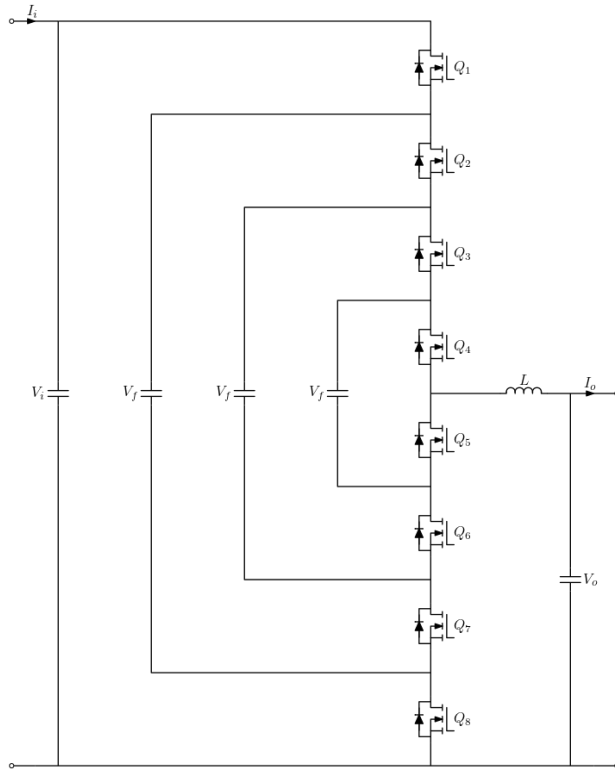
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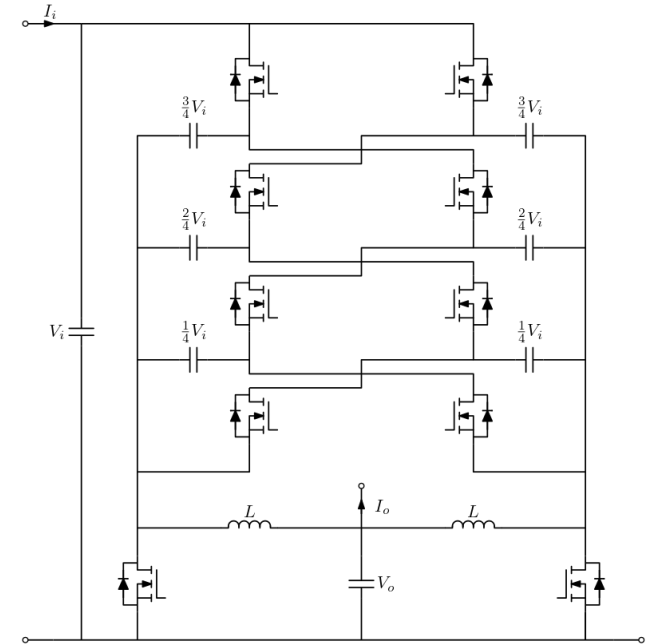
Optimization

**Experimental**

Conclusions



5-Level Buck



Berkeley Buck

# Experimental Verification: 48 V to 1 V



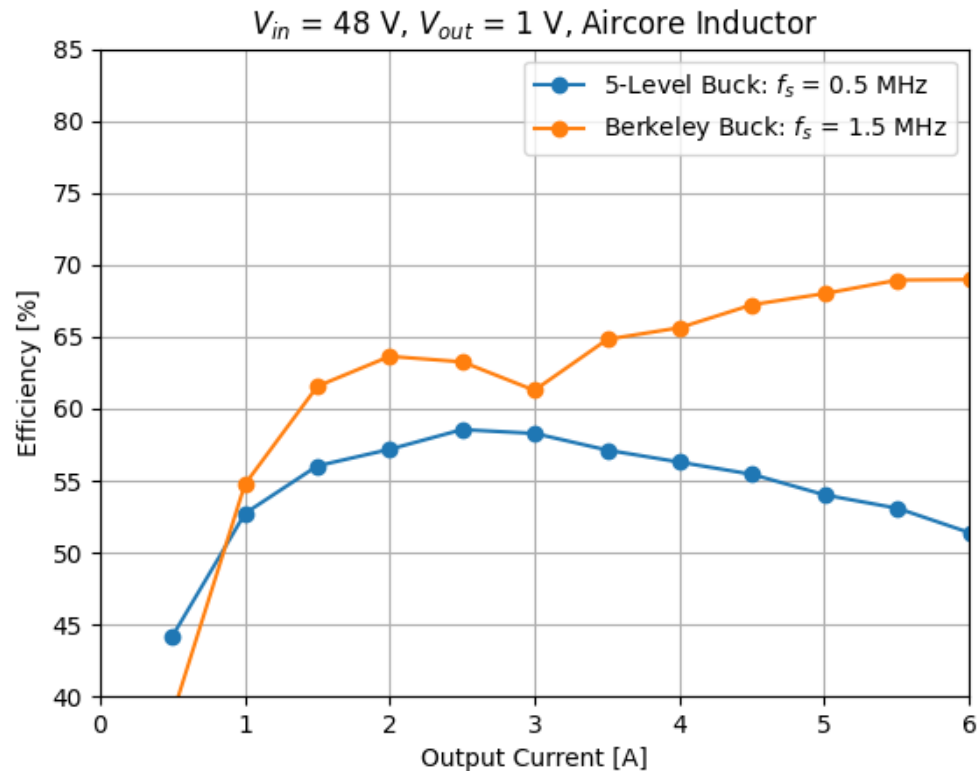
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Very preliminary results!



# Conclusions



- Two volume optimized bPOL48V module were presented
  - PCB Inductor Module: Up to 95% efficiency in 3960 mm<sup>2</sup>
  - Ferromagnetic Module: Up to 97% efficiency in 9240 mm<sup>2</sup>
  - Available for purchase or as reference design
- An optimization framework was developed
  - Multi-objective minimization of losses and area
  - Comparison of power electronic conversion topologies
- Prototypes were built and tested
  - 3-Level Buck converters show promise from 48 V to 5 V
  - Berkeley Buck converters show promise from 48 V to 1V

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