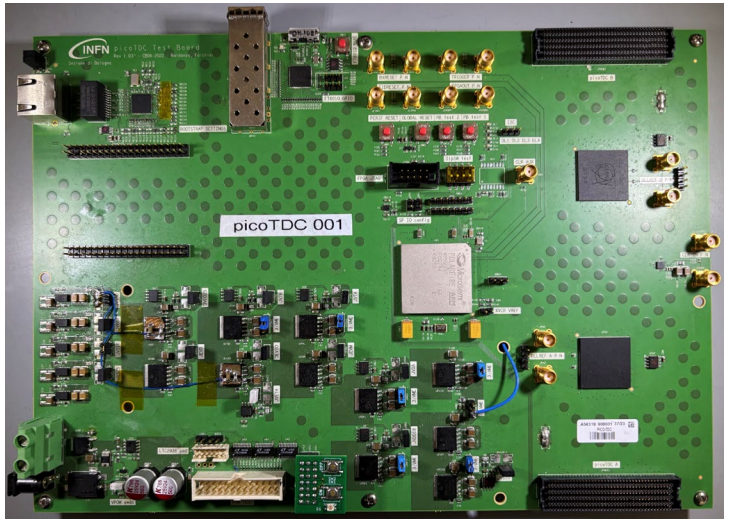
Design, test and performance of a picoTDC based board

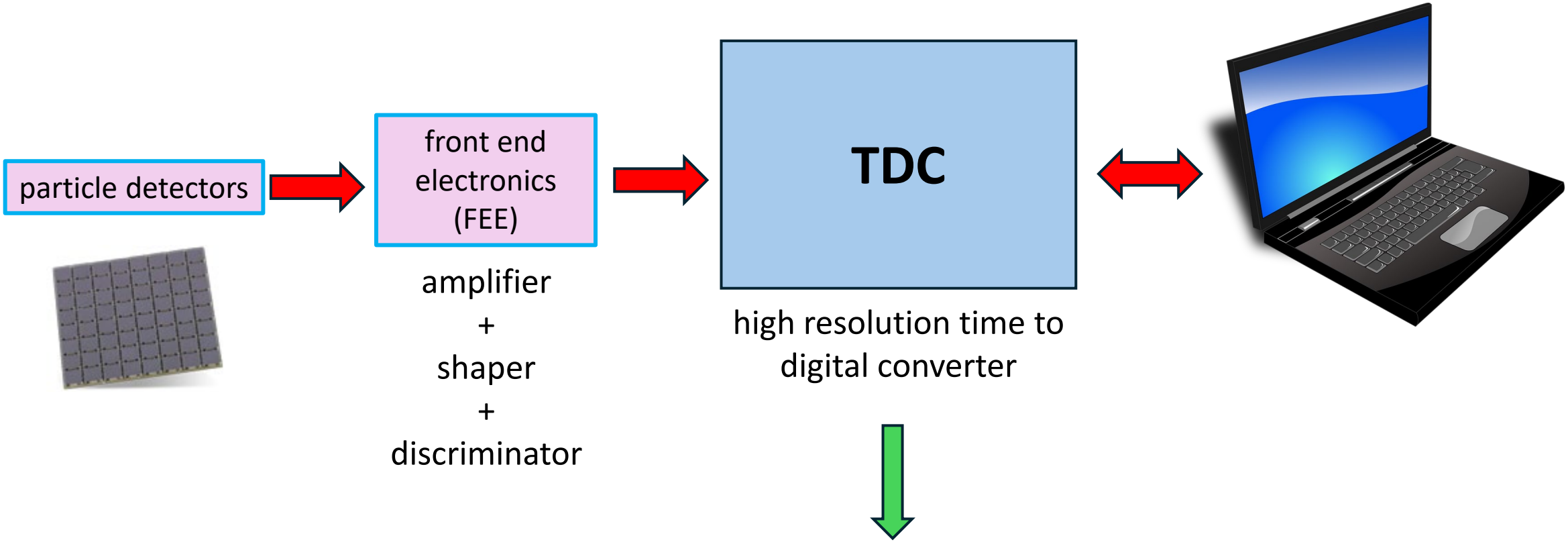
Davide Falchieri [a], Pietro Antonioli [a], Casimiro Baldanza [a], Daniele Cavazza [a], Sandro Geminiani [ab], Marco Giacalone [a], Jacopo Succi [ab], Carlo Veri [c]

INFN Bologna [a], University of Bologna [b], INFN Lecce [c]



TWEPP 2024, Glasgow, 30 September - 4 October 2024

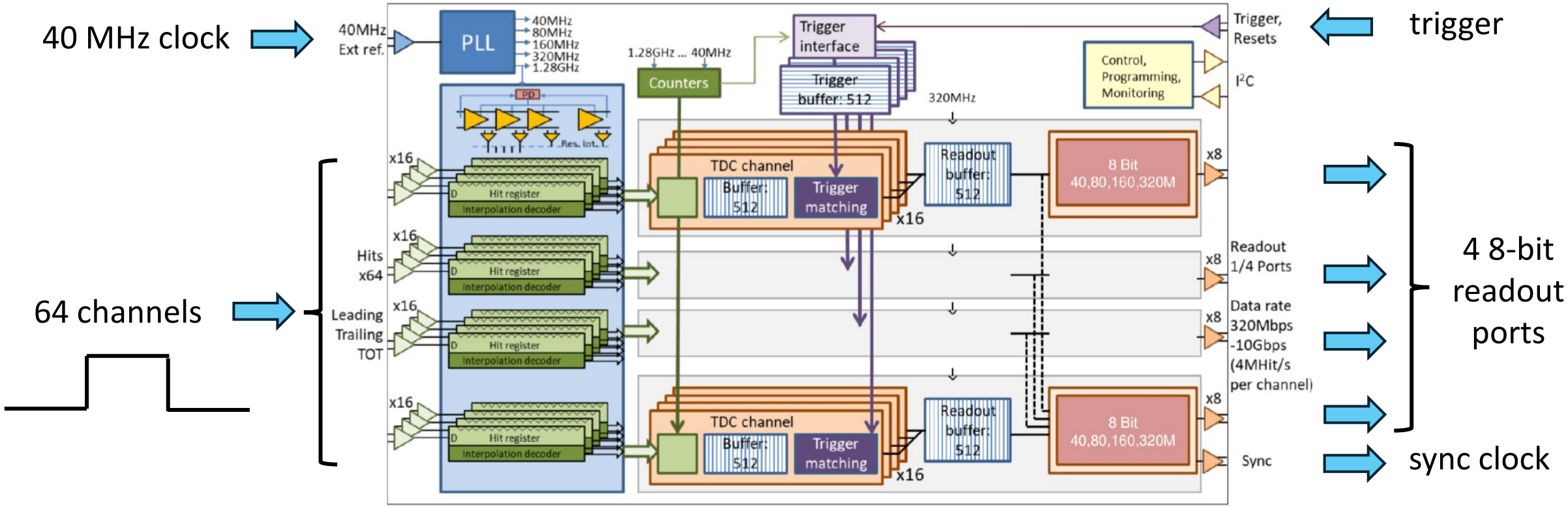
Towards a flexible timing measurement device

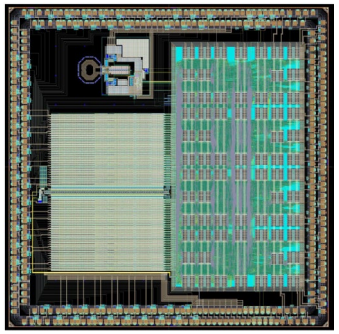


Our goal was to build **a flexible high resolution timing measurement device** able to:

- connect to multiple detector types + FEE with standard connectors
- provide high data bandwidth towards a PC via standard interfaces (Ethernet + USB3)
- provide the best achievable timing resolution on a lot of channels (128)

The picoTDC ASIC from CERN

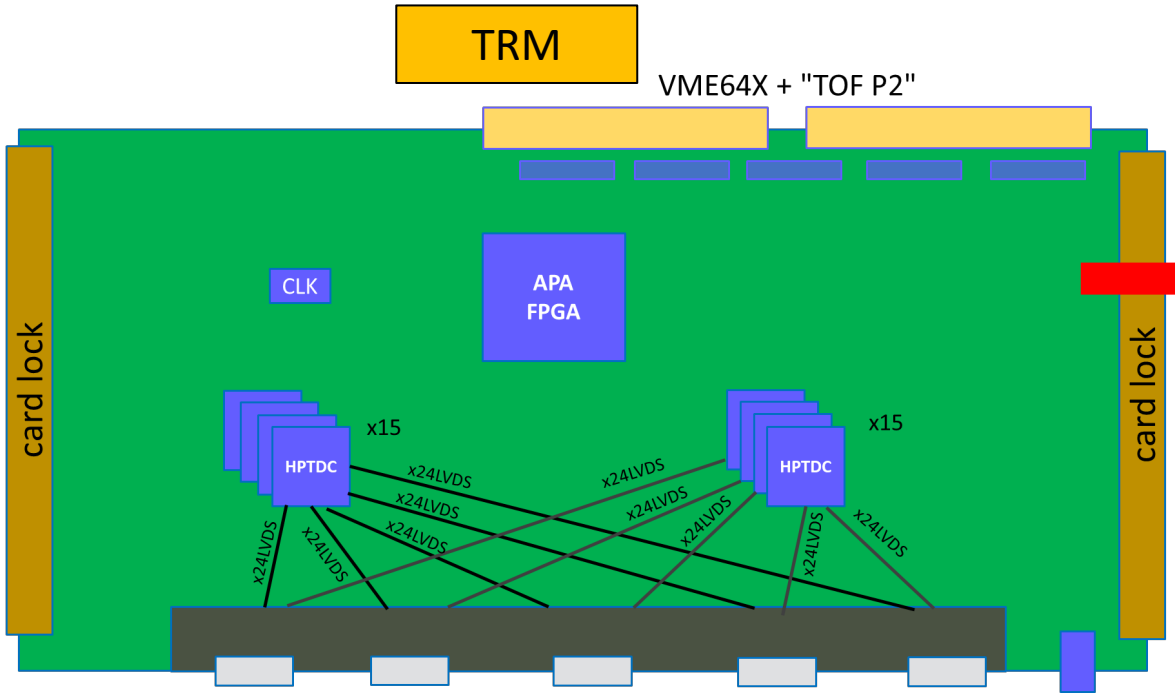


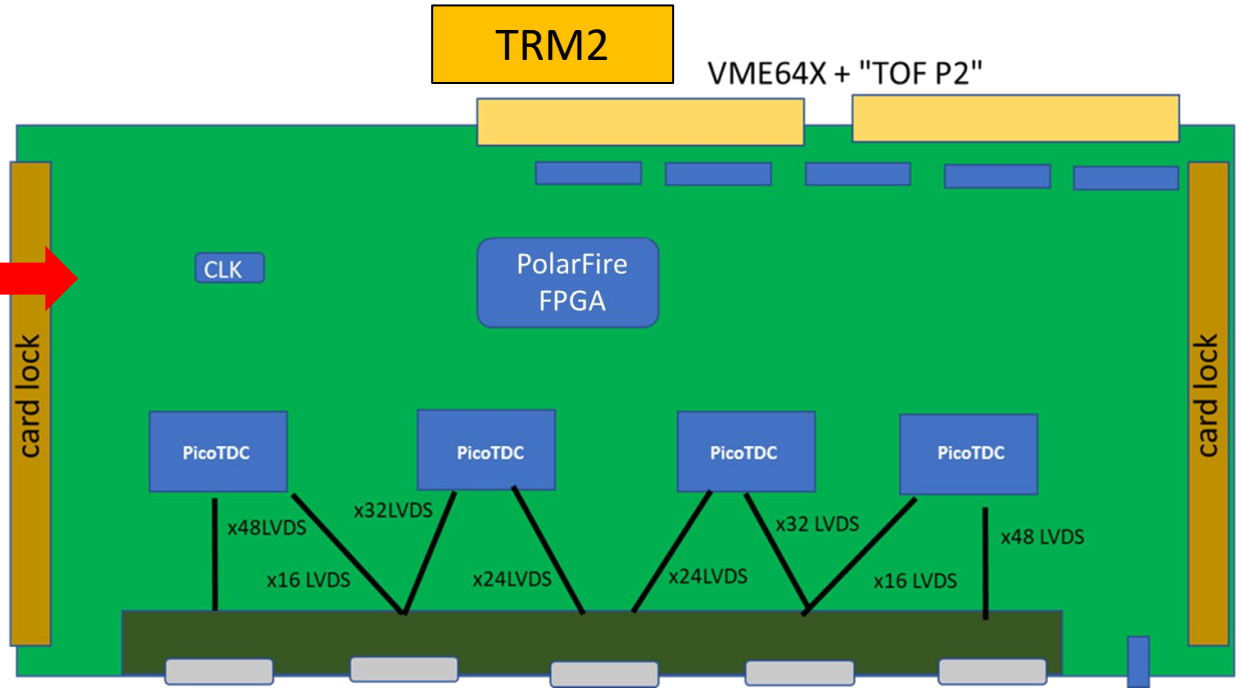


picoTDC main features:

- bin size: 3.05 ps (fine resolution) or 12.2 ps (coarse resolution)
- single shot resolution: <3.3 ps in fine mode or <4.2 ps in coarse mode
- measurement range: 204.8 μs
- measurement scheme: triggered or un-triggered time-tagging

From TRM to TRM2 for time measurements in ALICE TOF detector





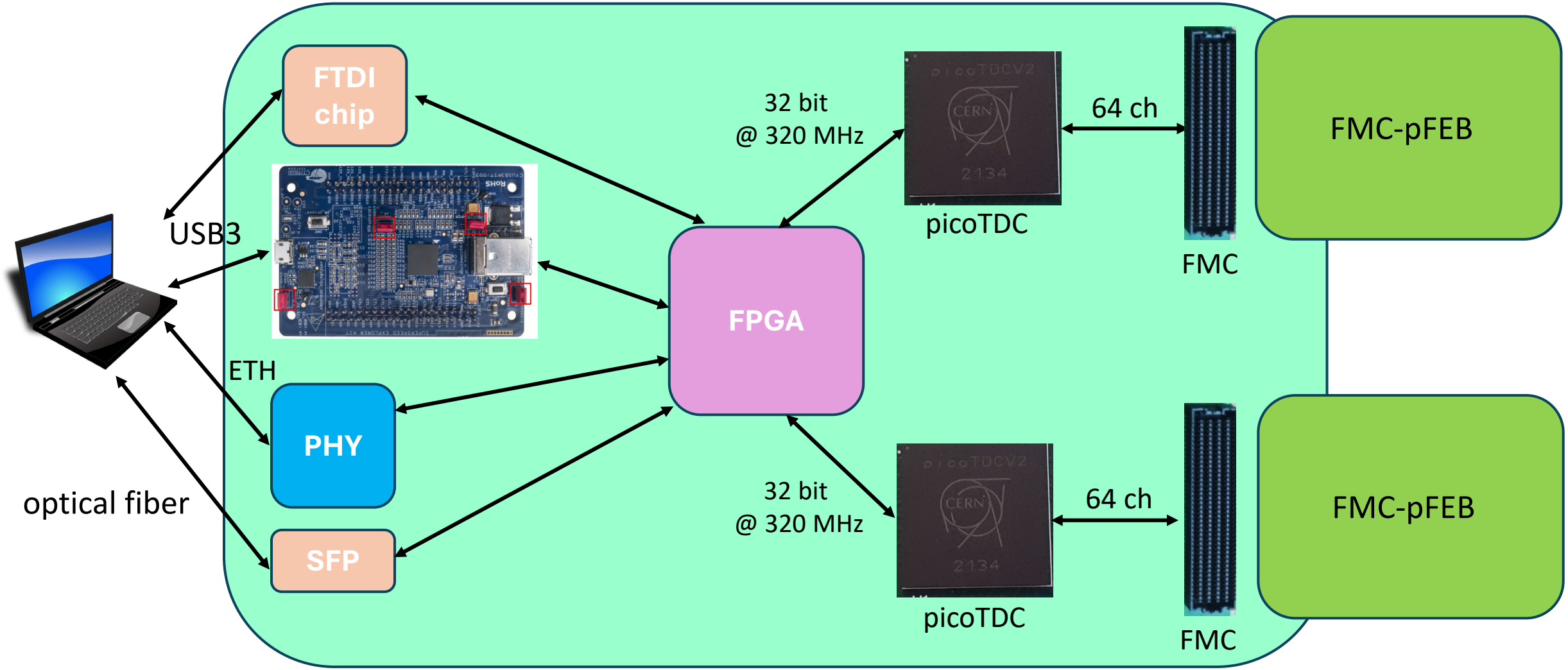
The **TRM VME** card is the main element of the TOF readout system and it hosts:

- an **Actel ProASIC FPGA** to manage the readout and board operations.
- **30 HPTDC** ASICs (24.4 ps LSB, 8 ch/chip) to provide time measurements.

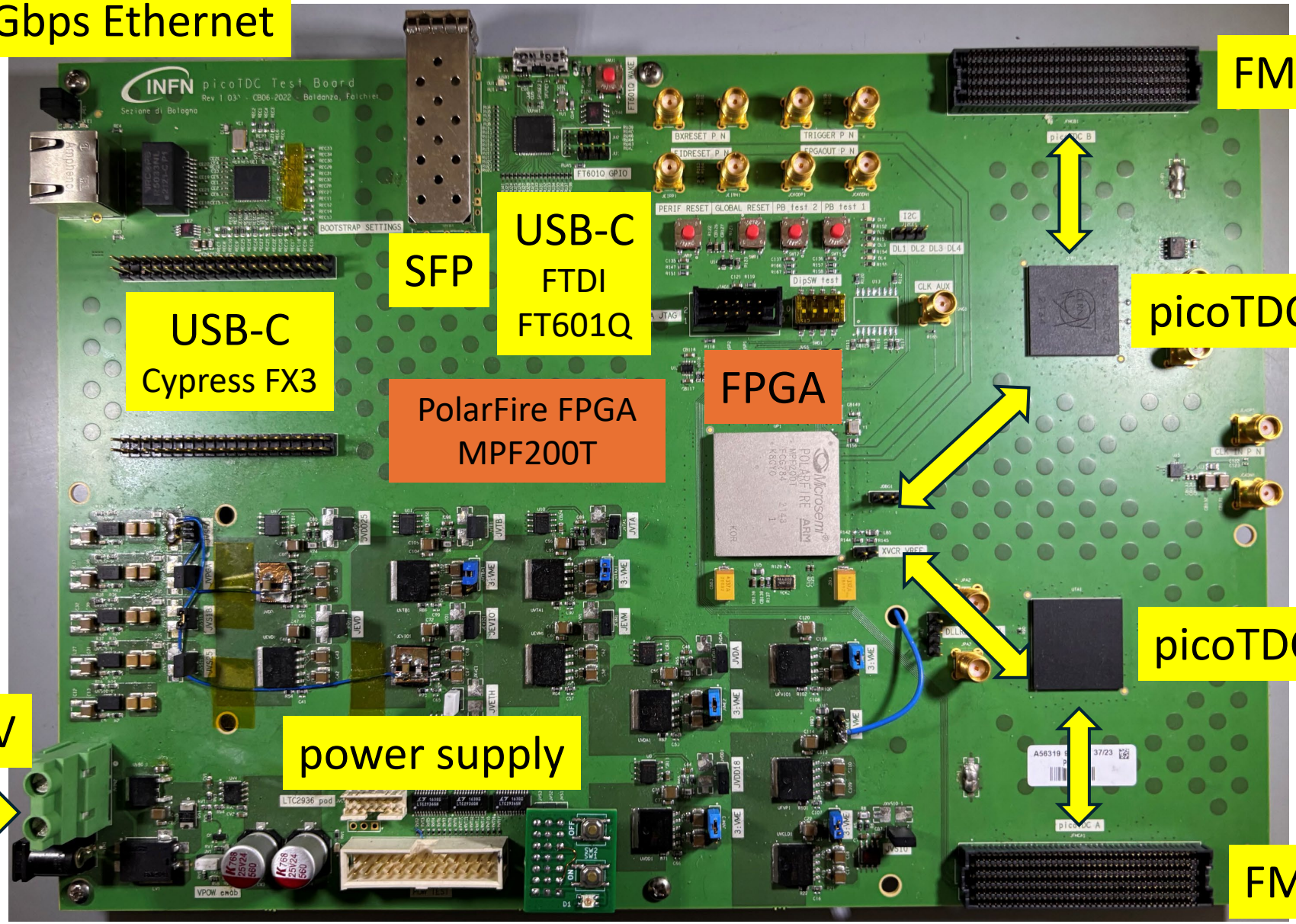
To replace damaged TRMs during LHC Run 4, a new **TRM2** project began, considering:

- **a PolarFire FPGA** to manage the readout and board operations.
- **4 PicoTDC** ASICs (12.2 ps or 3.05 ps LSB, 64 ch/chip) as successors of the HPTDCs.

Towards the picoTDC board



The picoTDC board



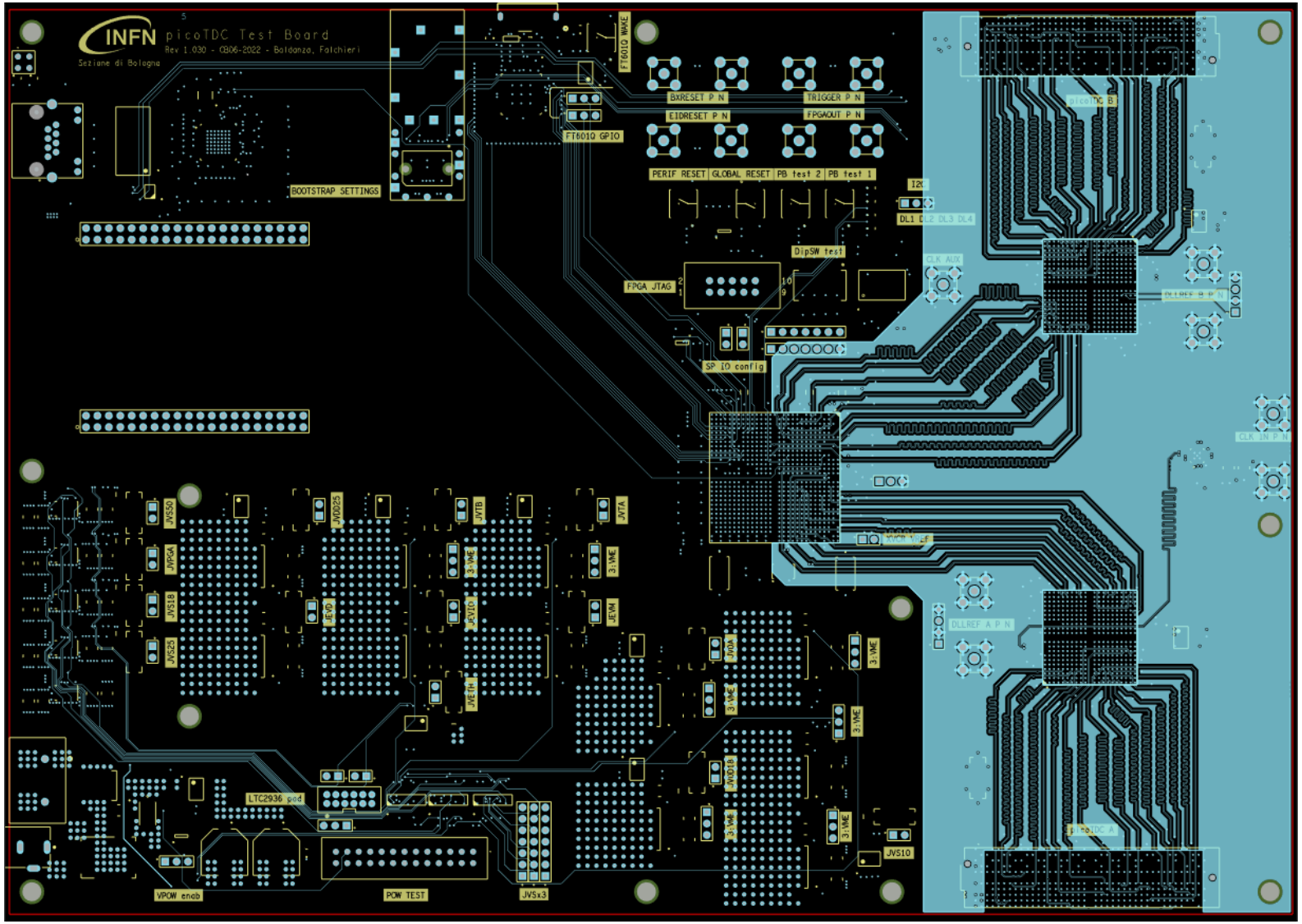
standard FMC HPC

table-top board (20 x 15 cm) to be used in conjunction with pFEBs

15 SMA I/Os, among which an option reference external clock

standard FMC HPC

The picoTDC board (layout)

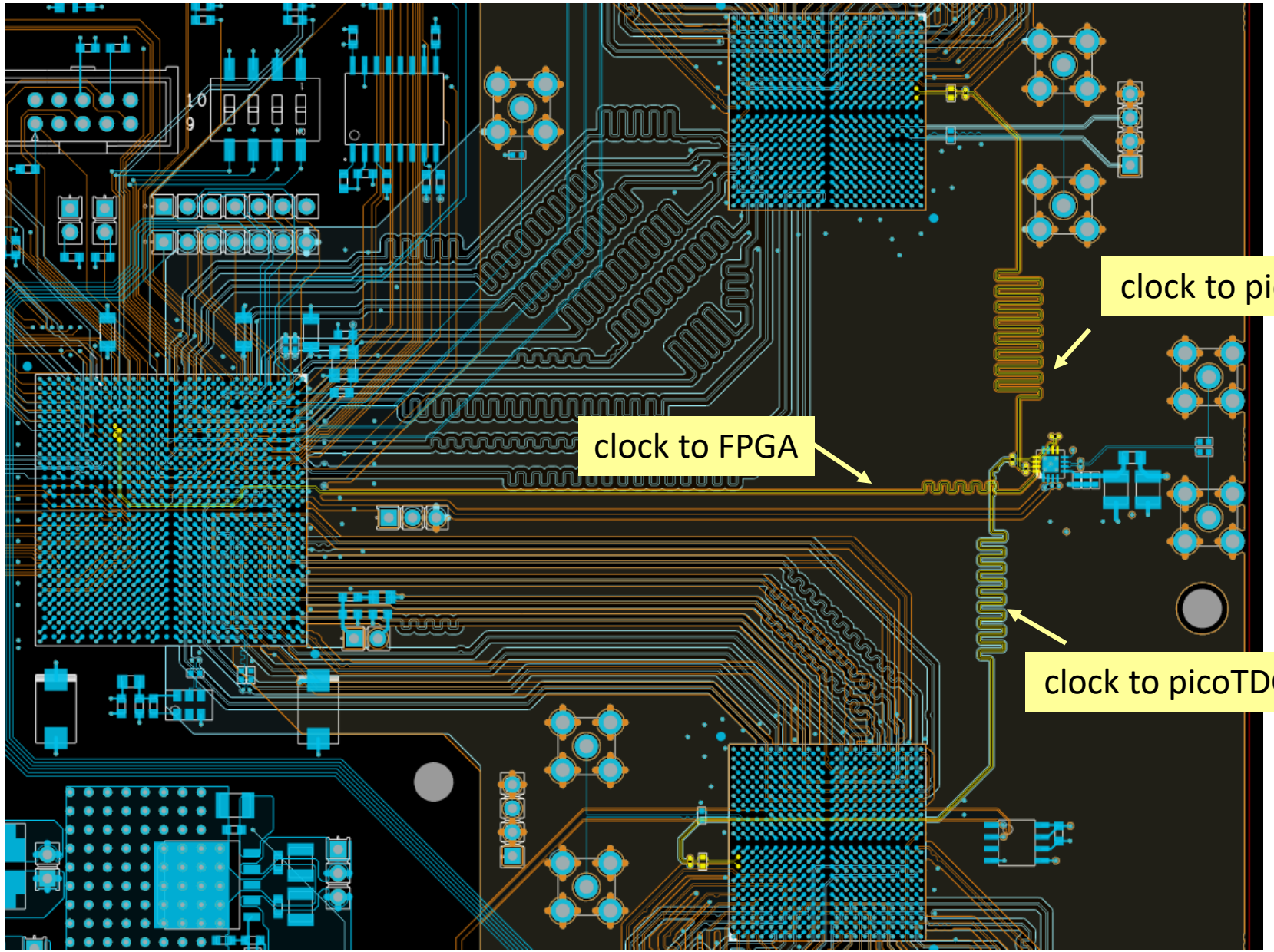


dieletric: FR-408, PREPREG_58
total thickness: 1.6 mm

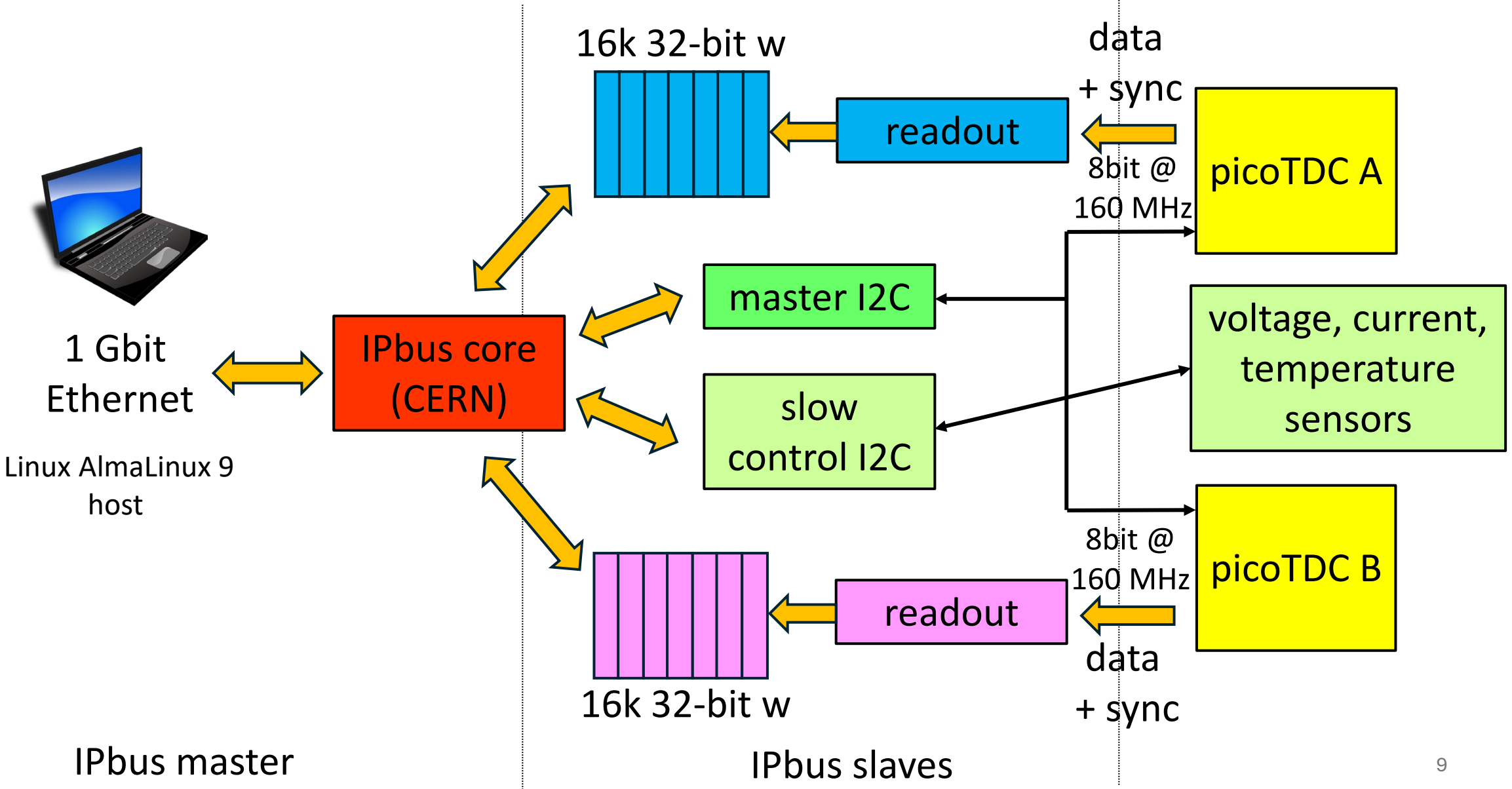
differential lines and equalization
PCB stackup, 14 layers

The picoTDC board (layout)

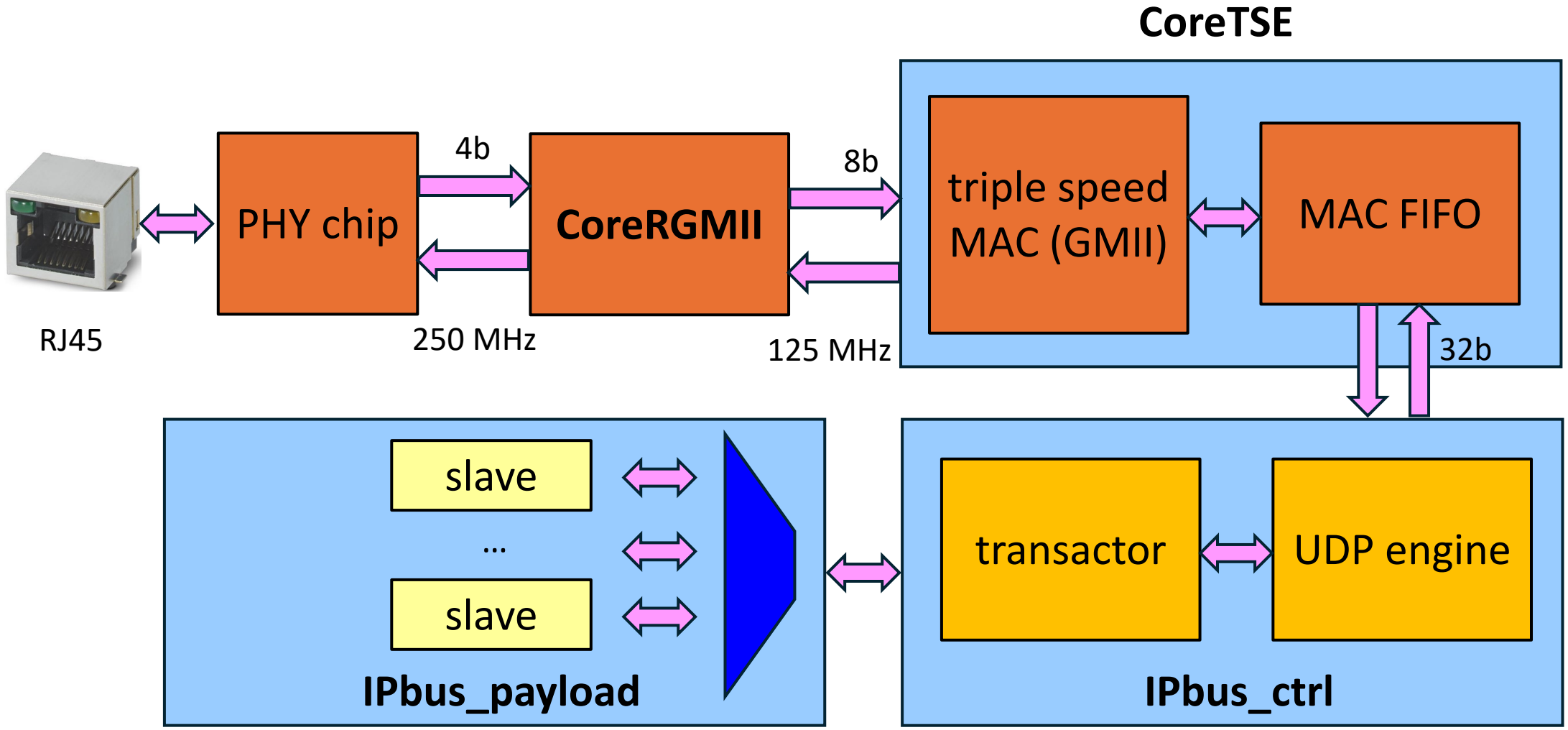
the 3 clock tracks are equalized



PolarFire FPGA firmware



PolarFire FPGA firmware: IPbus core implementation



We used the Microchip IP cores (CoreRGMII and CoreTSE) towards a first implementation of CERN IPbus core over a Microchip FPGA

picoTDC board software

The **user interface** is designed to hide the system complexity and works through **prompt line commands.** It provides **two main user programs:**

3-layer software structure (C++)

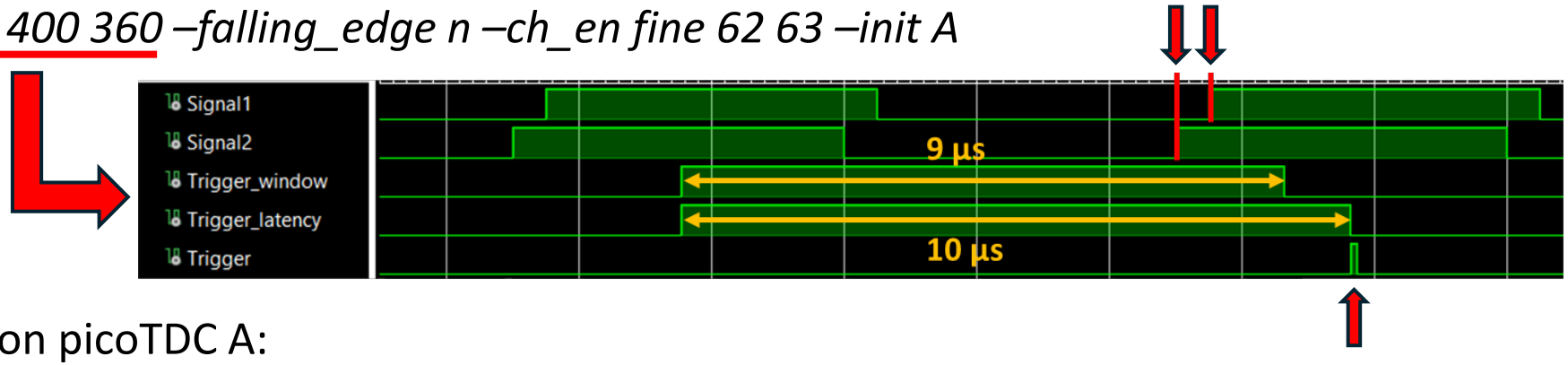
- user main programs
- C++ classes → IPbus slaves
- IPbus API library

PicoTOF — user program to configure both the picoTDCs

PicoRead — user program for reading out data from the picoTDC chips, considering a **trigger-based** readout

Configuration for triggered mode with channels 62-63 on picoTDC A:

*$ ./**PicoTOF** –triggered –lw 400 360 –falling_edge n –ch_en fine 62 63 –init A*

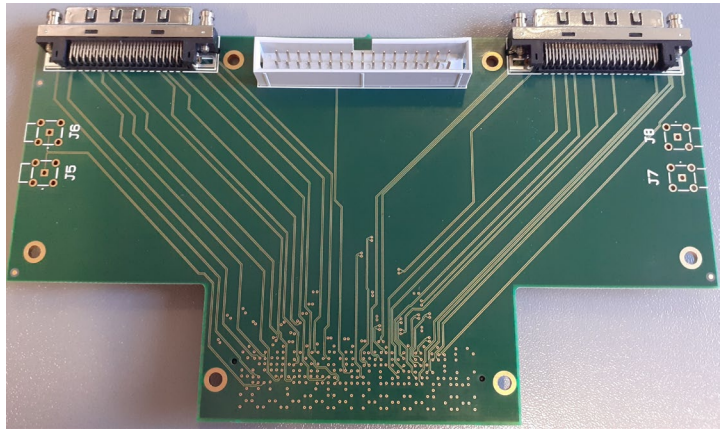


Acquisition of 10M events on picoTDC A:

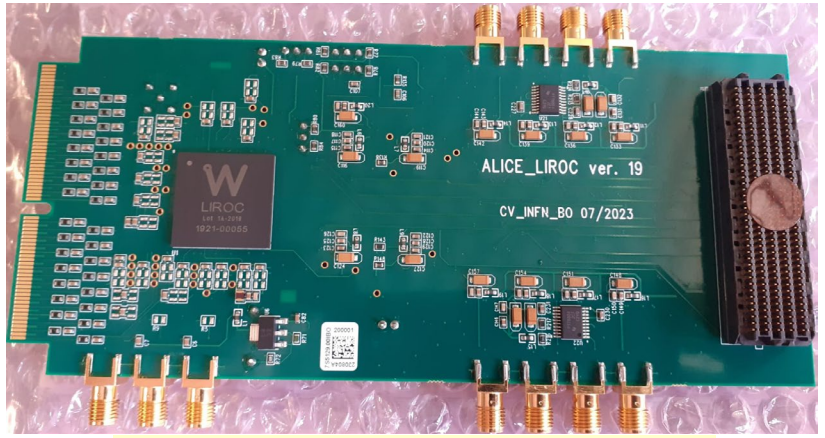
*$ ./**PicoRead** –chip A –events 10000000 –output file.ptdat*

Towards a family of pFEBs

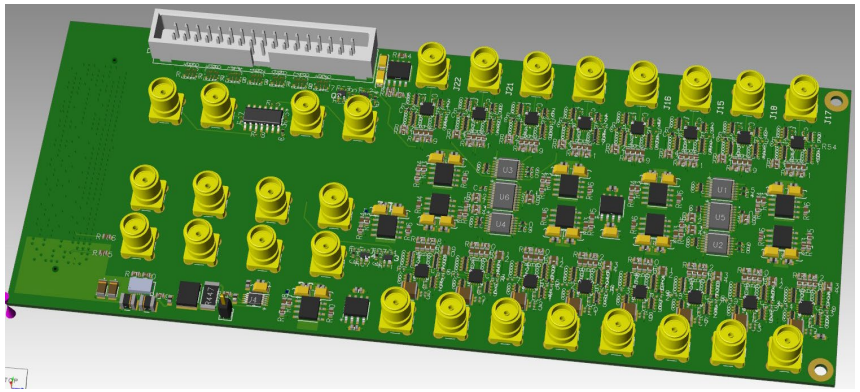
pFEBs



picoTDC breakout board



picoTDC LIROC board



pFEB-D board

We designed a family of custom picoTDC board – compatible mezzanines to provide connection towards detectors and their front-end electronics

A family of picoTDC compatible Front-End Boards (1)

from ALICE TOF MPRCs front -end

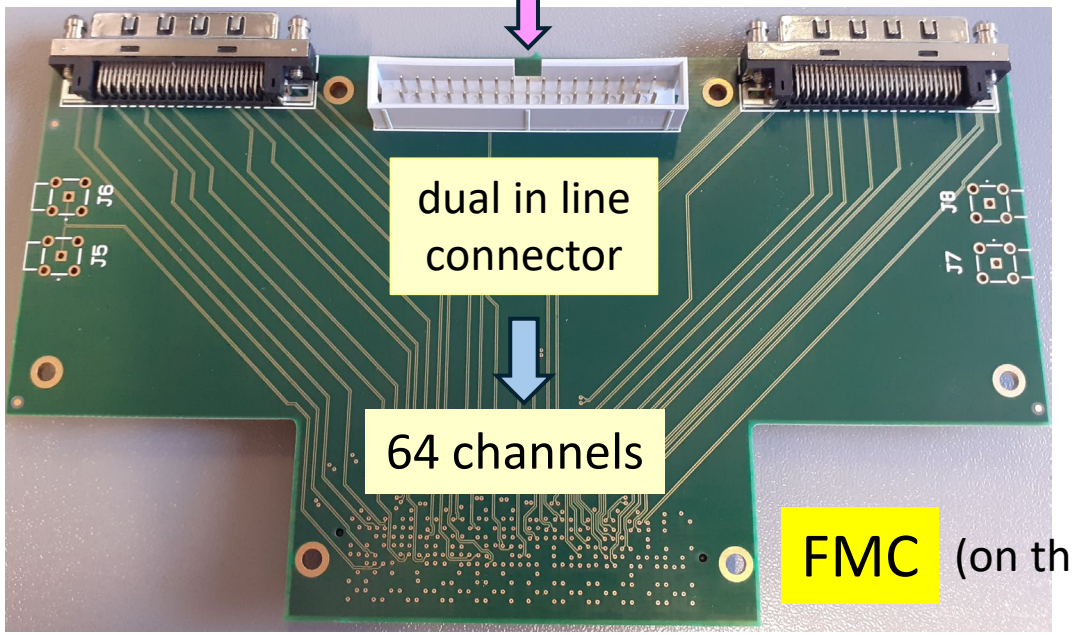
24 diff channels

24 diff channels

14 diff channels

VHDCI connector

VHDCI connector



2 MCx connectors

dual in line connector

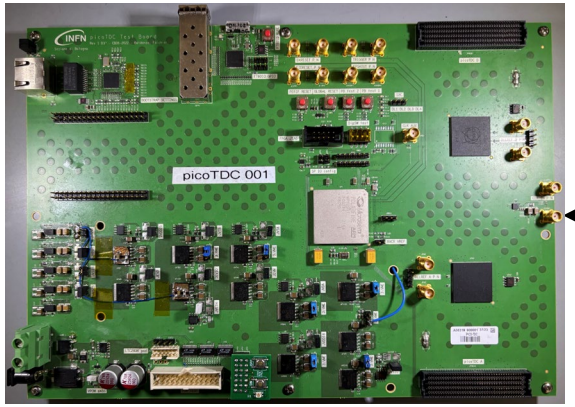
2 MCx connectors

64 channels

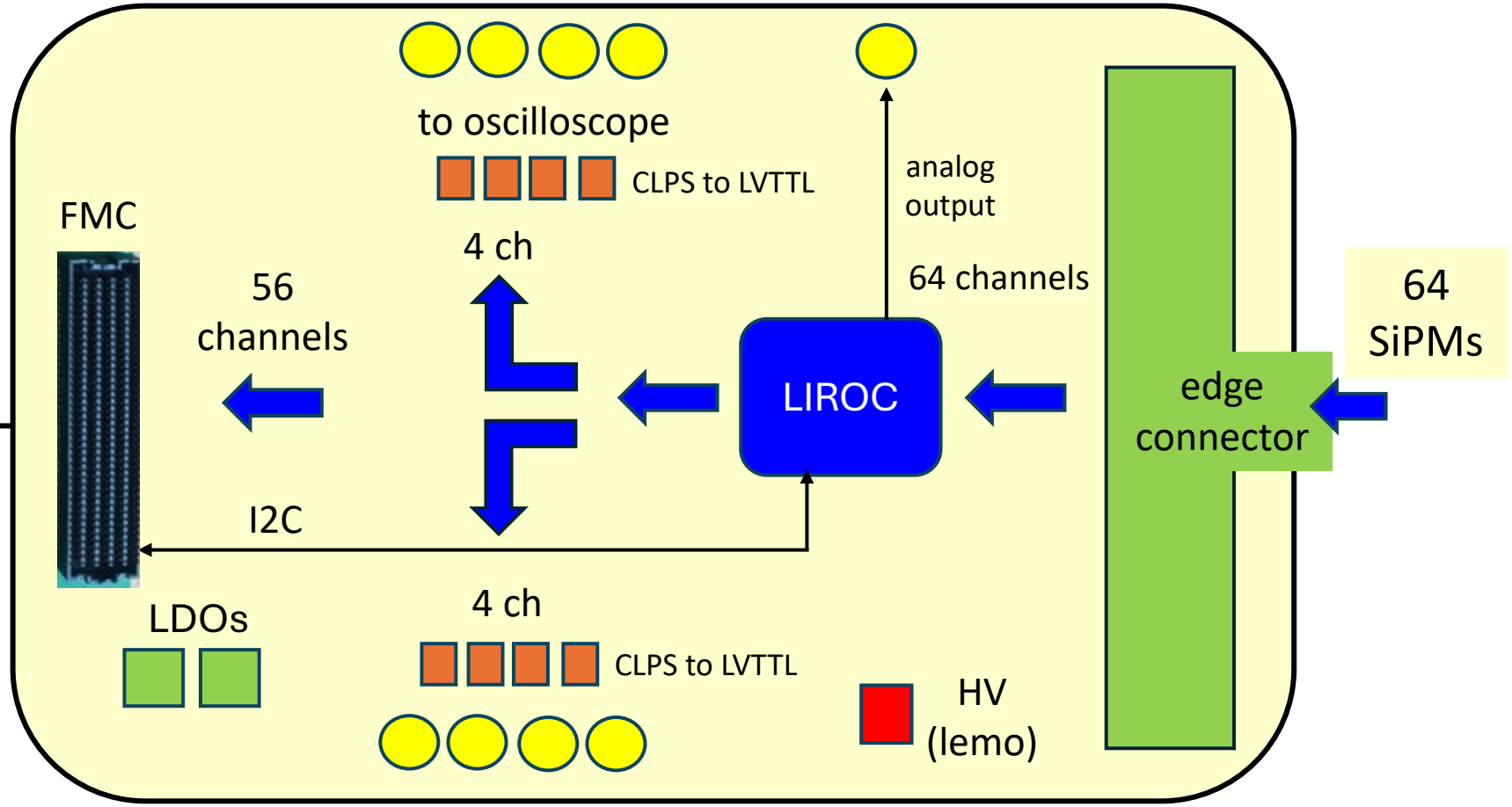
FMC (on the bottom side)

picoTDC breakout board

A family of picoTDC compatible Front-End Boards (2)

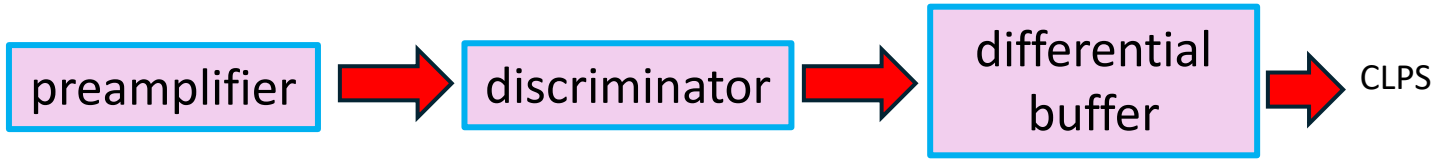


to picoTDC board



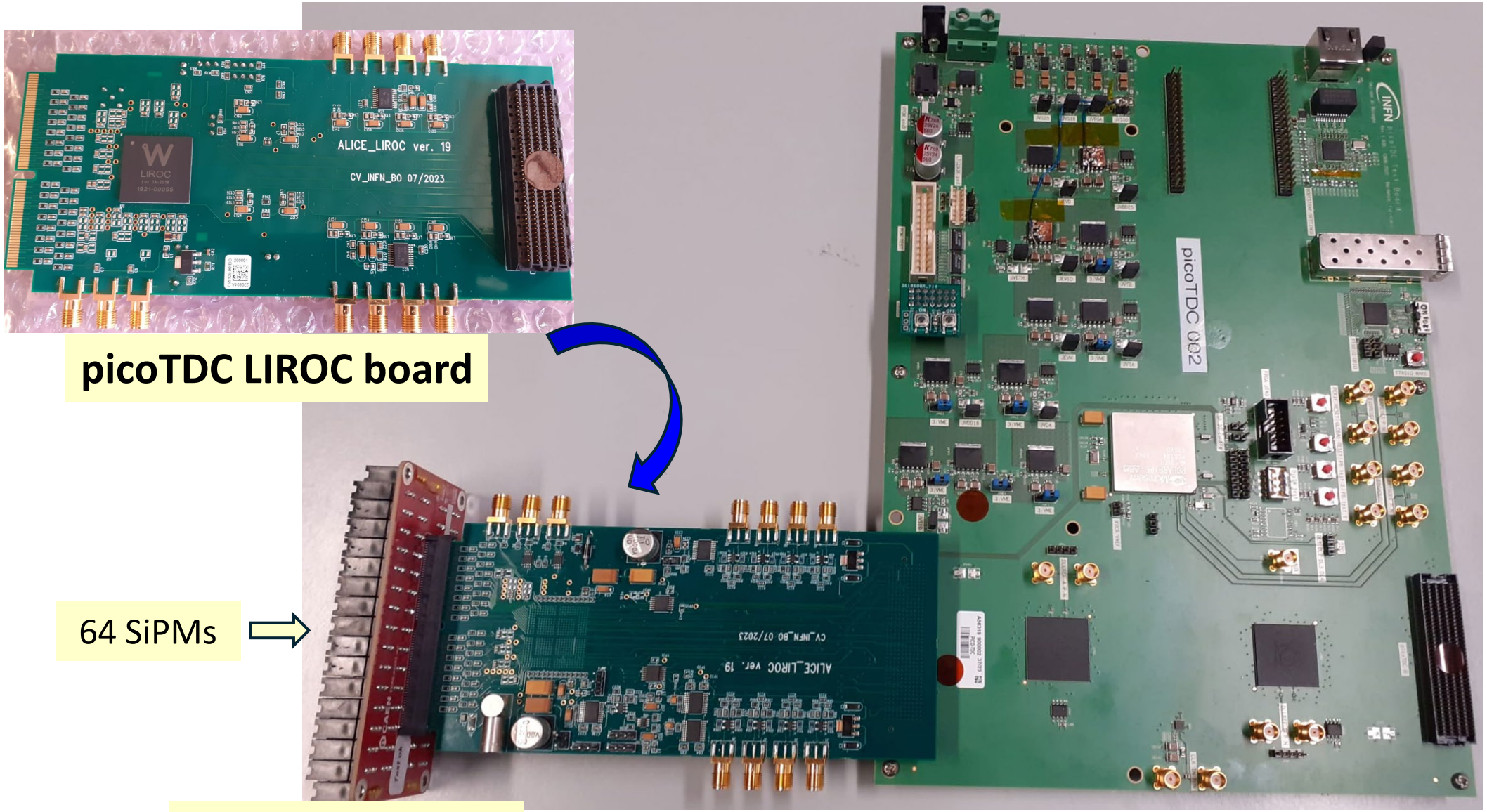
LIROC (from Weeroc) is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for LIDAR application

https://www.weeroc.com/products/sipm-read-out/liroc



timing resolution (better than 20ps FWHM)

A family of picoTDC compatible Front-End Boards (2)

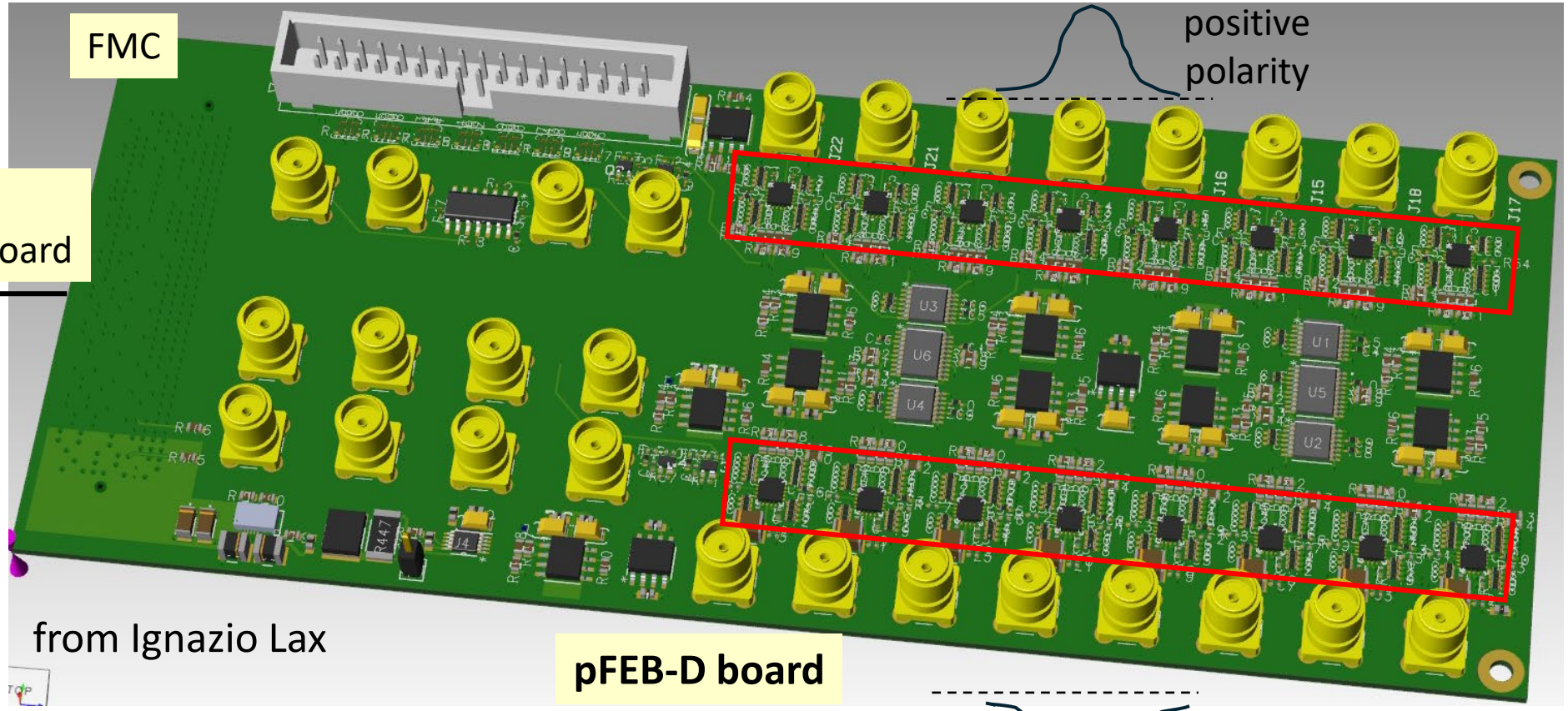


picoTDC LIROC board

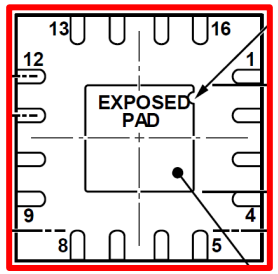
64 SiPMs

CAEN adapter board

A family of picoTDC compatible Front-End Boards (3)



ADCMP573



ultrafast SiGe discriminator

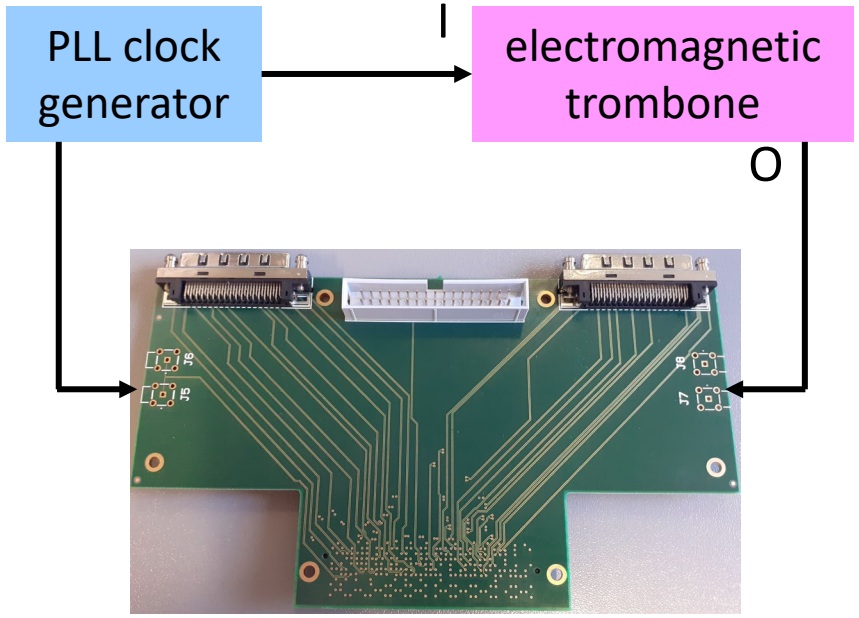
propagation delay error < 15 ps

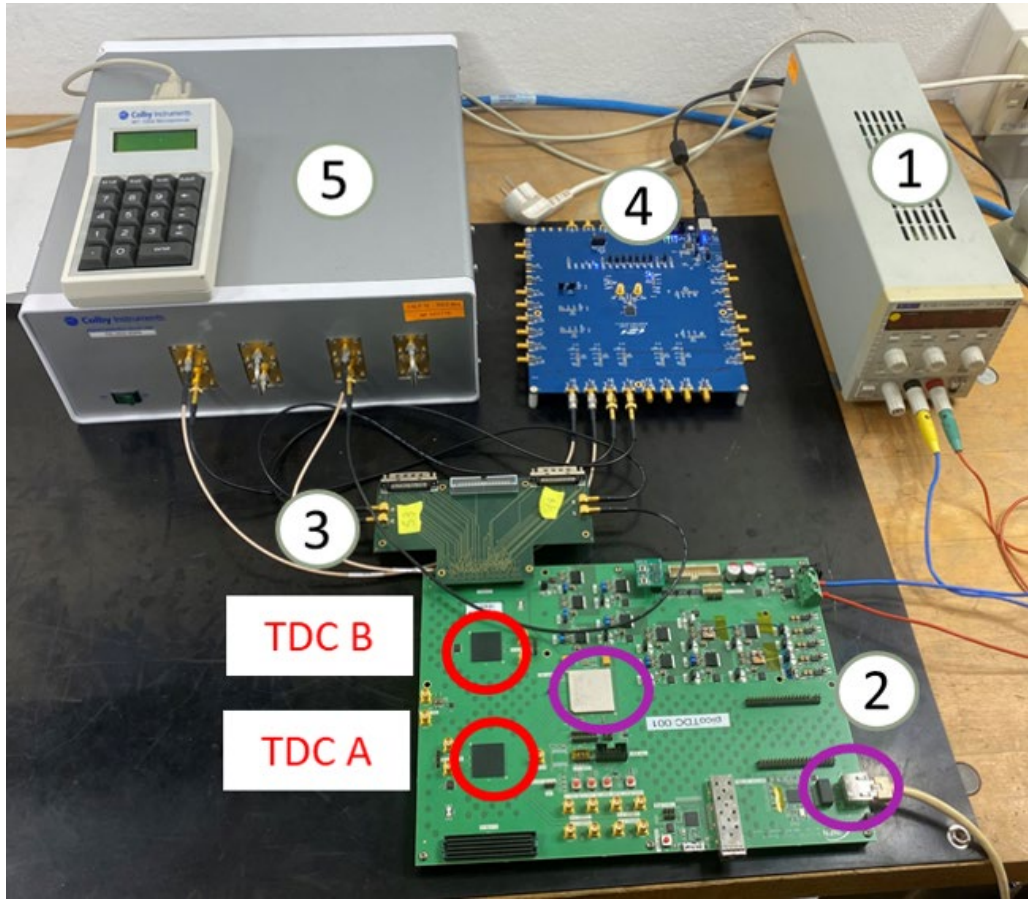
- 8 positive polarity inputs to discriminators
- 8 negative polarity inputs to discriminators
- 4 LVDS inputs (SMAs)
- 16 LVDS inputs (dual in line connector)

→ 36 channels

https://www.analog.com/en/products/adcmp573.html

TDC resolution measurements



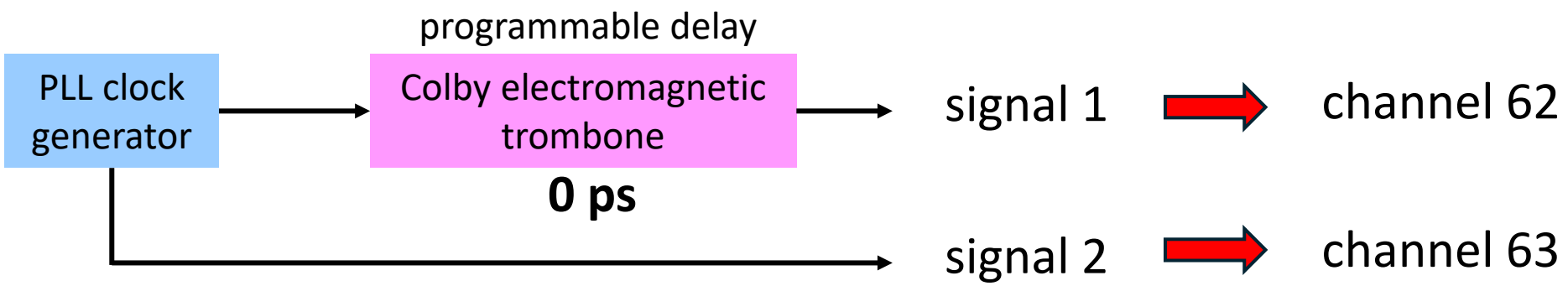


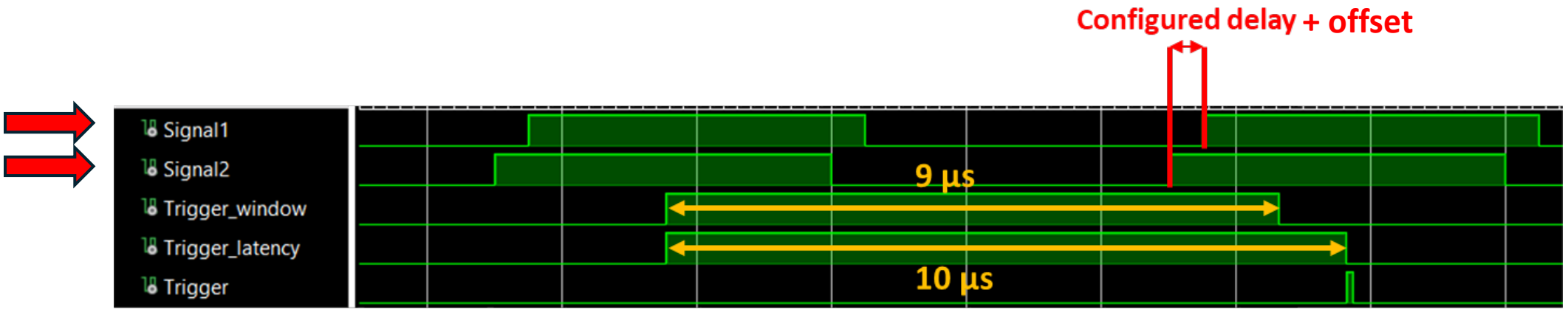
1. power supply
2. picoTDC board
3. pFEB breakout board
4. PLL clock generator (SiLabs Si5341-D)
5. electromagnetic trombone

This is the setup used for the **TDC resolution estimation** performing a **two-channel time measurement,** considering **two clock signals** (100 kHz) and employing an **electromagnetic trombone** to shift one of the two signals by a **delay within the 0-600 ps range**

https://amslaurea.unibo.it/32161/

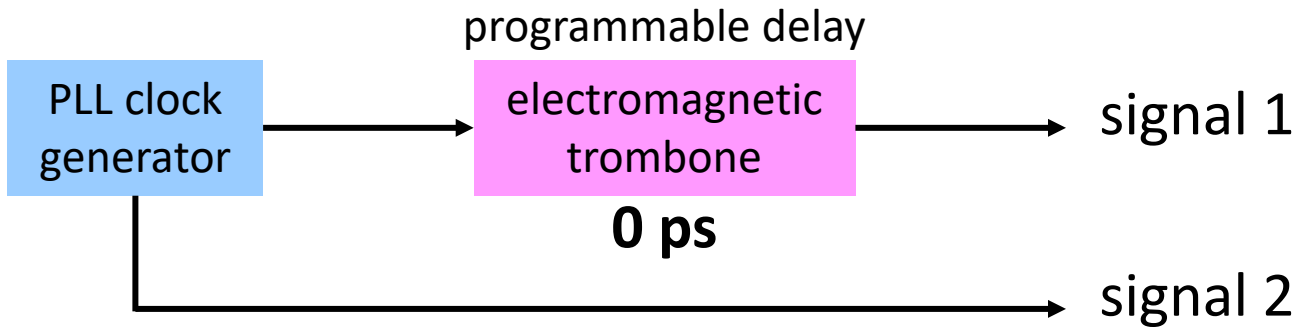
TDC resolution measurements

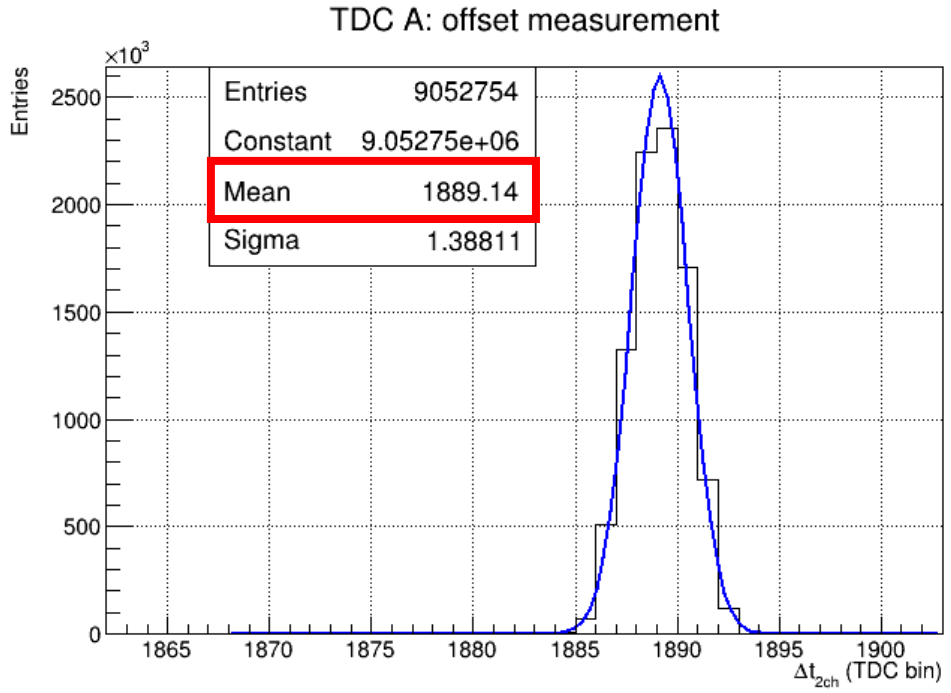


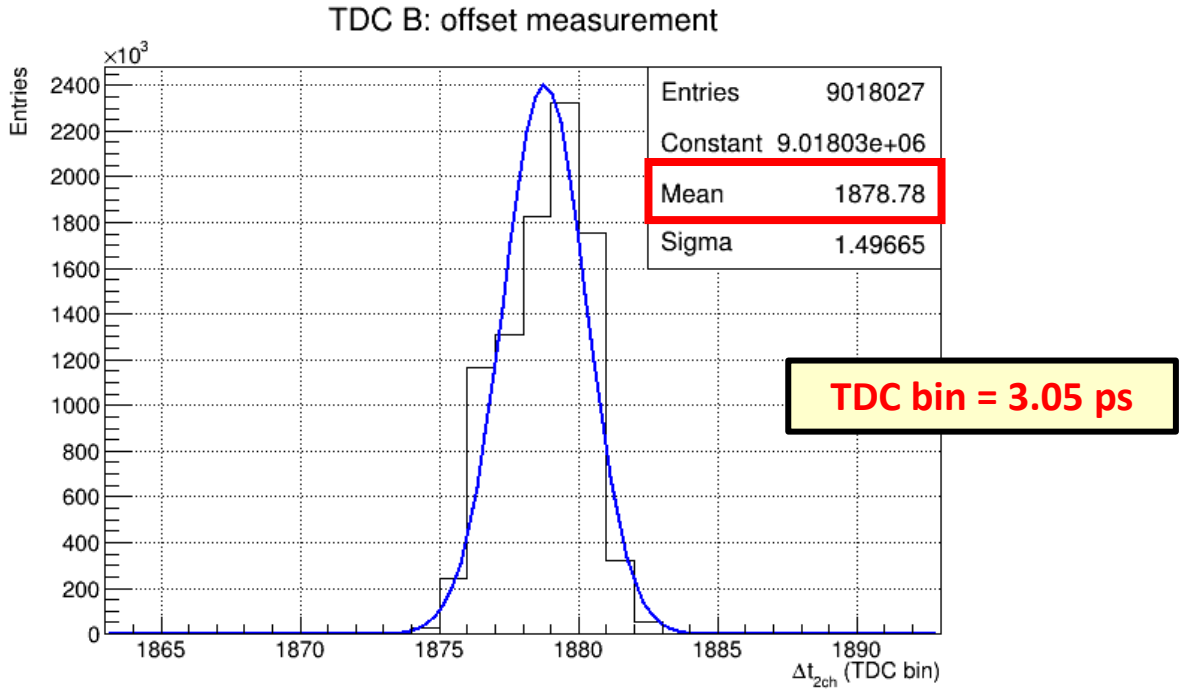


A software generated trigger is sent at 10 KHz

Data analysis and results: offset measurement





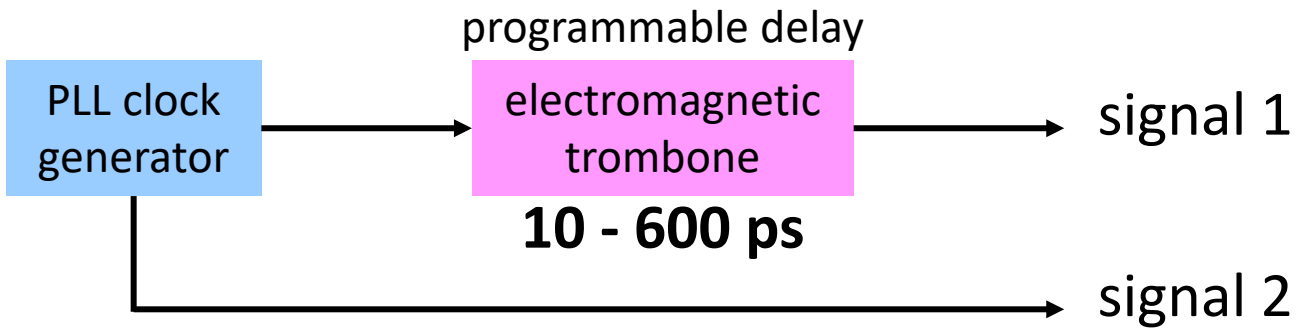


TDC bin = 3.05 ps

offset picoTDC A = 1889.1 · 3.05 ps = **5761.9 ps**

offset picoTDC B = 1878.8 · 3.05 ps = **5730.3 ps**

Data analysis and results (2)



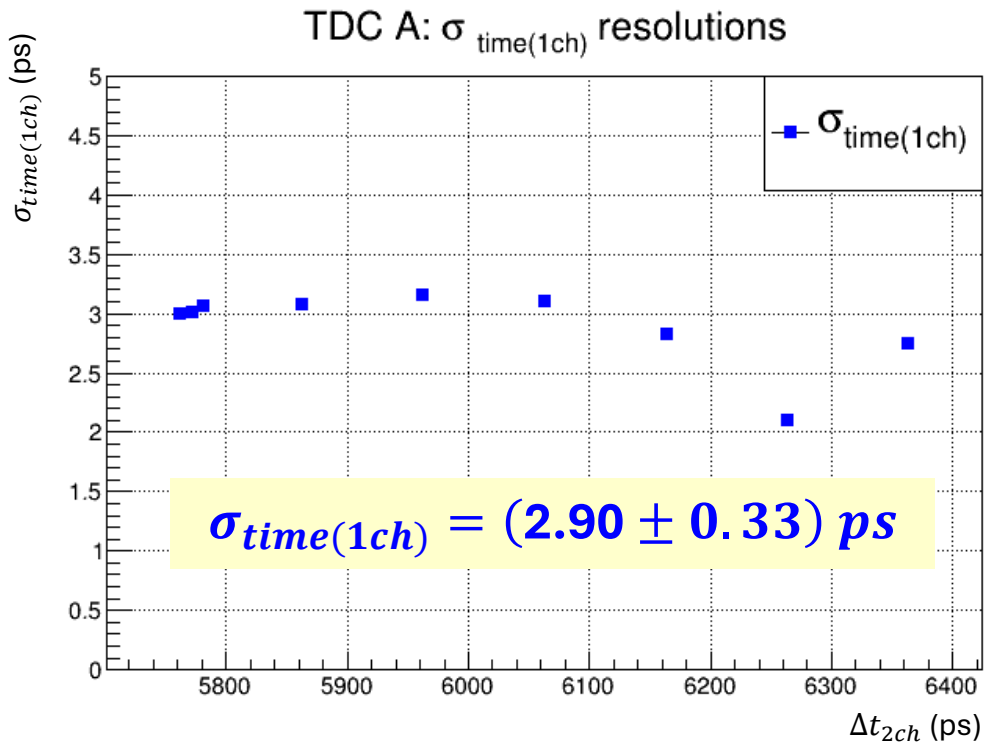
	picoTDC A		picoTDC B	
delay (ps)	$delay_{meas}$ (ps)	$\sigma_{time(2ch)}$ (ps)	$delay_{meas}$ (ps)	$\sigma_{time(2ch)}$ (ps)
10	10.5	4.3	8.7	4.6
20	20.2	4.3	18.7	4.6
100	101.0	4.4	100.7	4.6
200	200.9	4.5	200.5	4.6
300	301.4	4.4	300.8	4.5
400	401.9	4.0	401.0	3.8
500	501.3	3.0	500.4	2.9
600	601.8	3.9	600.8	3.6

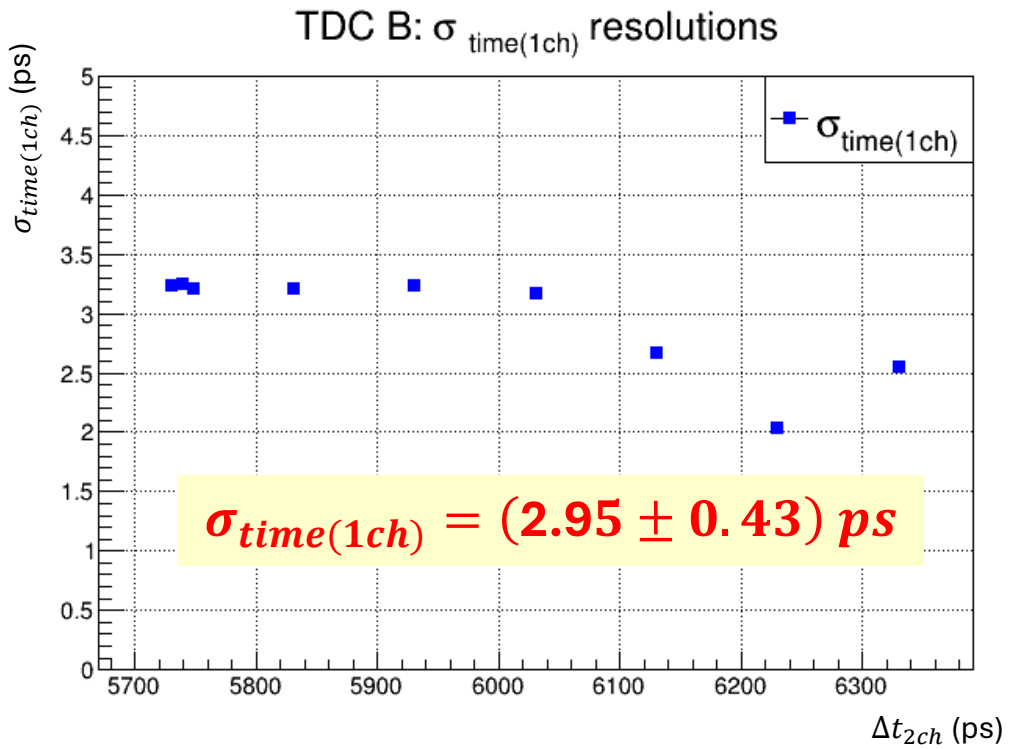
$$\mathbf{delay_{meas} = (mean_{meas} - mean_{offset}) \cdot 3.05\ ps}$$

$$\mathbf{\sigma_{time(2ch)} = sigma_{meas} \cdot 3.05\ ps}$$

The analysis results for the measured delays show an **excellent agreement (within 2 ps)** with the programmed delays

Data analysis and results (3)



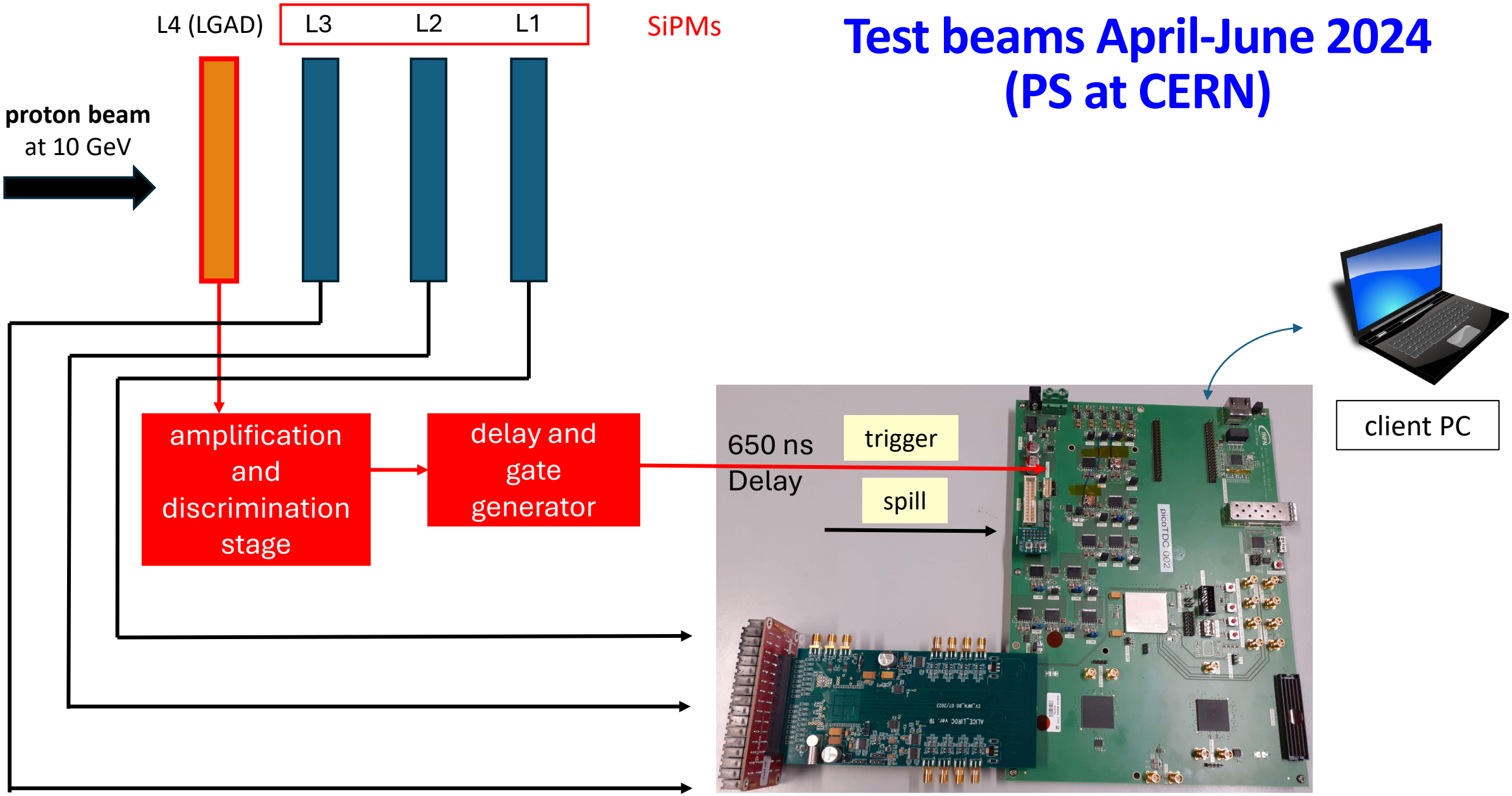


The $\boldsymbol{\sigma_{time(1ch)}}$ **resolution** value for each dataset is estimated, using the following:

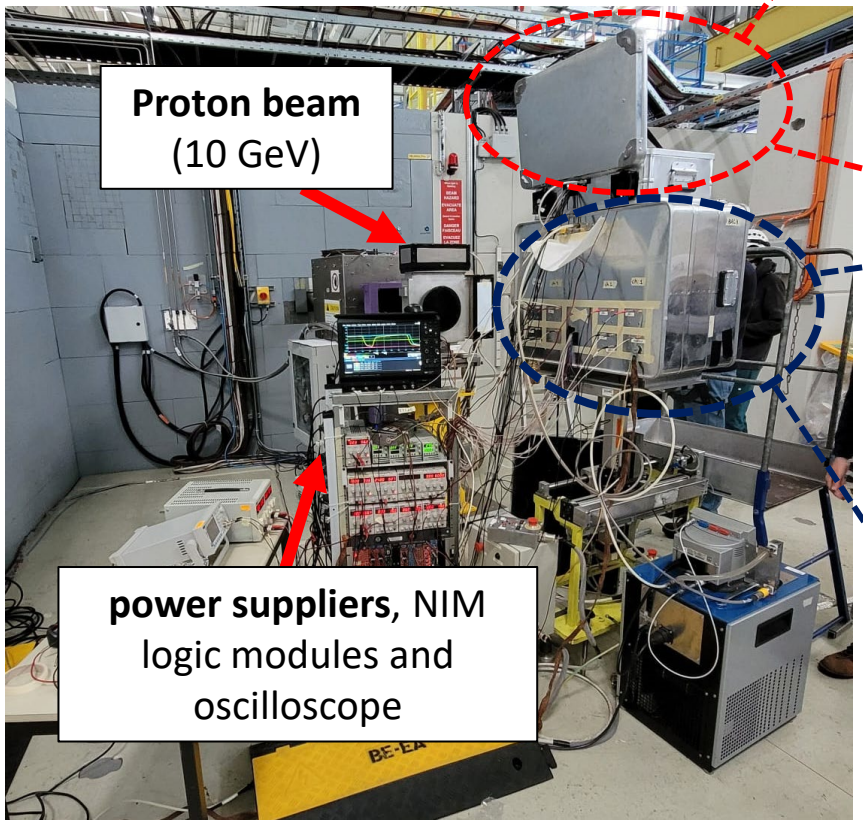
$$\boldsymbol{\sigma_{time(1ch)} = \frac{\sigma_{time(2ch)}}{\sqrt{2}}}$$

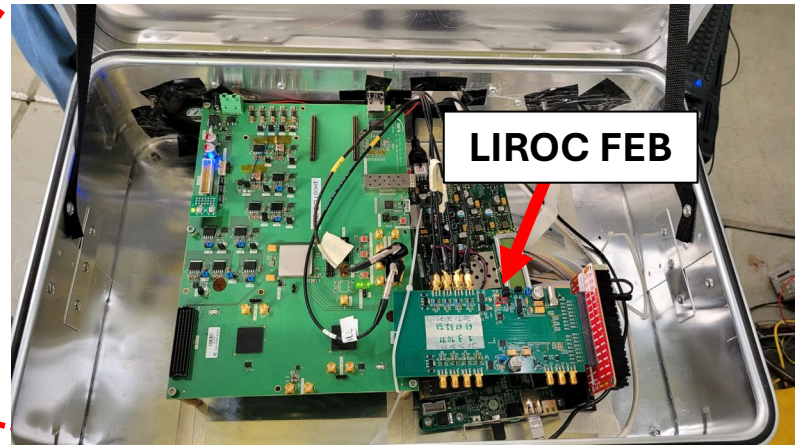
The **1-channel resolution** measured for both TDCs, **within a time interval of 600 ps**, is found considering the **mean** and the **standard deviation** for all 9 measurements

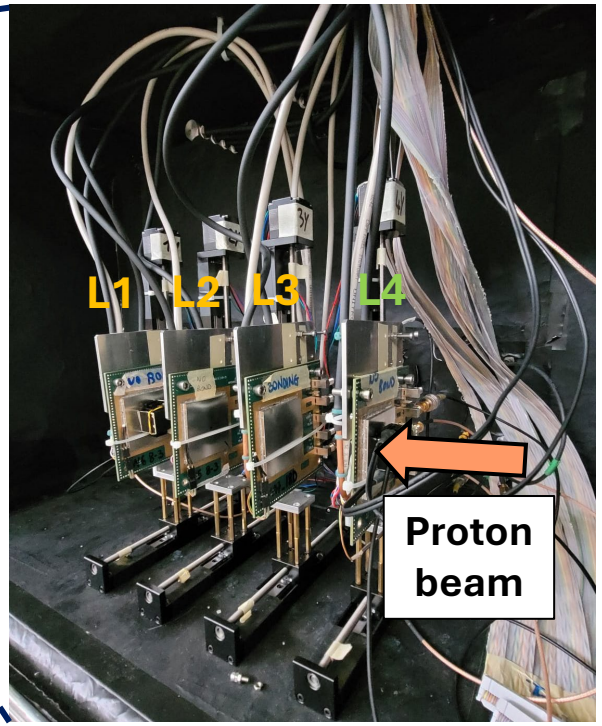
Test beams April-June 2024 (PS at CERN)



Test beams April-June 2024 (PS at CERN)





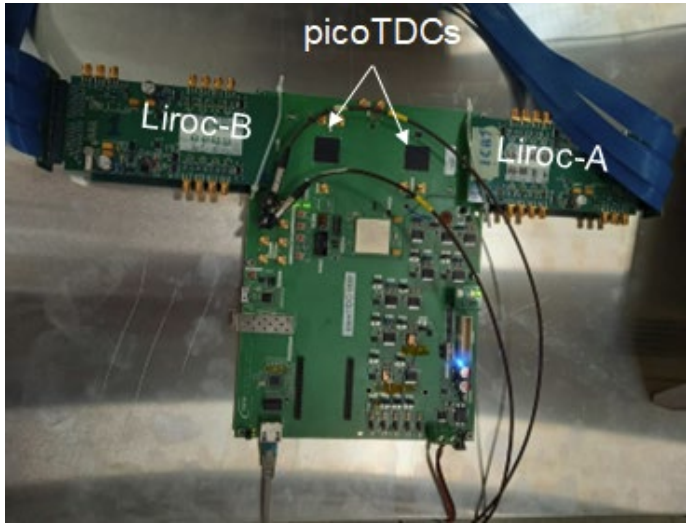


Sensor box including **four layers** (**LGADs** and **SiPMs**):

- **L4:** LGAD signal used as **the trigger signal**
- **L3, L2, L1:** **SiPM** sensors connected to **TDC input channels**

Readout electronics box including:

- **the DAQ chain**: the **PicoTDC board** and the **LIROC FEB**



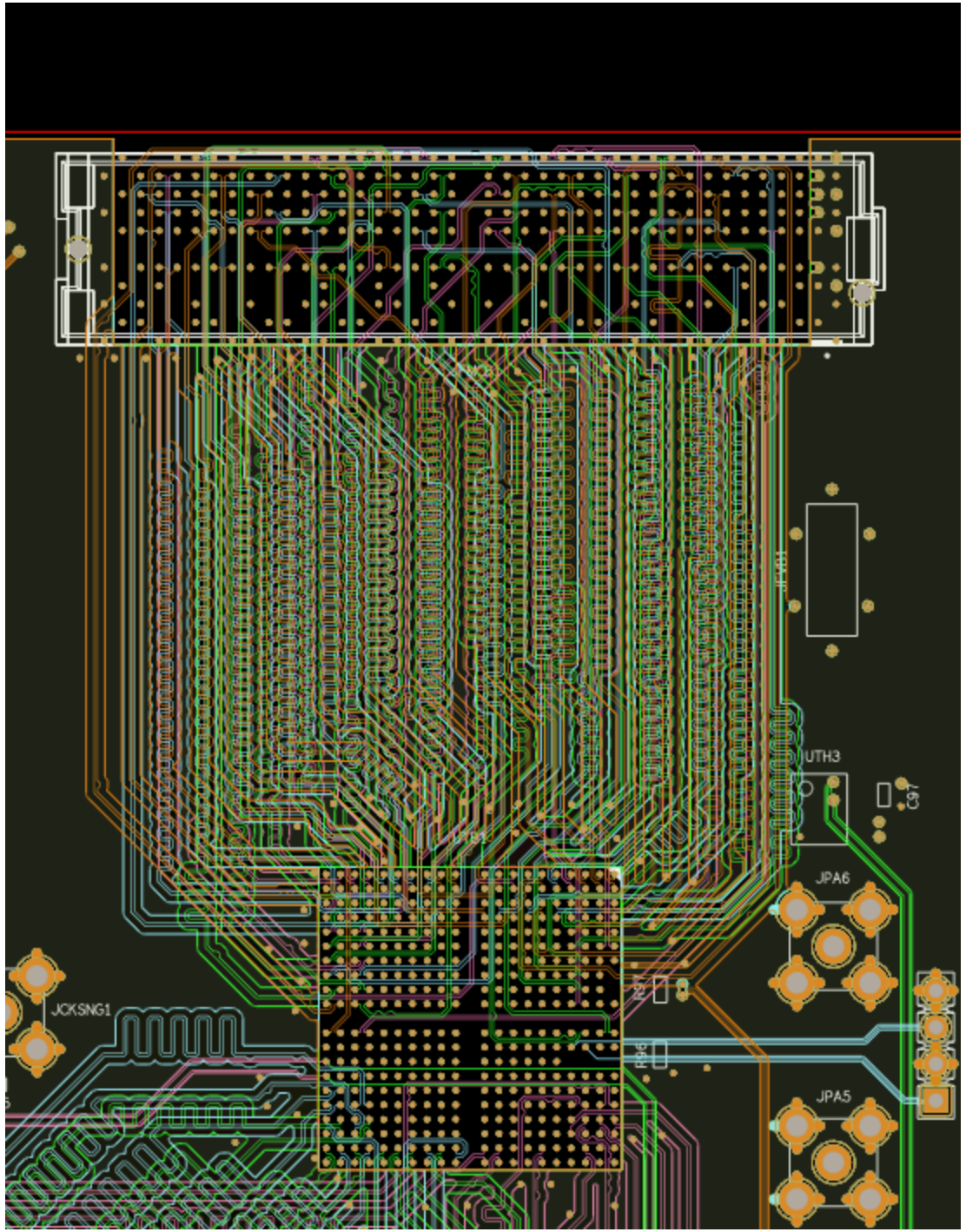
at TB of June/July 2024, **five layers** were employed and **both the TDCs on board** were used!

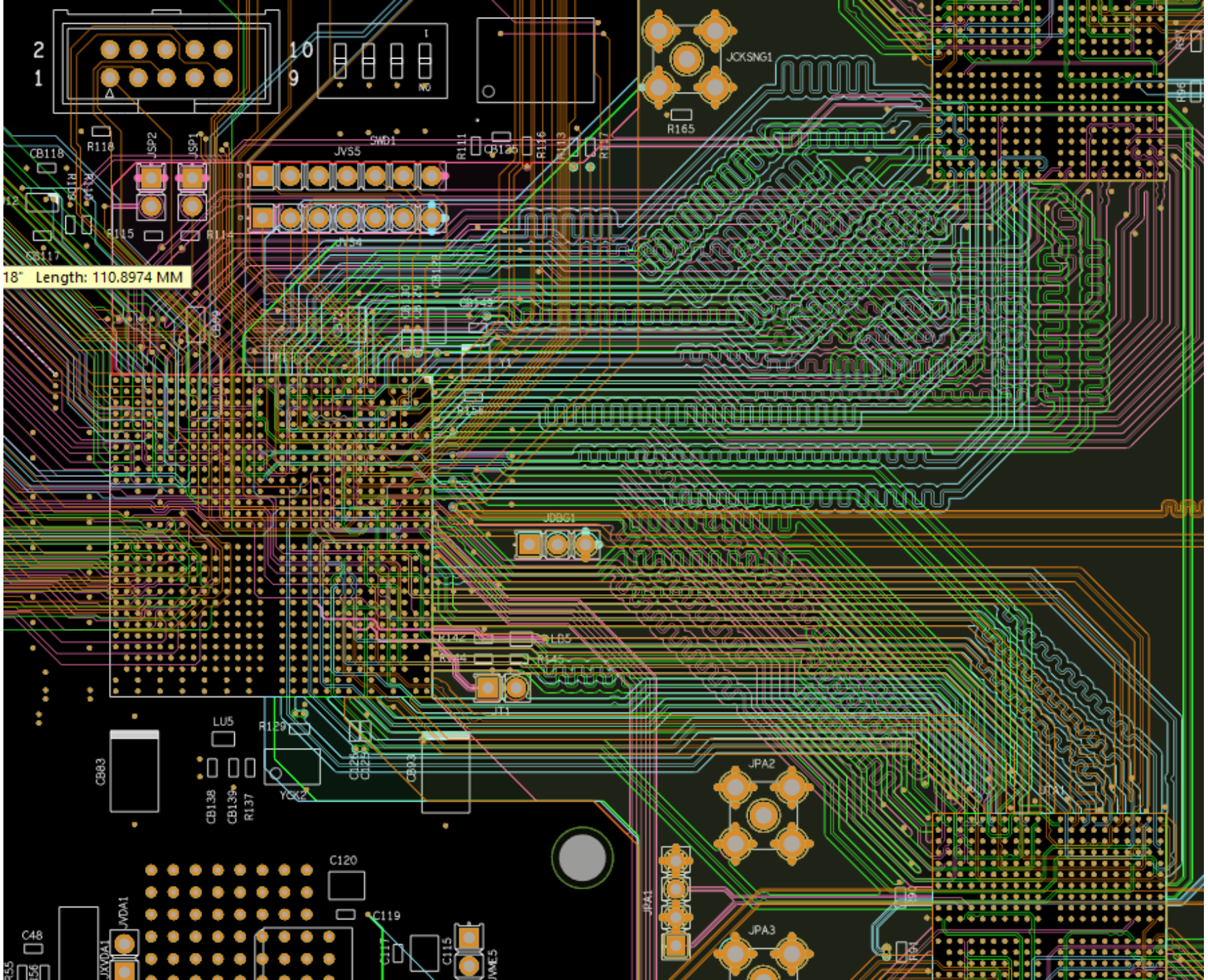
Conclusions and overlook

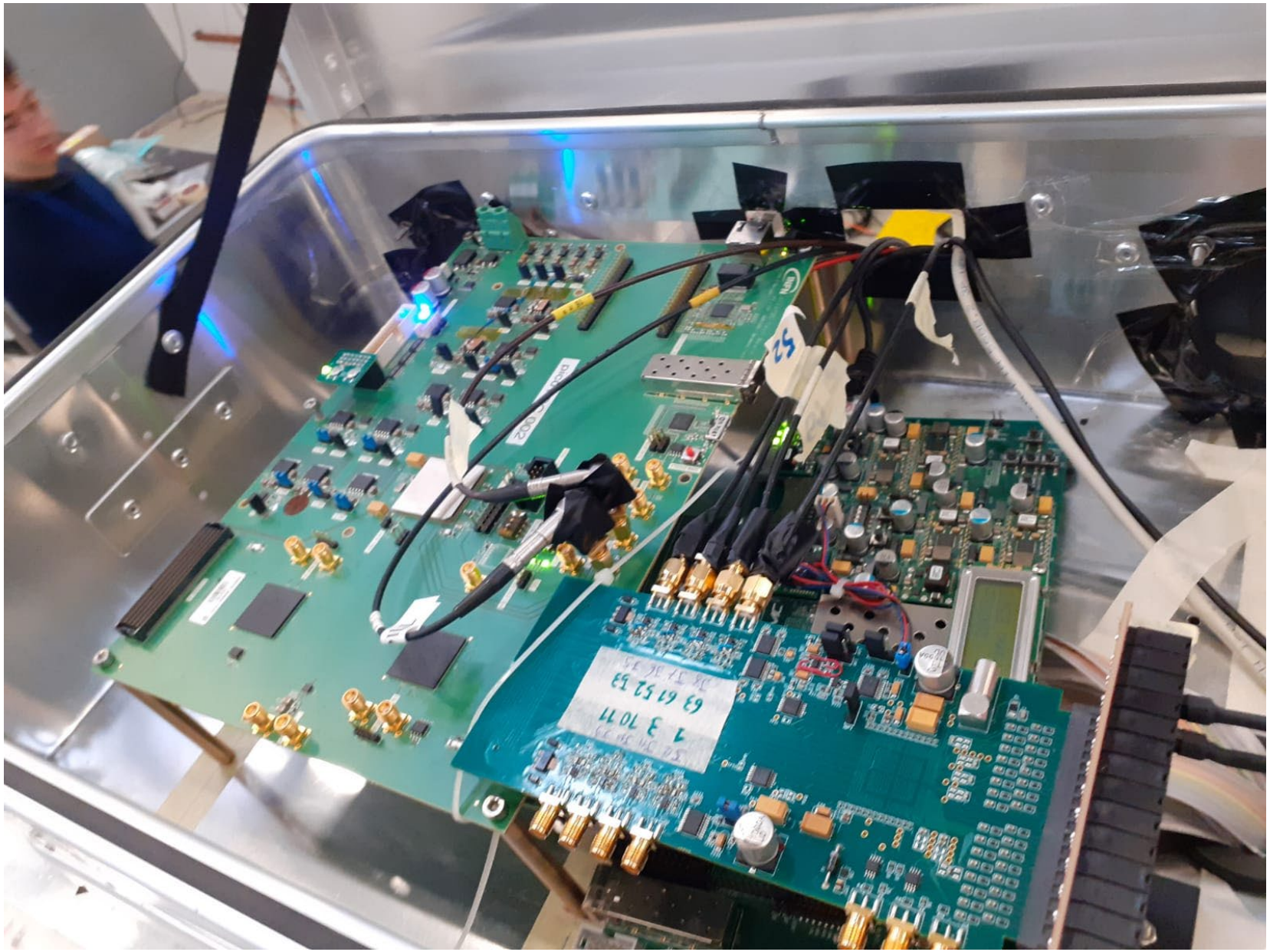
- we developed a board providing fast timing measurement on 128 channels
- we measured a picoTDC resolution as low as 3 ps, as expected
- we developed a family of pFEB boards to allow an easy connection to different detectors / front end electronics
- intensive use at on-going test beams in the context of AIDAInnova and ALICE3 R&D
- upcoming plans include:
  - developments of other generic FMC-PFEB cards (LVDS - Sub-LVDS adapters, etc.)
  - implementation of the data transfer over the optical link and USB-C
  - irradiation tests of some components
  - use the board as “open tool” to engage master students

Thanks !!!

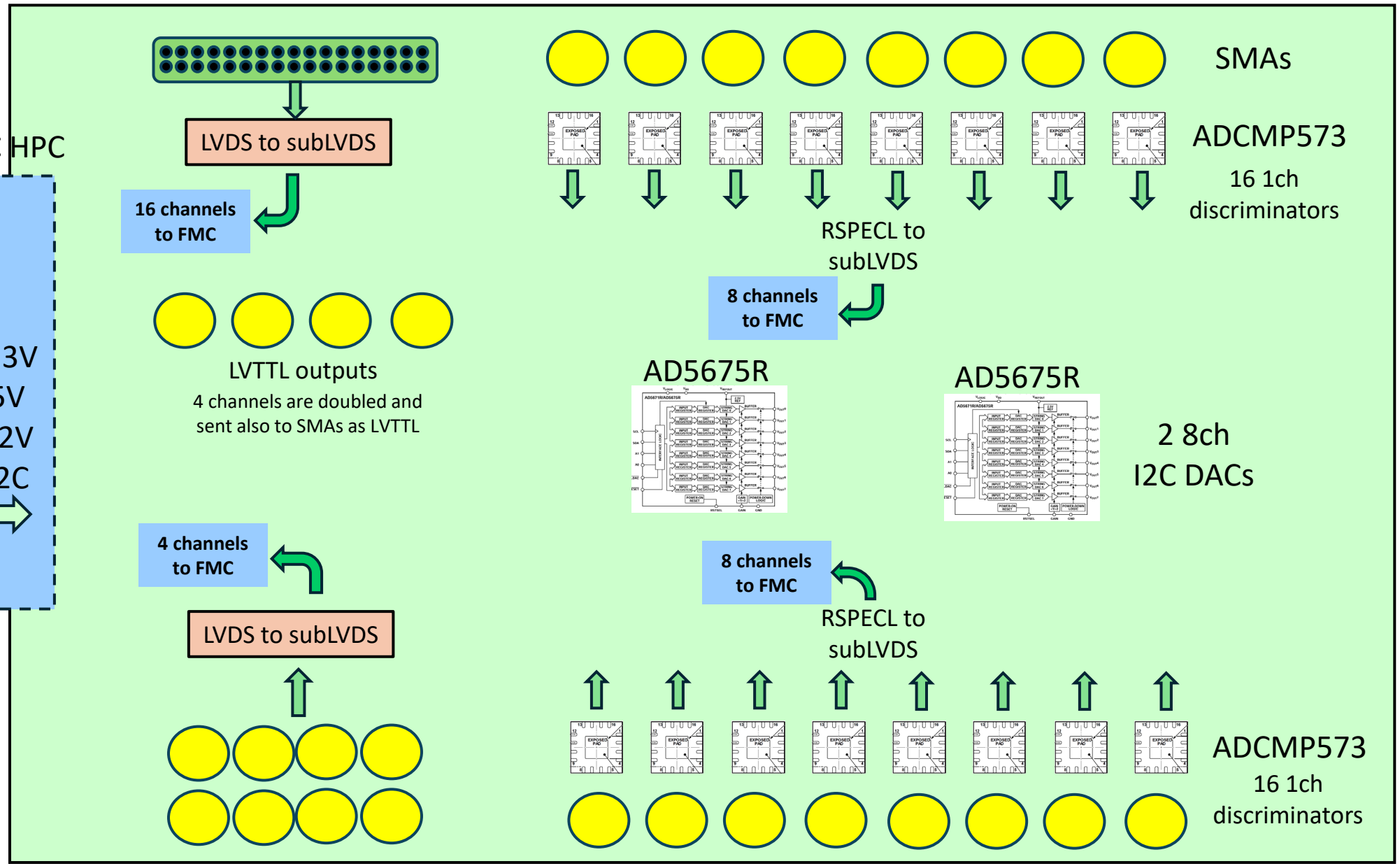
Backup

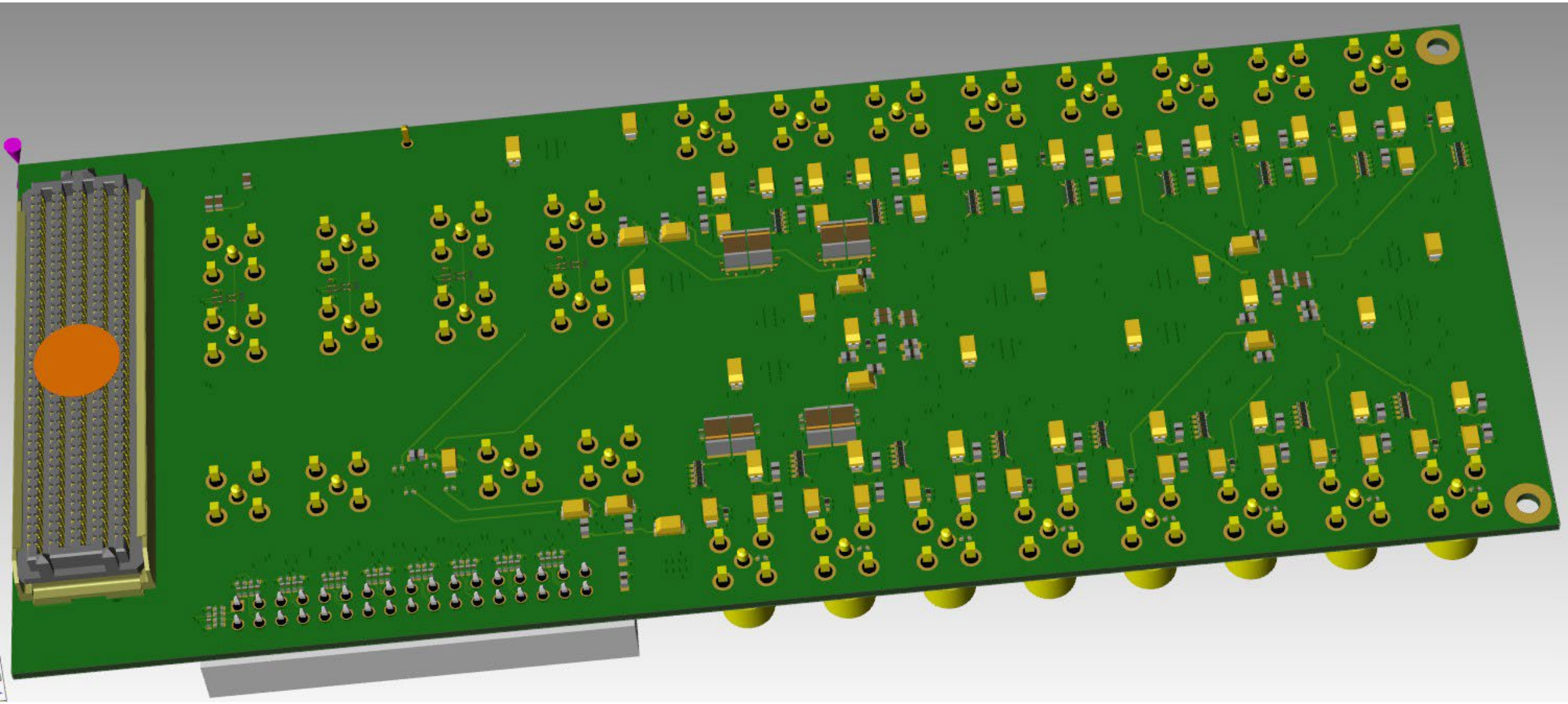

UTH3
JPA6
JCKSNG1
JPA5

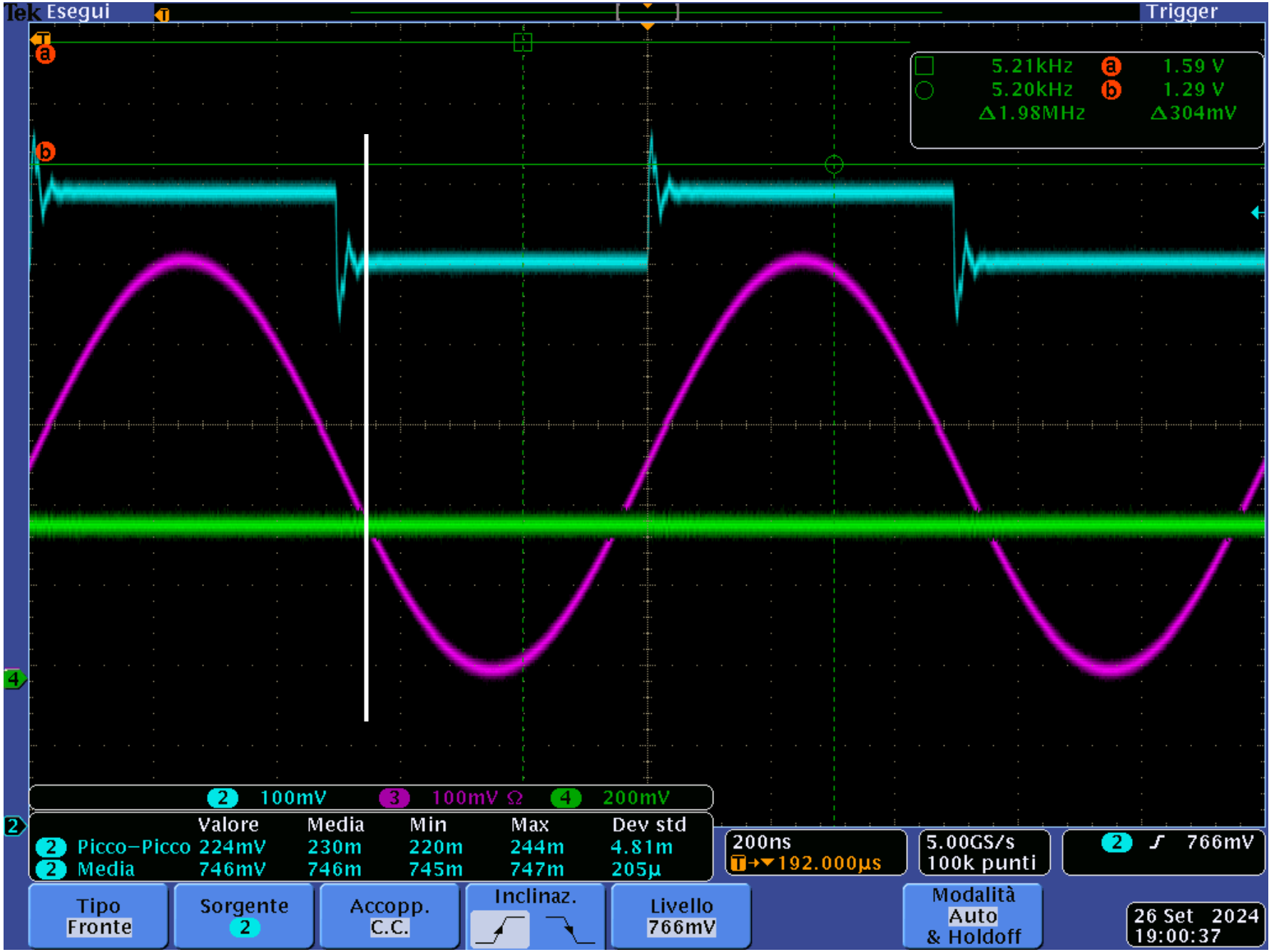

18" Length: 110.8974 MM
JCKSNG1
R165
JV55
SWD1
JSP2
JSP1
R118
CB118
R115
JDBG1
LU5
R129
CB83
CB138
CB139
R137
YC62
C120
C119
C115
C48
JVDA1
JPA2
JPA3
JPA1



A family of picoTDC compatible Front-End Boards (3)






Tek Esegui
Trigger
5.21kHz
5.20kHz
Δ1.98MHz
1.59 V
1.29 V
Δ304mV
2 100mV
3 100mV Ω
4 200mV
Valore Media Min Max Dev std
2 Picco-Picco 224mV 230m 220m 244m 4.81m
2 Media 746mV 746m 745m 747m 205µ
200ns
T→▼192.000µs
5.00GS/s
100k punti
2 766mV
Tipo
Fronte
Sorgente
2
Accopp.
C.C.
Inclinaz.
Livello
766mV
Modalità
Auto
& Holdoff
26 Set 2024
19:00:37