Design and Implementation of a Compact Analog Constant Fraction Discriminator for High-Resolution Timing in Gamma-Ray Spectroscopy

— TWEPP 2024 in Glasgow —

Michael Wiebusch

Experimentelektronik, GSI Darmstadt

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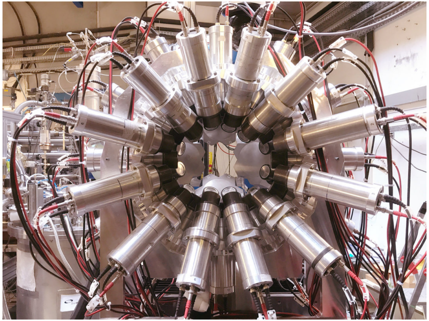
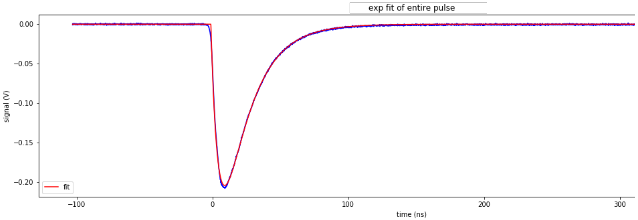
The Experiment



FATIMA - FAst TIMing Array at DESPEC, GSI Darmstadt

- 36 $LaBr_3(Ce)$ scintillators + PMTs
- measure **lifetimes** of exoctic nuclei $\Rightarrow$ detect decay γ **rays**
- need precise **time** of arrival AND **energy** (better than 3%)
- aim for amplifier + discriminator + **TDC** readout
- ... could benefit from a **CFD**!

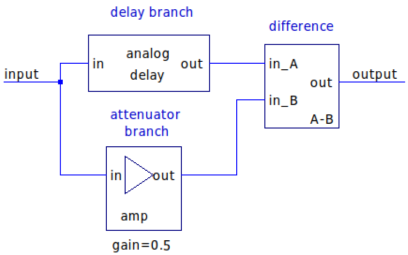


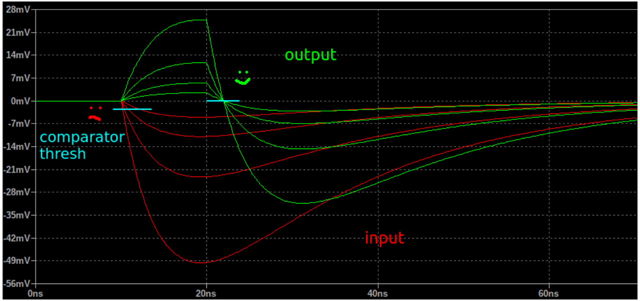
signal shape: $\tau_{lead} = 5.8\,ns$, $\tau_{tail} = 20\,ns$
relevant amplitudes: $10\,mV$ to $700\,mV$

Motivation

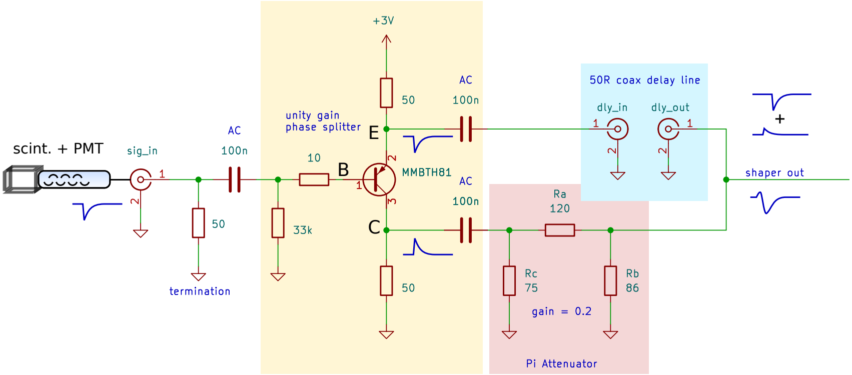
My Hobby: Discrete Circuit Golf

- What's the circuit with the fewest parts that acts as a **Constant Fraction Discriminator**?
- Nanosecond regime without expensive power hungry OpAmps?
- Let's see!

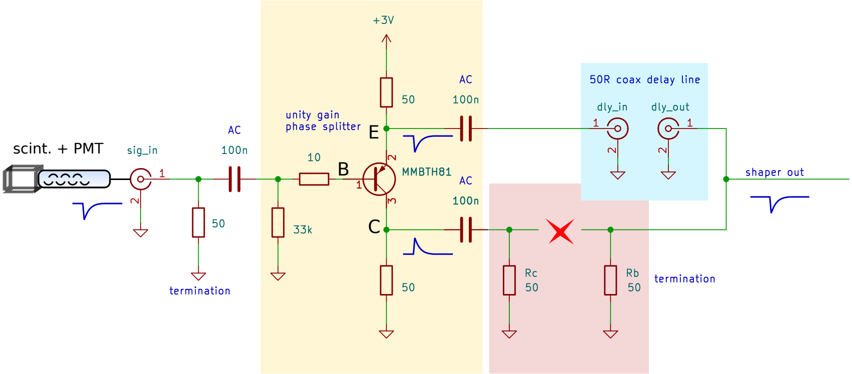




- A circuit (or signal processing algorithm) to counteract the time-walk effect when discriminating PMT or similar signals
- Superposition of delayed and attenuated copy - produce a zero crossing ("knot")
- Detect zero crossing with comparator → walk free time of arrival!

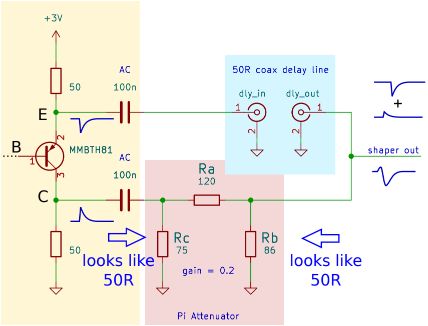


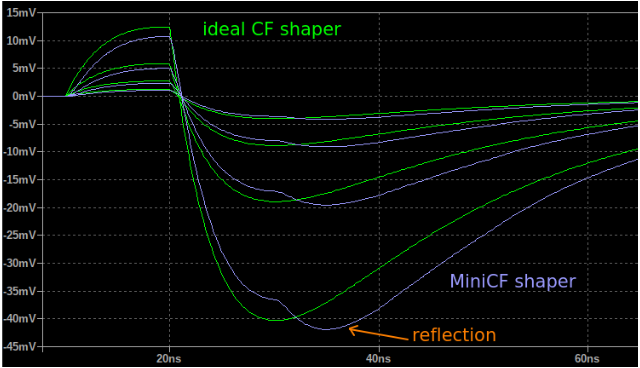
- Parts count: 1 transistor, 1 cable, handful of passives
- Passive analog summation - expect to lose amplitude - but we (almost) don't! How?
- Let's take a step back



- First we terminate the transmission line with 50R
- Match the load on the other transistor terminal (collector)
- Now we have unity gain follower (with delay)

MiniCFD features

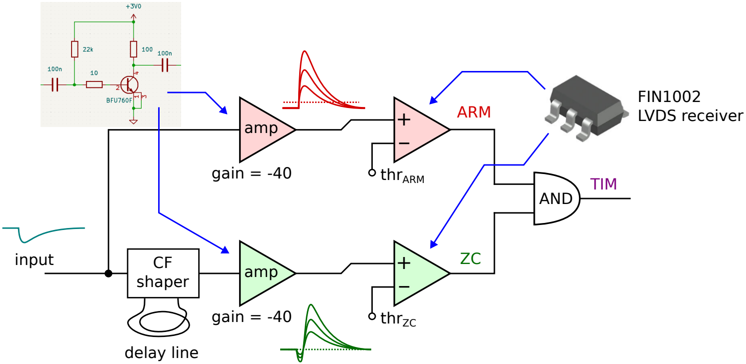




- Pi Attenuator can match impedance on both sides *AND* have a defined gain
- Emitter and Collector see same load :)
- Transmission line is terminated at the far end, but not at transistor ⇒ reflection
- But reflection doesn't matter, desired zero crossing is there!

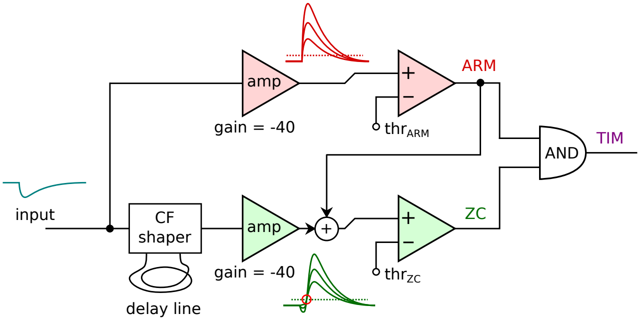
Python + Sympy help solving for the attenuator values

```
In [1]: from sympy import *

        Ra, Rb, Rc, F , Z0 = symbols("R_a R_b R_c F Z_0")
        init_printing()

        #################################################
        ##            Ra = 120 , F = 0.2              ##
        #################################################

        # The collector of Q has an output impedance close to 0,
        # so Ra || Rb = 50R to terminate the transmission line
        # The emitter of Q is loaded with 25R, i.e. 50R resistor || 50R transmission line
        # The collector of Q also needs to see the same load:
        # Rc || (Ra + (Rb || Z0)) = 50R

        equations = [ (1./Ra + 1./Rb)                                 - 1./50.,
                     Ra                                               - 120.0 ,
                     Z0                                               - 50.,
                     1./Rc + 1./(Ra + 1./(1./Z0 +1./Rb))             - 1./50. ,
                     F                      -    1./(1./Z0 +1./Rb)/(Ra + 1./(1./Z0 +1./Rb))    ]
        unknowns  = [Ra,Rb,Rc,F,Z0]

        solutions = solve(equations,unknowns)
        print(unknowns)
        solutions

        [R_a, R_b, R_c, F, Z_0]

Out[1]: [(120.0,   85.7142857142857,   74.6113989637306,   0.208333333333333,   50.0)]
```



- Simple common emitter amplifiers to boost signals for comparator (LVDS receiver)
- Threshold DAC ⇒ PWM on FPGA GPIO + RC
- ZC exactly at baseline ⇒ lower comparator noising when idle

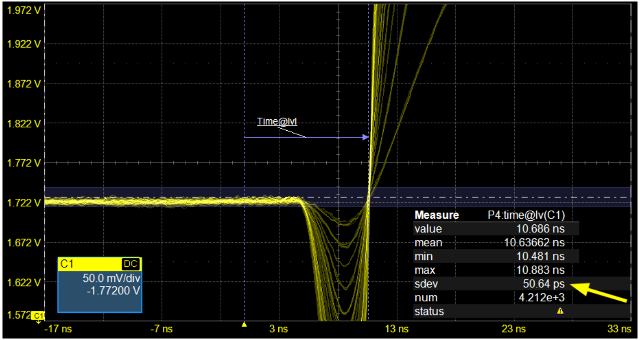
So Far: Only CF ... Now Discriminator



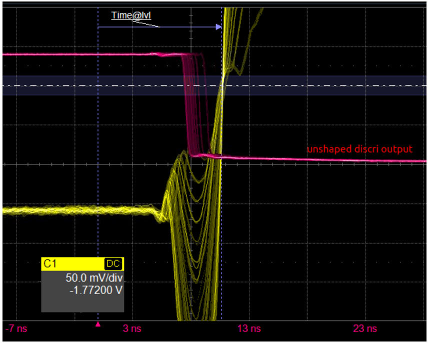
- Add a tiny bit of the ARM TTL signal to CF-shaped signal
- Zero-Crossing now above baseline!

Shaper in Real Life

Waveforms measured with prototype board and pulse generator
Shaper settings: Fraction = 0.3, Delay = 2.5 ns

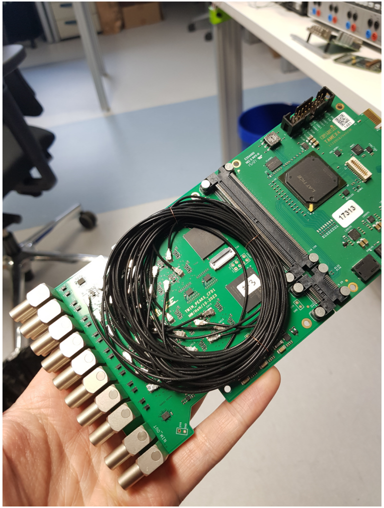


CF shaper + amplifier



CF shaper + amplifier + kick

The Board



"Twin_Peaks_CFD1" analog Front-End

- 16 channels with LEMO inputs
- board size: $12 \times 10\,cm$
- plugs onto a 32 ch FPGA based TDC card (in-house development: TAMEX4, prec. $15\,ps$)
- board features integrating pulse shaper for charge ($\approx$energy) measurement
- delay lines are $2.5\,ns = 50\,cm$ Hirose U.FL cables (e.g. WiFi antenna connectors in notebooks)
- total board power $\approx 6W$

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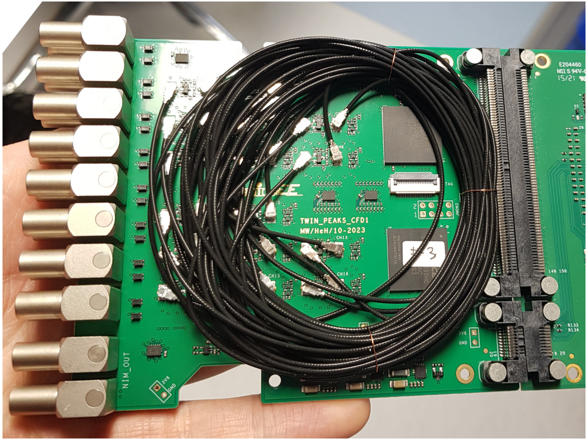

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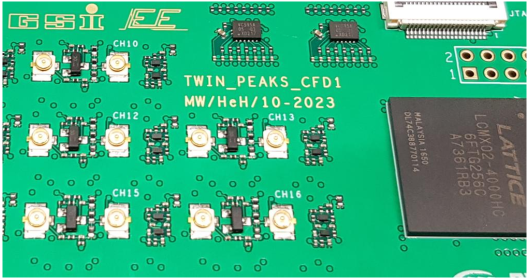

channel front

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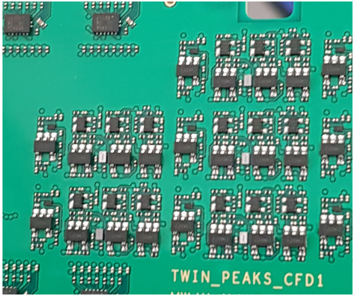

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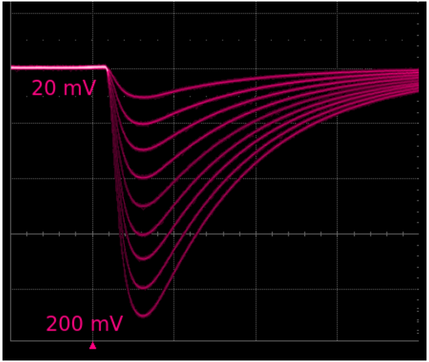
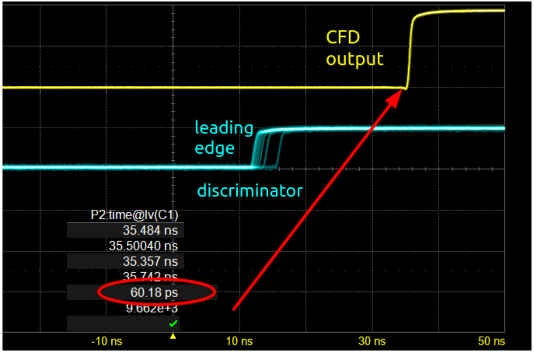
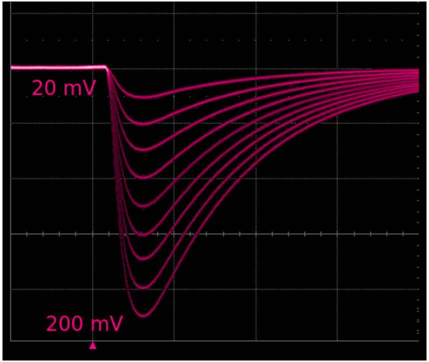


LaBr-like input signals
$\tau_{rise} = 5.8\ ns,\ \tau_{fall} = 20\ ns$



logic output signal from LE-Discriminator vs CFD



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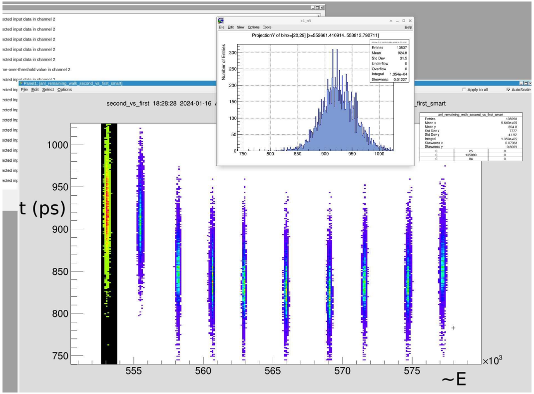

residual walk as function of amplitude

Conclusion

Summary

- A compact **CFD** Front-End was designed for the needs of a fast **gamma scintillator array** (FATIMA at DESPEC)
- Commercial **mini coax cables** (U.FL) were used as delay elements
- The complexity and cost of the CFD circuit was greatly reduced by **analog circuit tricks**
- The desired **performance** was achieved in the **lab** and during an **experiment** run

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Perspectives

- follow-up projects: fast scintillators + SiPMs
- faster **rise time** $\Rightarrow$ shorter **delay** for CFDs
- integrate delay lines in **PCB**?
- direct integration of CF(D) in the detector?