An FPGA-based Data Aggregator for the New ATLAS ITK Pixel DCS

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The upcoming ATLAS Phase II upgrade mandates replacing the tracking system with the all-silicon Inner Tracker (ITK), featuring a pixel detector as its core element. The monitoring data of the new system will be collected from an on-detector ASIC, Monitoring Of Pixel System (MOPS), and aggregated to the Detector Control System (DCS) via a newly developed FPGA-based interface known as MOPS-Hub. The implementation details and experimental outcomes of the MOPS-Hub will be presented. Additionally, mitigation strategies for addressing potential Single-Event Upset (SEU) issues in the new system along with the proton irradiation results, are presented.

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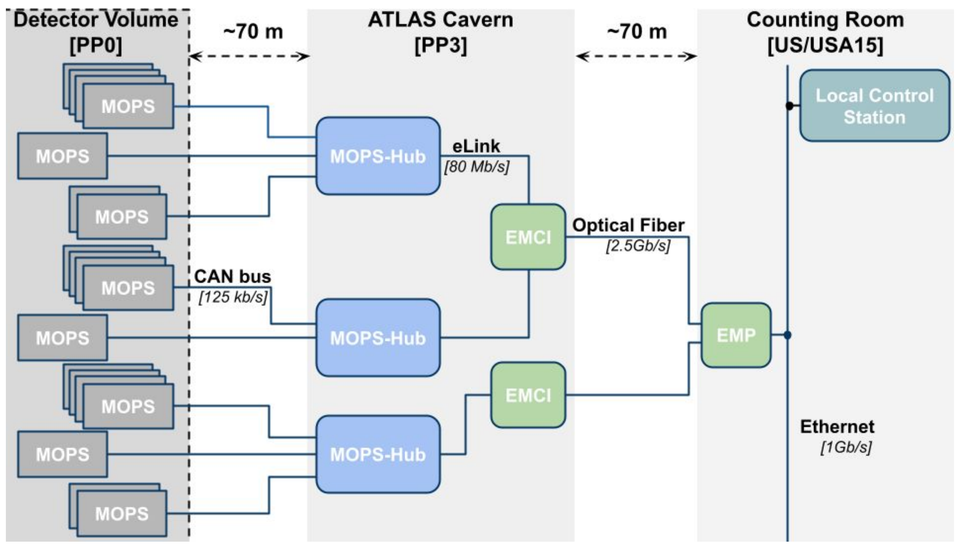
The NEW ITK Pixel DCS System

The control and monitoring path of the DCS system includes:

1. The MOPS (**M**onitoring **o**f **P**ixel **S**ystem) chip.
2. MOPS-Hub system.
3. Power supplies.
4. The DCS computer (main counting room).



The main communication interface between the MOPS [*ca.* ***1100 MOPS*** *inside the detector volume*] and the DCS control station in the counting room is facilitated using the **MOPS-Hub**

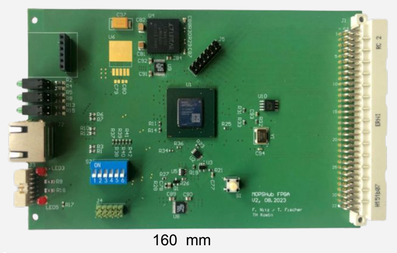
Specifications of the new interface:

1. Communication and power lines of the CAN busses are **galvanically isolated**.
2. Able to manage up to 16 CAN buses/MOPS-Hub (Each has up to 4 MOPS).
3. **6** different ATLAS cavern locations (Patch Panel **PP3**).
4. Components are radiation tolerant.
5. Make a high data transfer over long cables (70m between PP3 and the counting room).

- Up to **8 MOPS-Hub** to **1 Embedded Monitoring and Control Interface (EMCI).**
- **The EMCI** combines all E-Link signals of the MOPS-HUBs in one bidirectional **serial channel using Low-Power Gigabit Transceiver** (**LpGBT**)**.**
- The **Embedded Monitoring Processor (EMP)** will drive up to 12 **EMCIs** and interfaces them to the control network (Ethernet).

Specifications of the PP3-FPGA:

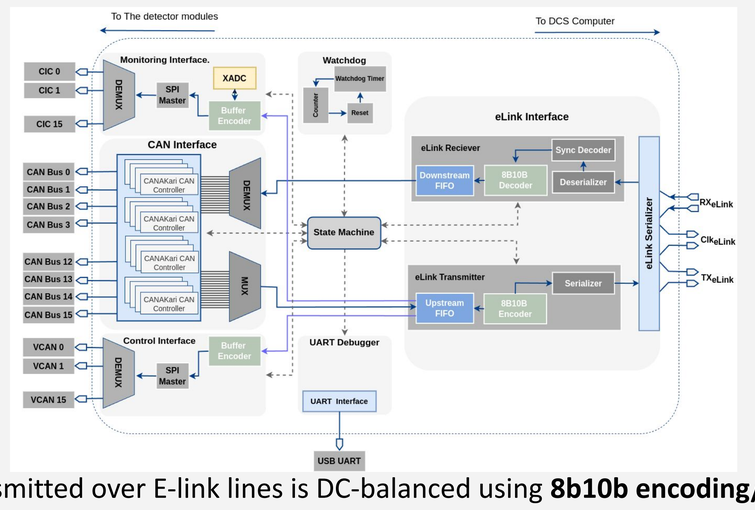
- Core unit of MOPS-Hub is the PP3-FPGA board (**Artix 7 XC7A200T**).
- External watchdog IC as an additional safety precaution.
- **MOPS-Hub Functionality:**
  1. Aggregate measurement data from the MOPS chips.
  2. Send out all values to the DCS control station.
  3. Control power of individual **VCAN**[1] lines (ON/OFF).
  4. Monitor voltage and current of all **VCAN** lines.
- **Radiation Tolerance**
  - **TID**: up to 10 krad (150 krad with safety factor).
  - **Neutron fluence**: $5x10^{11}/cm^2$ neutron equiv.fluence.
  - **Hadron fluence**: $2x10^{-7}$ cm^2/pp.



PP3-FPGA V2

[1]*VCAN:* power lines for individual MOPS.

Firmware Specifications:



- The data transmitted over E-link lines is DC-balanced using **8b10b encoding/decoding.**
- **The Central Finite State Machine** brings the system in a working state and supervises the data aggregation from MOPS to the local control station.
- The control power of individual is handled via a separate SPI bus.
- The monitoring information/CAN bus (voltage/current of Vcan) is acquired via an SPI bus.
- Debugging and diagnostics via UART communication.
- SEU/SET mitigation is needed for fabric logic elements and configuration memory.

SEU Mitigation Architecture

SEU mitigation in the MOPS-Hub has 4 levels:

Level 1: State Machine and Logic
- **Mitigation Technique:** Watchdog

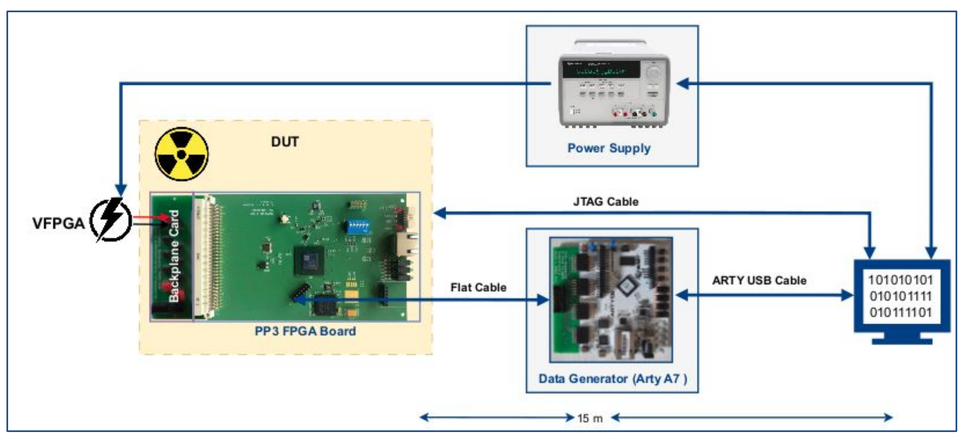
Level 2: Fabric logic elements
- **Mitigation Technique**: TMR (FF (FlipFlops) as well as Clock and Reset Domains)

Level 3: Configuration Memory **[**Up to 2-bits upset**]**
- **Mitigation Technique**: Soft Error Mitigation (SEM) tool from Xilinx [ECC/CRC detection]

Level 4: Configuration Memory **[**Multi-bit upset**]**
- **Mitigation Technique**: Multi-boot Auto Reconfiguration.

The Test Setup at HIT

- The proton beam testing campaign was carried out at Heidelberg Ion Beam Therapy Center (HIT) at different beam settings.

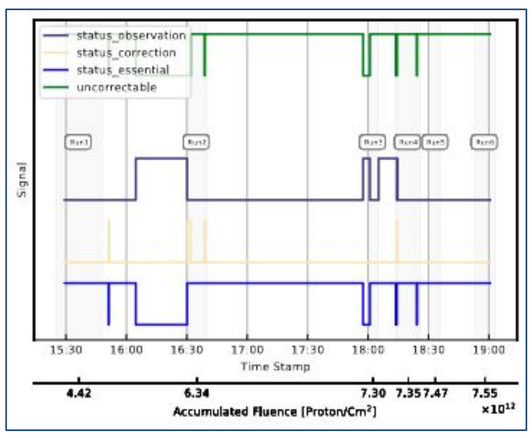


- A 3000 bit long shift register was implemented in the PP3-FPGA firmware for SEU estimation.
- The **ARTY board** acts as a control unit, writing to and reading data from the 3000 BIT shift register to check any mismatch.
- **During operation, two scenarios were considered:**
  - **With Watchdog Disabled:** to avoid resets during shift register read/write processes.
  - **With Watchdog Enabled:** for testing the Multi Boot Auto-configuration mechanism and error correction by the SEM IP.
- The DUT power supply current was continuously monitored from the Host Computer.

Proton Irradiation Results

CRAM Behaviour

- The proton irradiation of the PP3-FPGA with the watchdog enabled was performed at varying fluences, reaching a maximum of **7.5×10^{12}** protons/cm^2.
- The reset rate peaked at 2 resets per second.
  - The SEM IP can correct up to 2 upsets in one frame , as indicated by the ***status_correction*** signal.
  - The Multi-bit Upsets potentially overwhelmed the SEM IP's protection mechanisms, evidenced by the ***status_uncorrectable*** and ***status_essential*** signals.
  - Accumulation of upsets, particularly in critical areas in the circuits disrupted the system's operation.



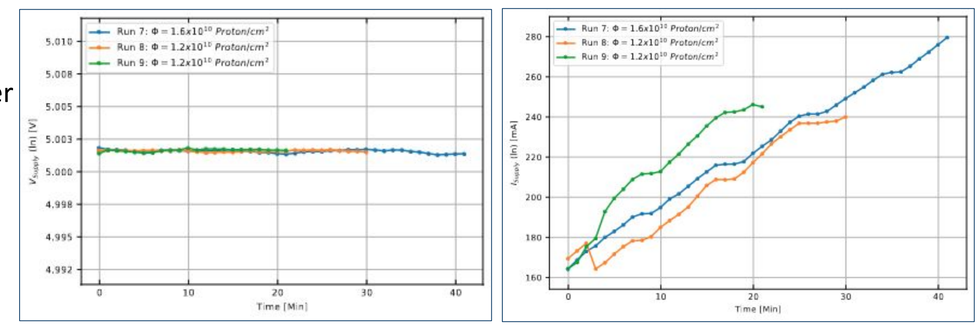
SEU Estimation

Run	Energy [MeV]	FWHM [mm]	Intensity [protons/s]	Duration [min]	Fluence [protons/cm^2]	SEUs [N]	σ [cm^2/bit]
7	145.46	11.5	8×10^8	37	8×10^{11}	7	2.92×10^{-15}
8	155.82	10.8	8×10^8	39	8×10^{11}	9	3.75×10^{-15}
9	165.89	10.2	8×10^8	17	4×10^{11}	4	3.33×10^{-15}

- A total of 20 SEUs were observed during the campaign and considered for the analysis.
- The estimated SEU rate in the CRAM of the XC7A200 can reach up to 127 SEUs in 10 years of the LHC operation.

Current and Voltage Behavior

- A preset limit == 510 mA
- No sudden increases in the power supply current.
- Accumulation of SEUs causes a gradual increase in the current consumption of the FPGA.
- The current dropped back to its initial level after reconfiguration.



- Comprehensive radiation characterization demonstrated reliable FPGA operation in harsh radiation environments has been introduced.
- The PP3-FPGA was rigorously evaluated for SEU resilience during the proton beam campaign at the HIT facility.
- Findings underscore the effectiveness of the MOPS-Hub performance for the ATLAS ITK pixel DCS.