The DAQ software for ATLAS Pixel Tracker system testing for HL-LHC

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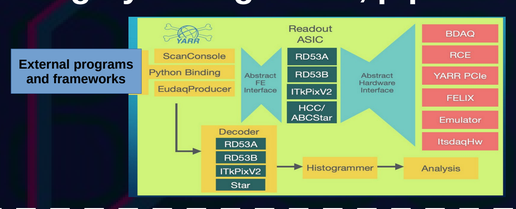
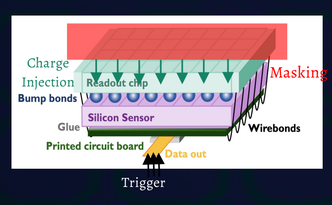
Introduction

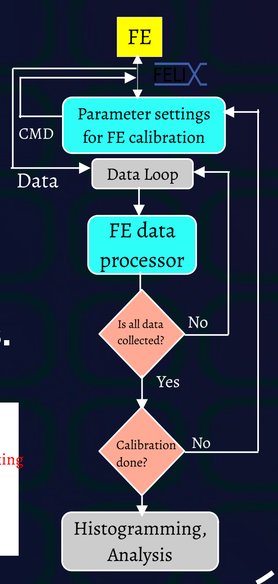
The ATLAS experiment is preparing for the High-Luminosity LHC era, by replacing the current innermost detector with an advanced all-silicon tracker (pixels and strips) to withstand radiation damage and increased particle activity. Pixel module quality control spans various production stages which necessitates a robust data acquisition software capable of handling high data rates and MHz calibrations. Yet Another Rapid Readout (YARR) software, adaptable to diverse hardware platforms including ATLAS Phase-2 readout board i.e. FELIX, facilitates these testing scenarios.

Yet Another Rapid Readout (YARR)

- Smart data acquisition software supporting various readout ASICs (silicon pixels & strips).
- Interfaces with diverse FPGA-based readout boards through PCIe link or ethernet.
- Numerous applications for on-detector electronics such as setting up the configuration, performing calibrations and running online diagnostics, in lab-scale test setups as well as testbeams and real detector operations.
- Modular by design such that conceptual pieces are separated in individual libraries with well-defined scope, functionality and interfaces.
- FE data processor is highly configurable, pipelined, and therefore naturally scalable.







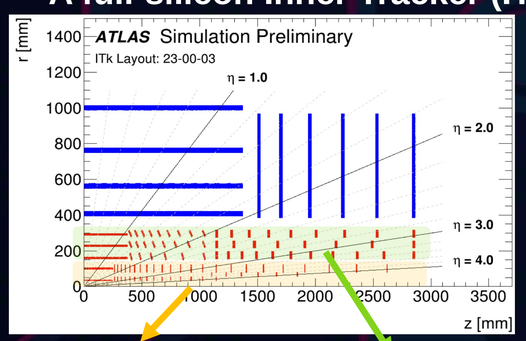
ATLAS Phase 2 readout system

- The Front-End Link eXchange (FELIX) system is an interface between the trigger and detector electronics and commodity switched networks.
- It uses FPGAs on server-hosted PCIe boards to pass data between custom data links connected to the detector as well as LHC clock and trigger information to the on-detector electronics.
- The host system memory over a PCIe interface then routes data to network clients, such as the Software Readout Drivers (SWROD) to build event fragments, buffer data, perform detector-specific processing and provide data for the ATLAS High Level Trigger.
- Readout and configuration of on-detector electronics communication will rely on the Low power GigaBit Transceiver (LpGBT) radiation tolerant protocol with Versatile Link, developed at CERN.

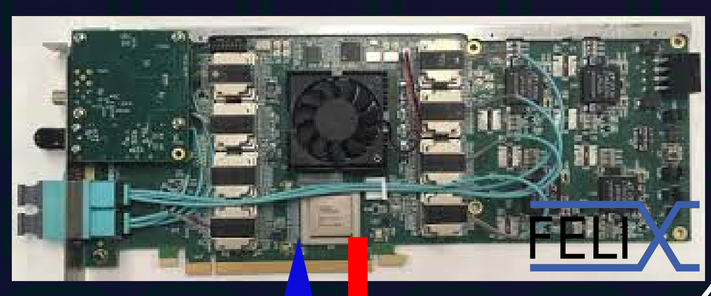
Detector	#FELIX cards	#Uplinks (data)	#Downlinks (command)	Uplink BW (Gb/s)	Downlink BW (GB/s)	Link protocol
ITk Pixel	220	4684	1564	10.24	2.56	LpGBT
ITk STrips	76	1824	1552	10.24	2.56	LpGBT

The ATLAS ITk Pixel detector for HL-LHC

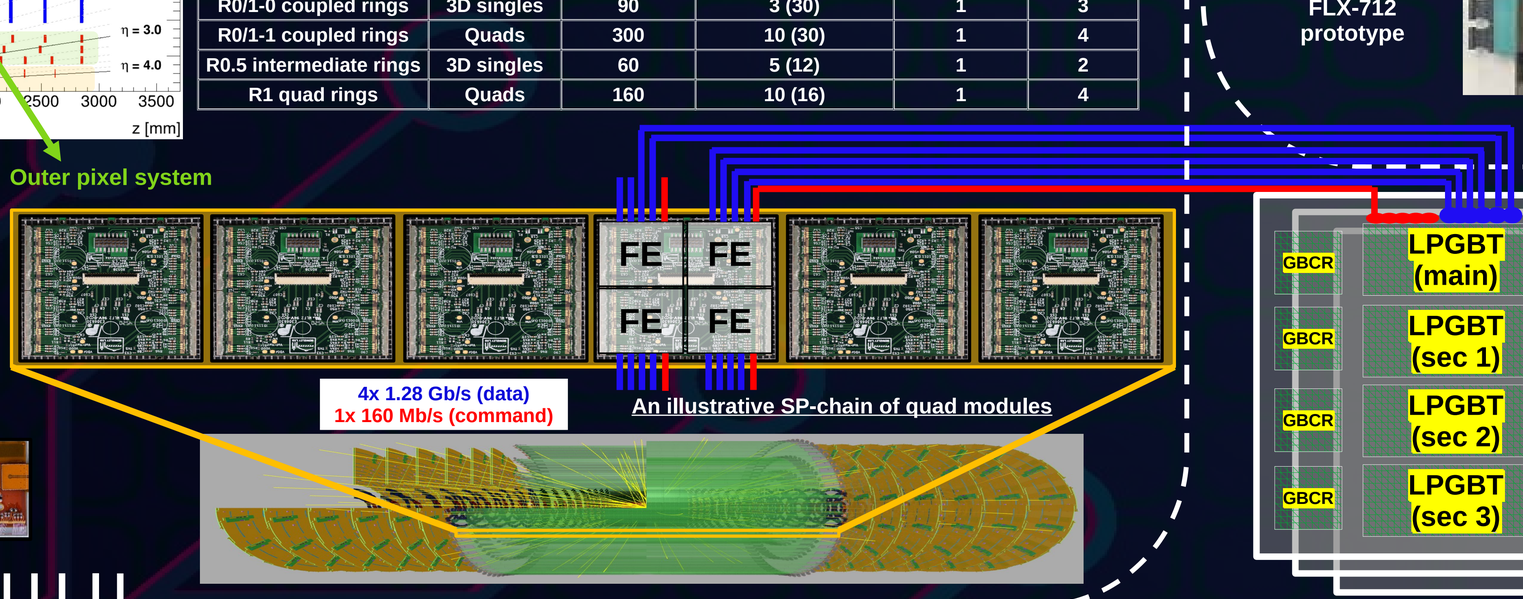
A full-silicon Inner Tracker (ITk) made of pixel and strip subdetectors. The layout of the pixel inner system is described in the table below.



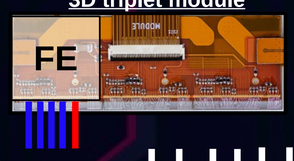
Layer	Module type	Total # of modules	Serial-powered chain length (total)	#Command/ module	#Links/ module
L0 barrel	3D Triplet	96	4 (24)	3	12
L1 barrel	Quads	240	6 (40)	1	2
R0/1-0 coupled rings	3D singles	90	3 (30)	1	3
R0/1-1 coupled rings	Quads	300	10 (30)	1	4
R0.5 intermediate rings	3D singles	60	5 (12)	1	2
R1 quad rings	Quads	160	10 (16)	1	4



FLX-712 prototype

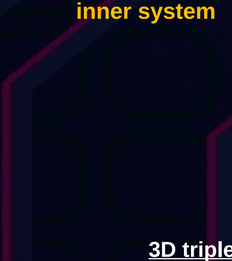


3D triplet module



Multi-module tests with YARR

Running digital calibration with up to 144 virtual FEs on a single YARR process at 5 KHz trigger frequency and 100 charge injections.

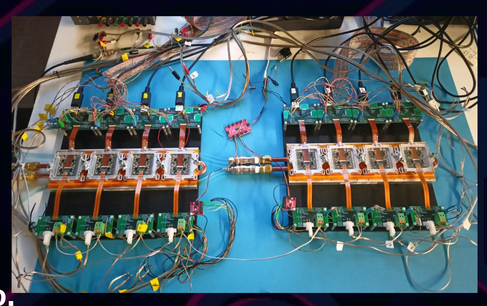


Running digital calibration with 5 ATLAS ITkPix v1.1 FEs on a single YARR process at 5 KHz trigger frequency and 100 charge injections.

Running digital calibration with 6 ATLAS ITkPix v1.1 digital quad modules on one YARR process each, at 5 KHz trigger frequency and 100 charge injections.

Conclusion & future work

- YARR has been successfully performing module electrical QC tests with diverse commercial as well as ATLAS phase-2 PCIe FPGA-based readout boards.
- FE calibrations with YARR have been demonstrated to work without failure with multiple virtual and real electrical links.
- Next, perform data transmission tests with YARR and FELIX on a serial-powered chain, and also in a FE link-sharing configuration as in the realistic detector scenario.
- Furthermore, enhancing YARR performance for FELIX hardware by parallelization to ensure scalability and loss-less readout.



A serial-powered chain of 8 quad modules at LBNL

References

i. The ATLAS collaboration, Technical Design Report for the ATLAS Inner Tracker Pixel Detector, CERN-LHCC-2017-021 (2017), https://cds.cern.ch/record/2285585.
ii. The ATLAS TDAQ collaboration, FELIX: the Detector Interface for the ATLAS Experiment at CERN, EPJ Web of Conferences 251, 04006 (2021), https://doi.org/10.1051/epjconf/202125104006.
iii. The ATLAS collaboration, Expected Size and Readout Rate of the Data of the ATLAS ITk Pixel Detector, ATL-ITK-PUB-2022-001 (2022), https://cds.cern.ch/record/2800852.
iv. The ATLAS collaboration, The Opto-electrical conversion system for the data transmission chain of the ATLAS ITk Pixel detector upgrade for the HL-LHC, ATL-ITK-PROC-2021-003 (2022), https://cds.cern.ch/record/2773360.
v. Timon Heim, YARR - A PCIe based readout concept for current and future ATLAS Pixel modules, J. Phys.: Conf. Ser. 898 032053 (2017).

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