Tests of the Prototype Peripheral Electronics Board for the High Granularity Timing Detector

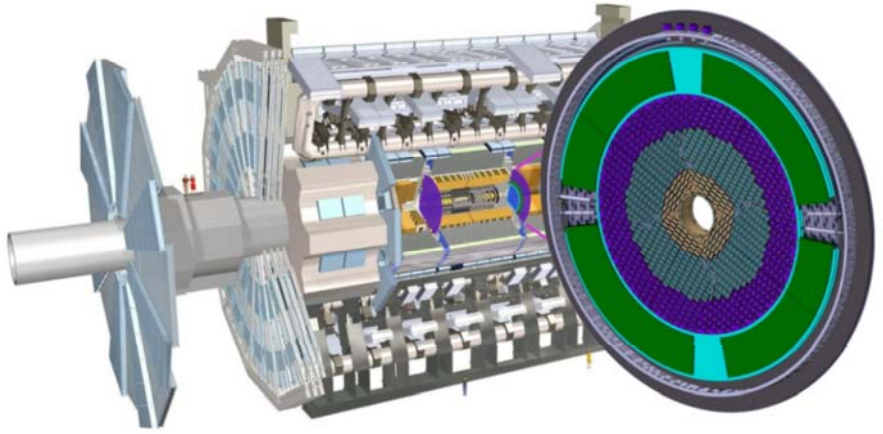
April, 2024

TWEPP 2024

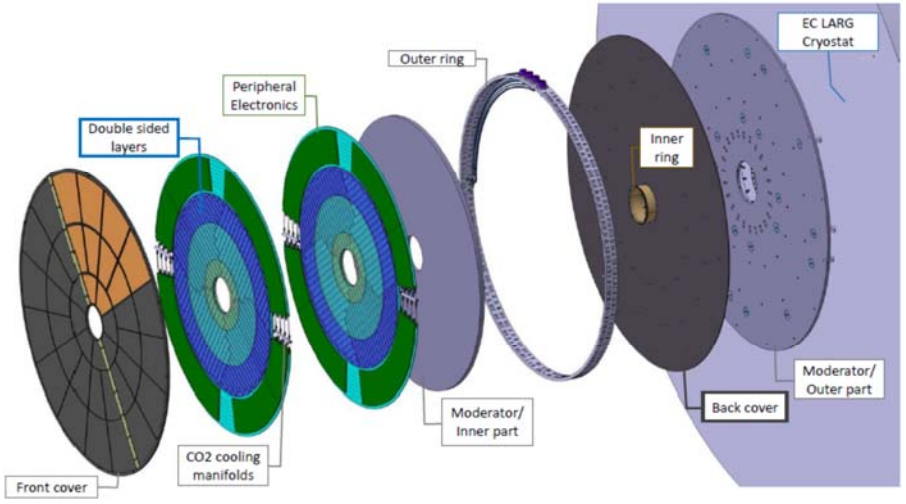
Introduction

■ HGTD

The large increase of pileup is one of the main experimental challenges for the High Luminosity LHC project (HL-LHC) physics program. A High-Granularity Timing Detector (HGTD) is proposed for the ATLAS Phase-II upgrade to provide an accurate measurement of the time of the tracks in order to mitigate the effect of the pile-up in the object reconstruction.



Position of the HGTD within the ATLAS Detector



Global view of the HGTD

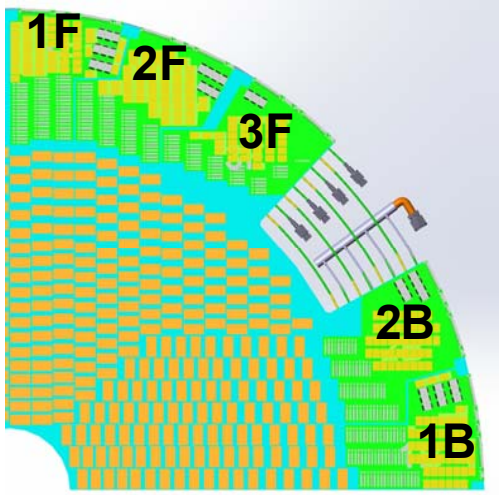
Introduction

■ Peripheral Electronics Board (PEB)

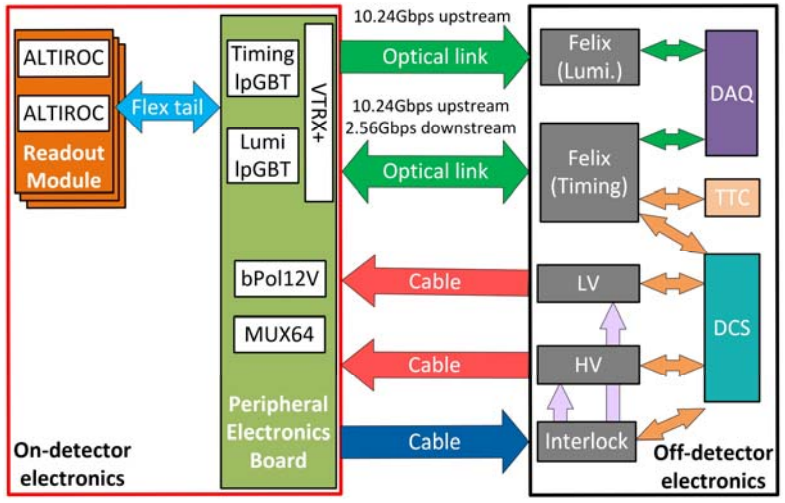
PEB acts as a bridge between the front-end modules and the off-detector electronics. According to the different read-out rows, six types of PEB boards are needed for a layer quadrant but are identical between quadrants.

Basic functions of PEB:

- Control, monitoring & data aggregation and transmission
- Power-supply distribution: LV & HV
- Thermistor connection between the front-end modules and the interlock system



One quadrant of the HGTD
6 types of PEB: 1F, 2F, 3F, 1B, 2B, 3B(back side)



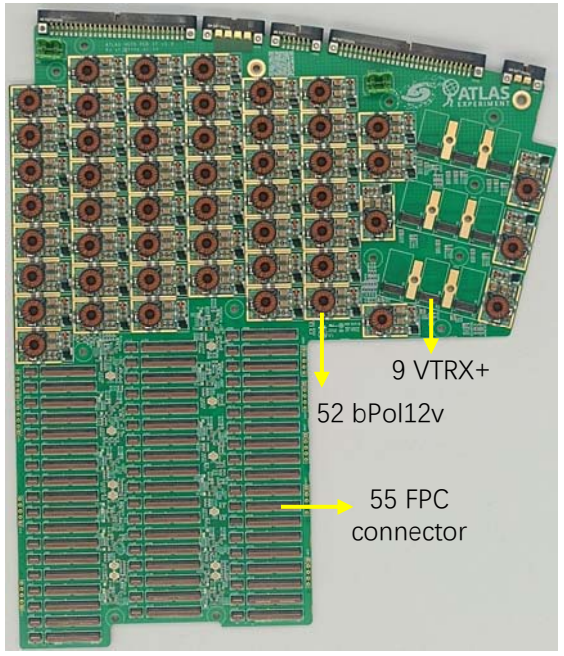
HGTD electronics architecture

Prototype Peripheral Electronics Board (1F)

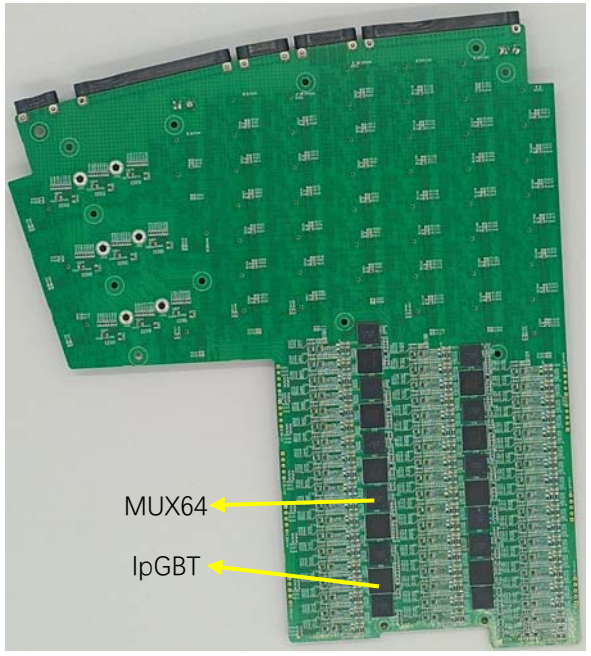
PEB	Modules	lpGBT	MUX64	bPOL12v	VTRx+
1F	55	9+3	9	52	9

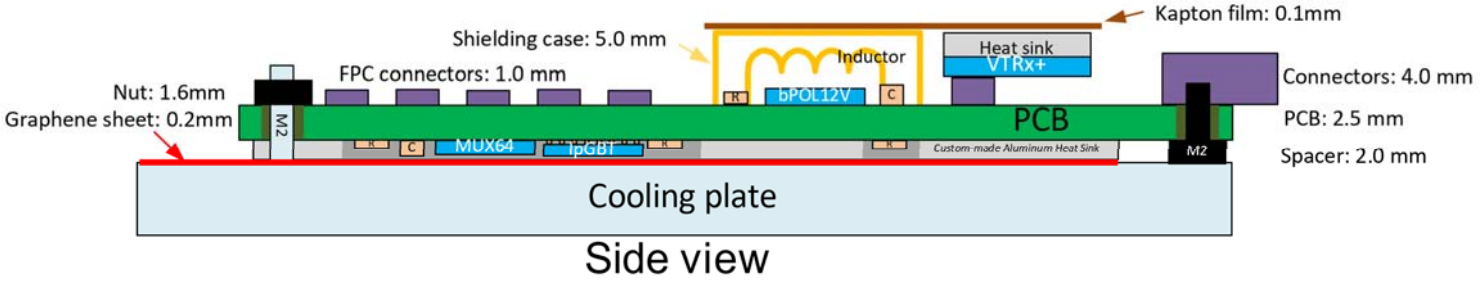
- Key dimensions
  - PCB thickness: 2.5 mm
  - 55 FPC connectors
    - Center to center distance: 6.5 mm
  - 52 bPOL12v power blocks
    - Size: 24 mm x 14.5 mm
    - Height above PCB: 5 mm
    - Height under PCB: 2 mm

Front side



Back side



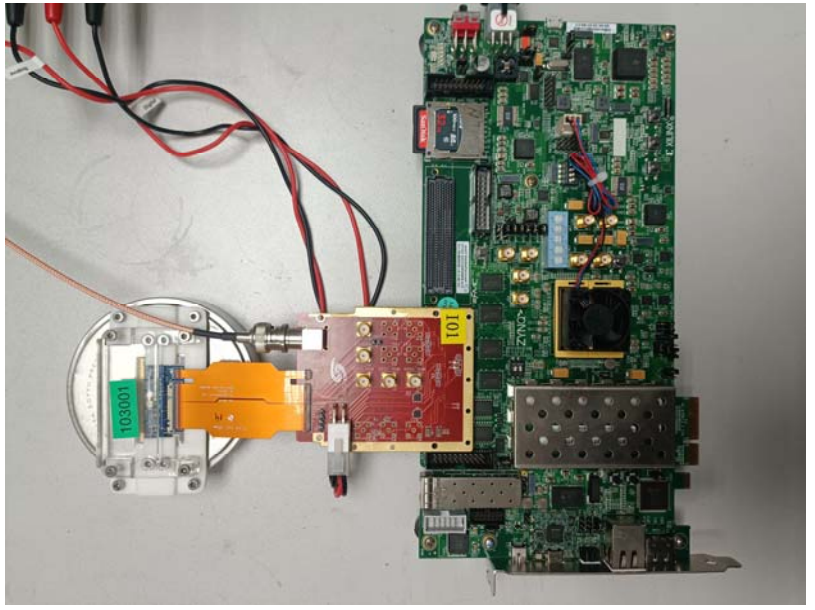


Side view

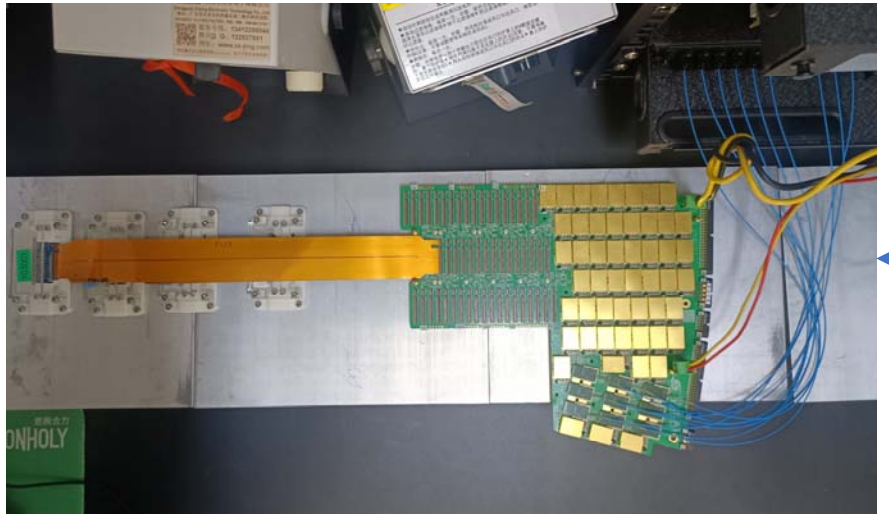
Tests of PEB 1F

Test setup

- FLEIX card: DAQ system with 24 GBT channels
- PEB 1F: connected with FELIX card via optical links
- Front-end modules: ALTIROC3 modules connected with PEB 1F via flexible PCB
- ZC706 can only support 1 ASIC (ASIC0)

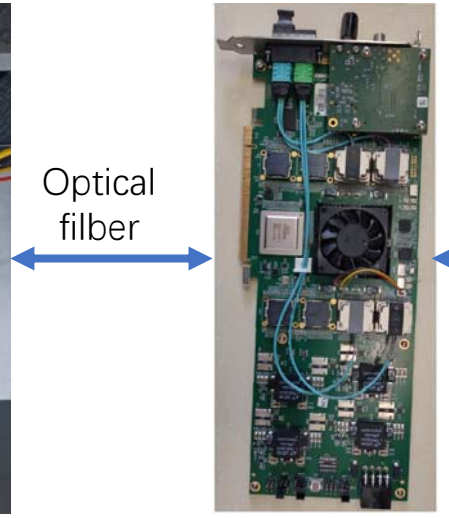


ZC706 test setup



Front-end modules

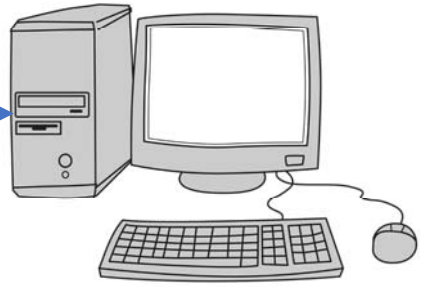
PEB 1F



Optical filber

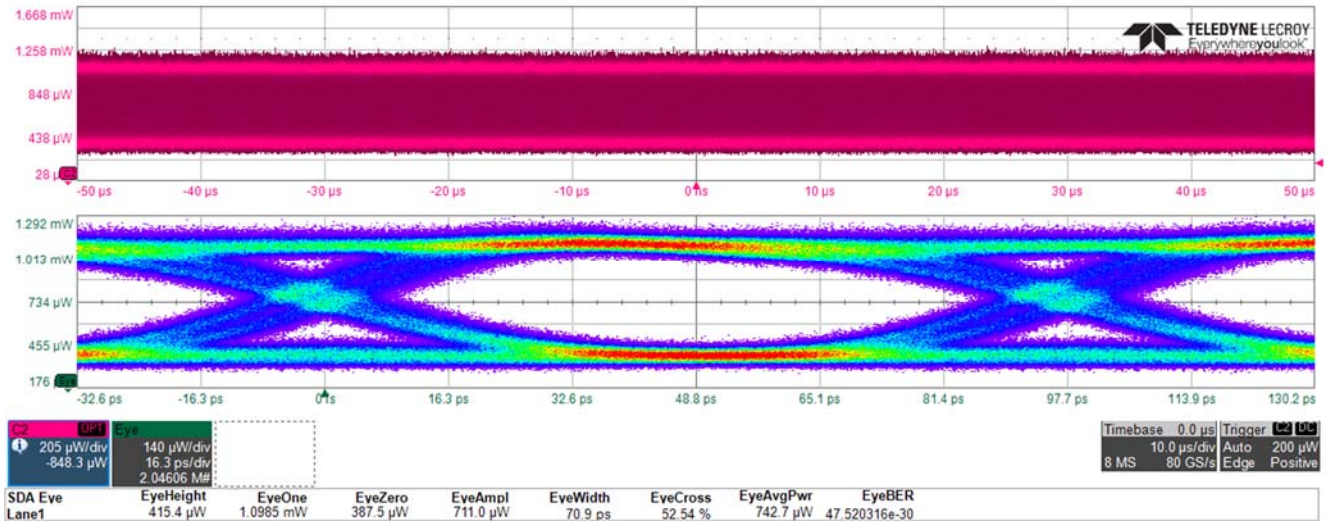
FELIX card

PCIE

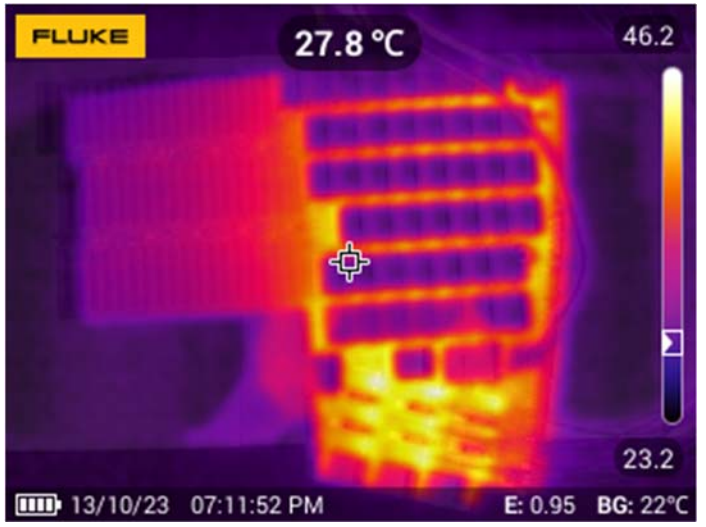


Server

Some Tests Results of PEB 1F

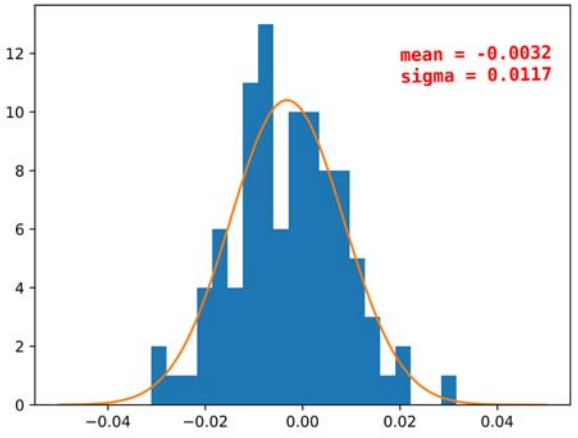


Optical eye-diagram test for 10.24 Gbps up link data transmission



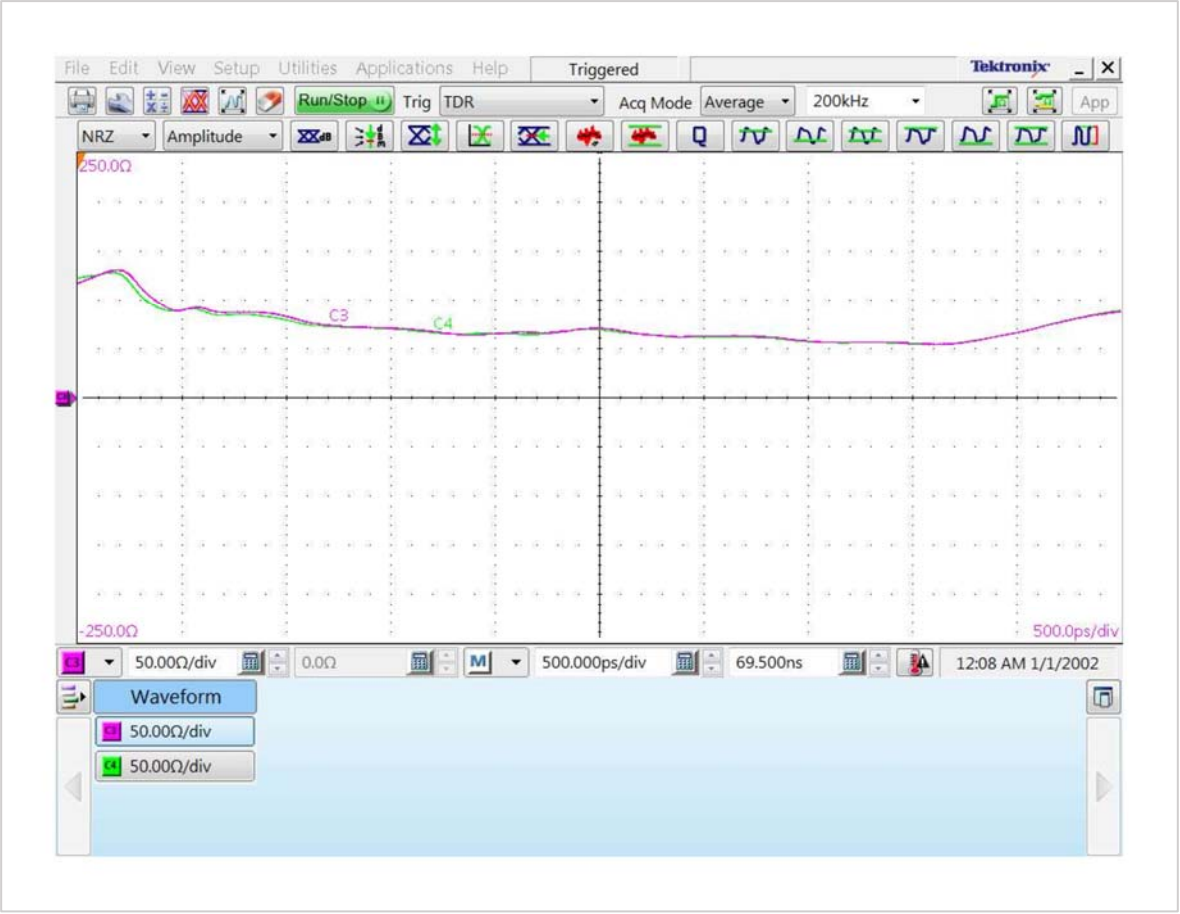
Heat test

Jitter and skew test for the PEB 1F output clock

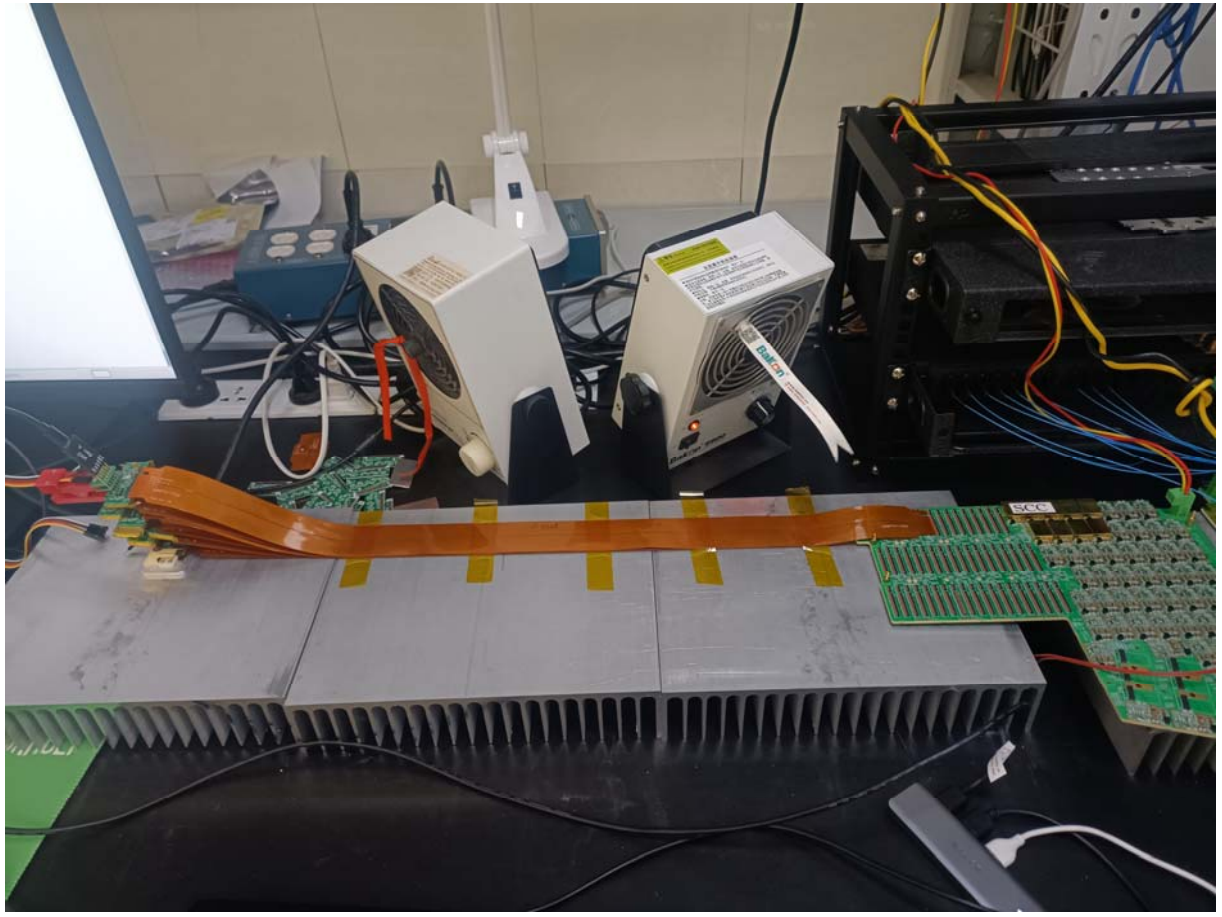


Power check: the distribution of the deviation (%) of the bPol12V output

Some Tests Results of PEB 1F



Time-domain reflectometry test for the longest 10.24Gbps path



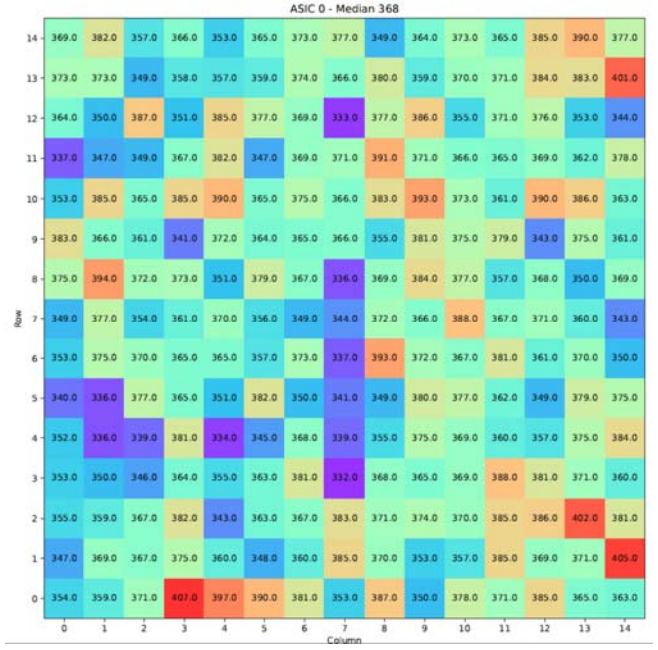
Cross talk check for the stacked flexible PCB

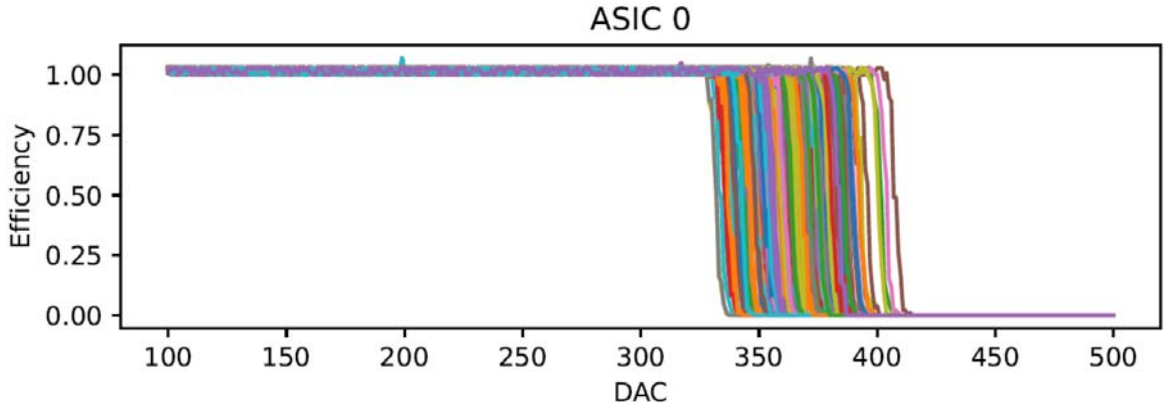
Some Preliminary Scan Results

- Module number: 103008
- HV = -70V
- M_VDDA = 0.87V
- M_VDDD = 0.85V
- Q injected: 4 fC

Some Preliminary Scan Results

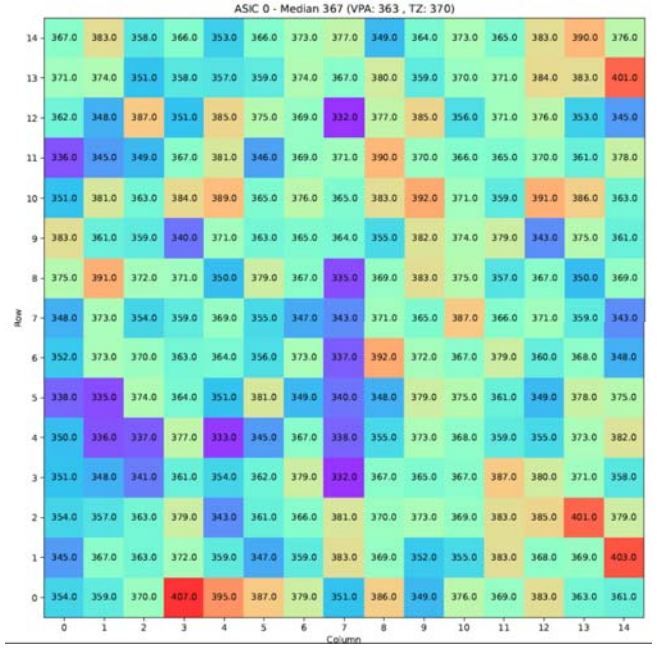
Module scan—PEB 1F

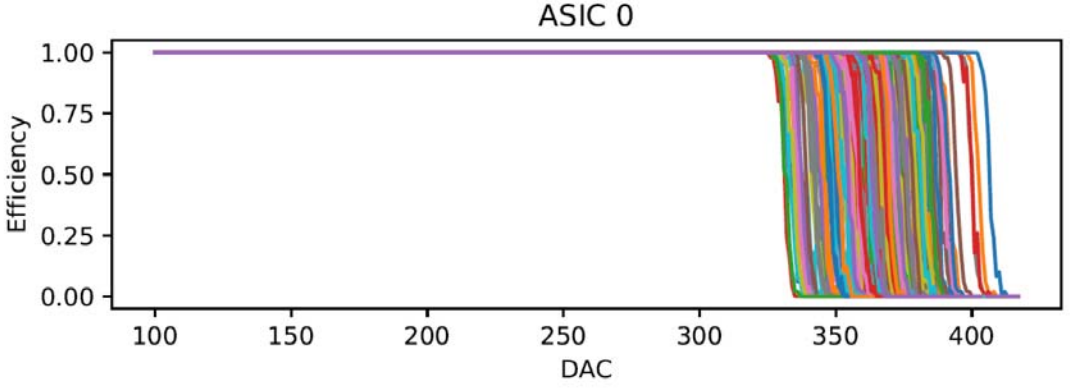




Vth scan

Module scan—ZC706

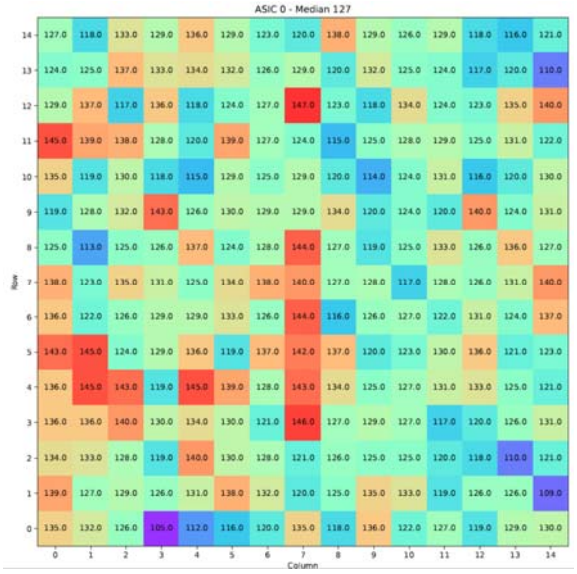


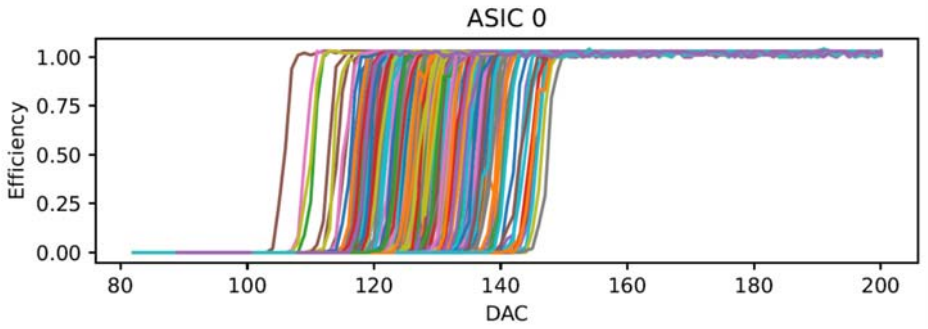


Vth scan

Some Preliminary Scan Results

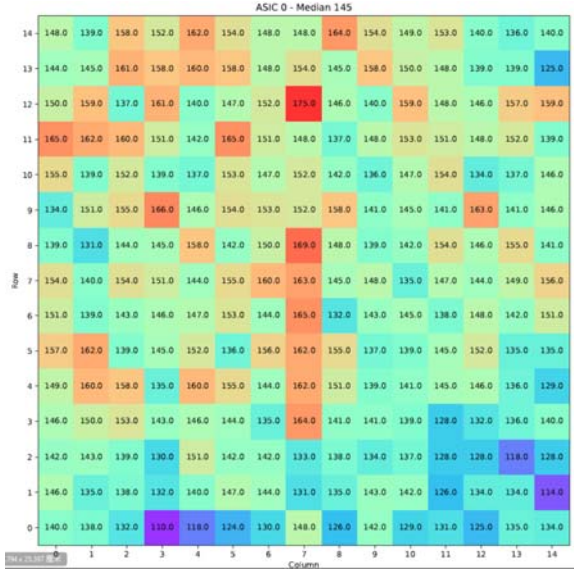
Module scan—PEB 1F

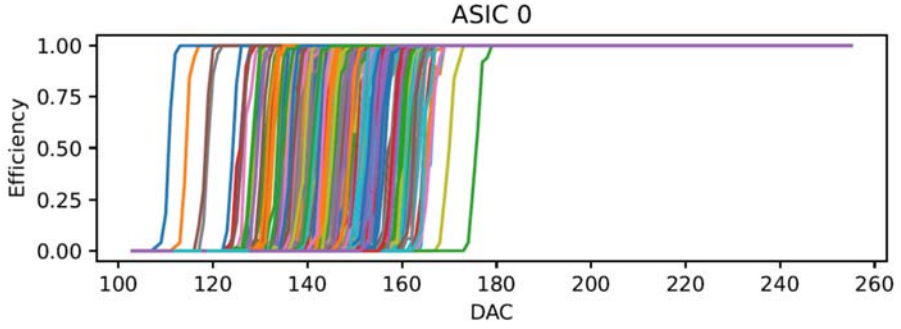




Vthc scan

Module scan—ZC706

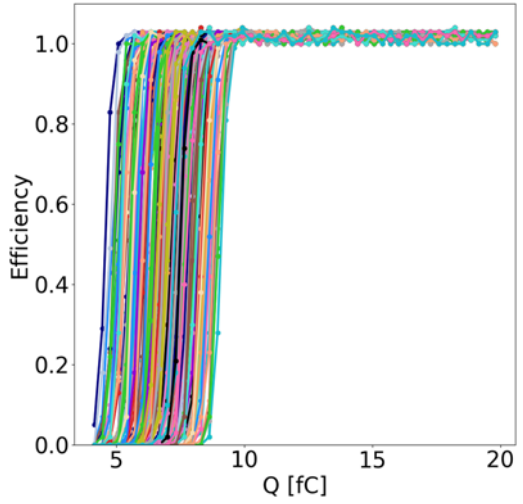


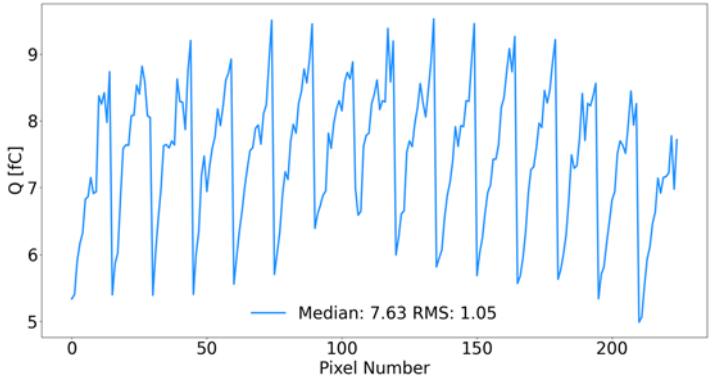


Vthc scan

Some Preliminary Scan Results

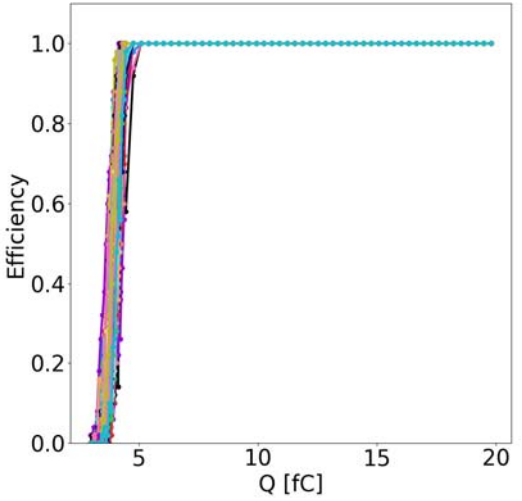
Module scan—PEB 1F

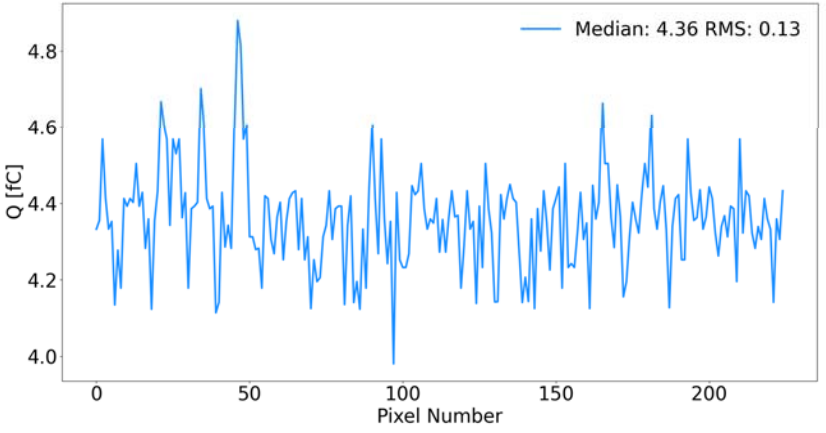




Charge scan

Module scan—ZC706

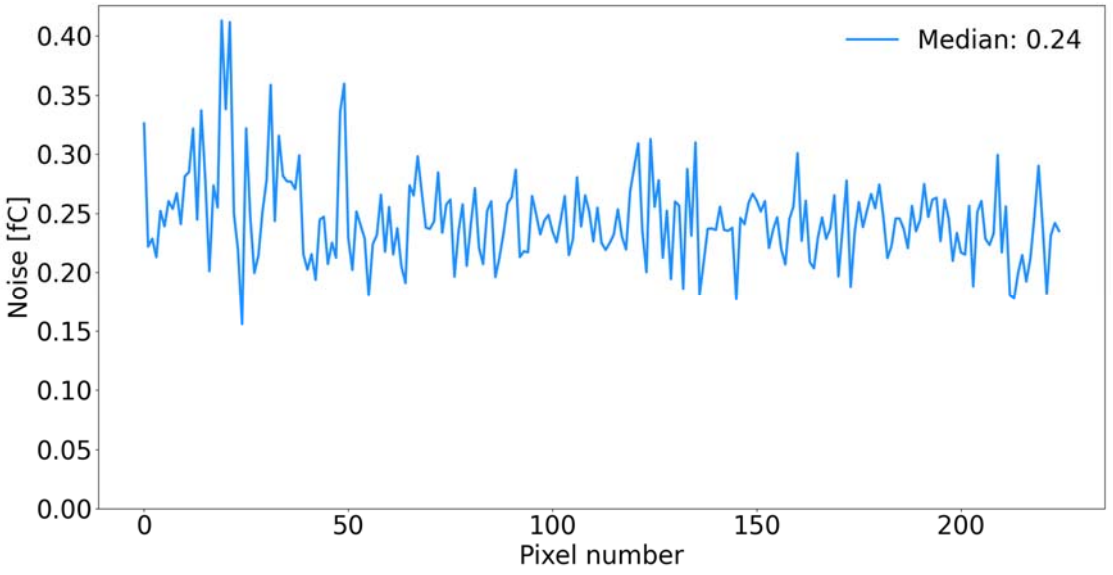




Charge scan

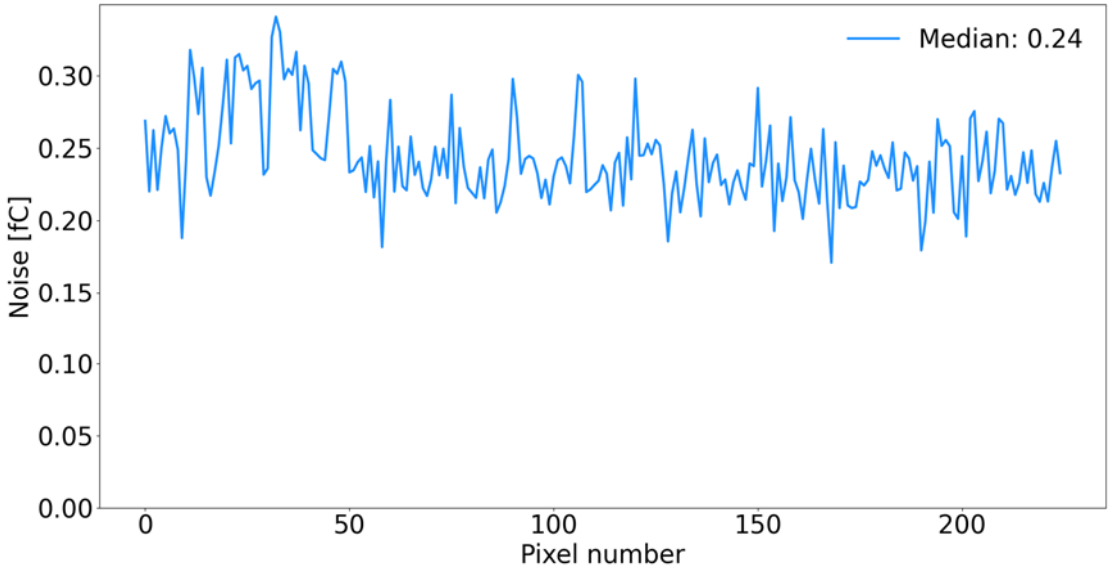
Some Preliminary Scan Results

- **Module scan—PEB 1F**



Noise

- **Module scan—ZC706**



Noise

The End