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Tests of the Prototype Peripheral Electronics Board for the High Granularity Timing Detector

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Introduction

- The High Granularity Timing Detector[1](HGTD) is proposed as a part of the ATLAS Phase-II upgrade to mitigate the impact of pileup on object reconstruction by precisely measuring the time of tracks.
  - ➢Time resolution target
    - 35-70 ps/hit up to 4000 fb^{-1}, 30-50 ps/track
  - ➢Luminosity measurement
    - Goal for HL-LHC: 1% luminosity uncertainty
  - ➢Detector position
    - Two end-caps located at ± 3.5m from IP in Z
    - Total radius: 11 cm < R < 100 cm
  - ➢Active region
    - Pseudo rapidity coverage: 2.4 < |η| < 4.0
    - Radial extension: 12 cm < R < 64 cm
  - ➢Radiation hardness
    - Up to 2.5 x 10^{15} neq/cm^2, 2 MGy TID

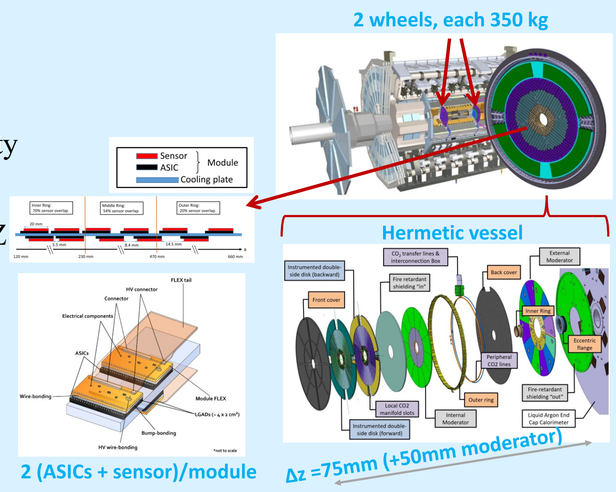

Figure 1. High Granularity Timing Detector (HGTD)

- HGTD Electronics
  - ➢8032 front-end modules with 3.6 M channels
    - Each module consists of two Low Gain Avalanche Detectors (LGADs) bump-bonded to two ATLAS LGAD Timing Integrated Read-Out Chips[2] (ALTIROC), used to measure the track timing and beam luminosity.
  - ➢A flexible PCB (flex tail) is used to connect the front-end module with the Peripheral Electronics Boards (PEB)
  - ➢The connections between on-detector and off-detector electronics are performed via optical fibers and cables.
  - ➢The optical fibers provide shared data streams for Timing Trigger Control (TTC), Detector Control System (DCS) and Data Acquisition System (DAQ).

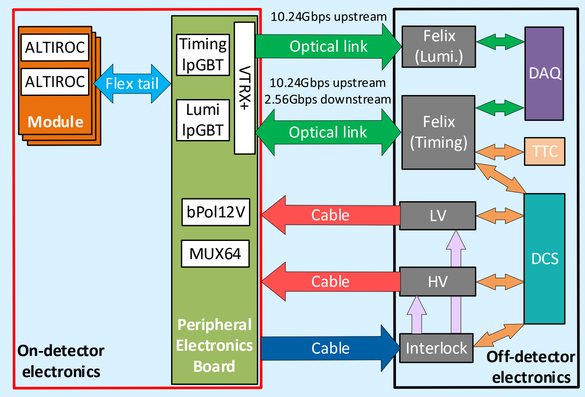

Figure 2. Schematic of the HGTD electronics

Tests of PEB

Basic functions of PEB

- PEB acts as a bridge between the front-end modules and the off-detector electronics.
  - ➢Control, monitoring
  - ➢data aggregation and transmission
  - ➢Power supply distribution: LV & HV
  - ➢Thermistor connection between the front-end modules and the interlock system

Testing with single board (PEB 1F)

- Time Domain Reflection (TDR) analysis @10.24 Gbps.
  - ➢Satisfying the requirement of 50 ohm impedance matching
- Clock jitter and skew.
  - ➢Jitter @TIE (Time Interval Error) < 10 ps at 320 MHz
  - ➢The phase difference between clock and data < 0.5 ns
- bPol12V output deviation from the designed value.
  - ➢Less than 4% at the 99.7% confidence level when the output is set as 1.2V, obtained from 44 bPol12V without load, which will be considered in bPol12V output settings to satisfy the input voltage requirement for the front-end module.
- BERT @ 1280 Mbps with multi-stacked flex tails.
  - ➢BERT < 10^{-12}
- Reliability testing with full loads
  - ➢54 thermal emulators were used as loads for PEB 1F
  - ➢Total power: ~247W
  - ➢:Thermal cycle: -40℃ ~ 70℃
  - ➢Pass more than 100 thermal cycles

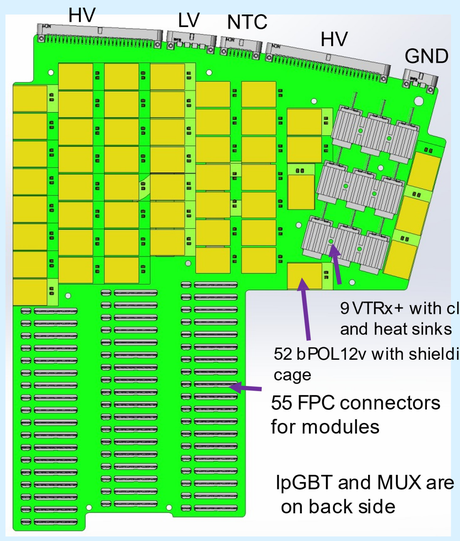

Figure 3. Top view of PEB 1F

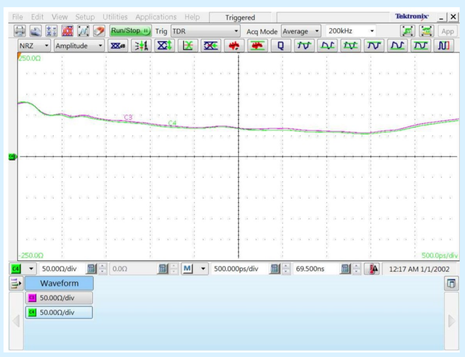

Figure 4. TDR measurement for the longest path with 10.24 Gbps

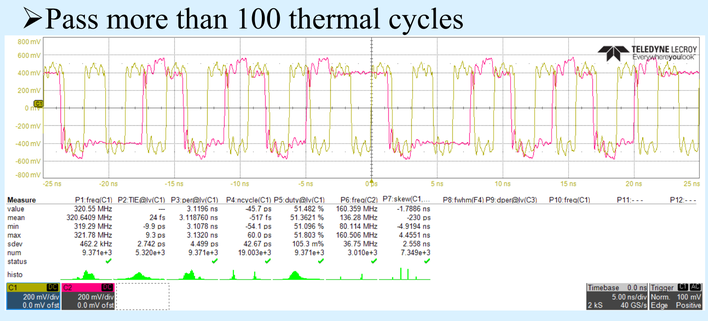

Figure 5. Clock jitter and skew measurement.

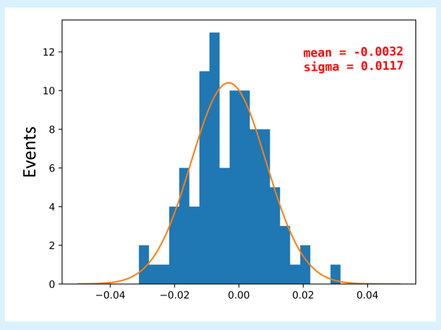

Figure 6. bPol12V output deviation

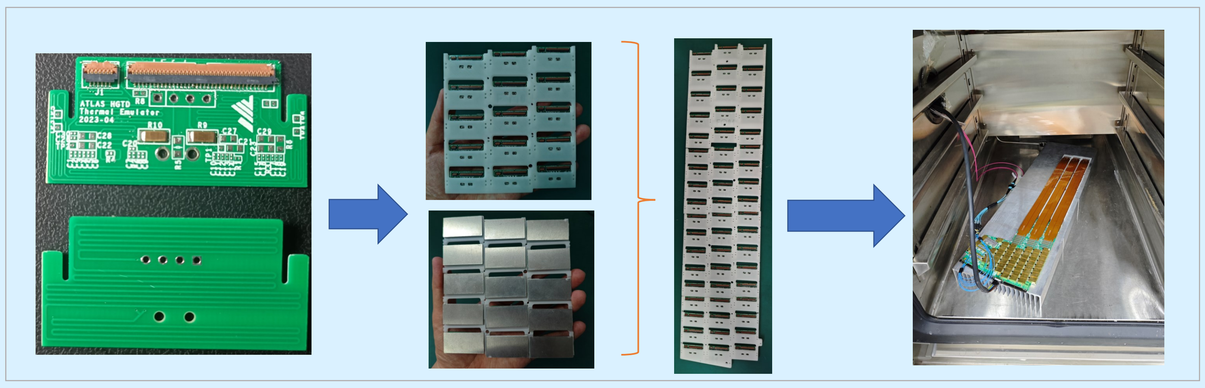

Figure 7. Reliability testing for PEB 1F

Testing with Demonstrator at CERN

- Demonstrator
  - ➢A system with full chain from front-end module to DAQ server
  - ➢Including PEB 1F + 42 modules in 3 columns + Flex tails + LV/HV + cooling
- Single module test bench
  - ➢ A Framework for ALTIROC Data Acquisition [3] (FADA)
  - ➢Including a dedicated firmware and a lot of scripts running at ZC706 board
  - ➢The test results from the single module test bench are used for comparison

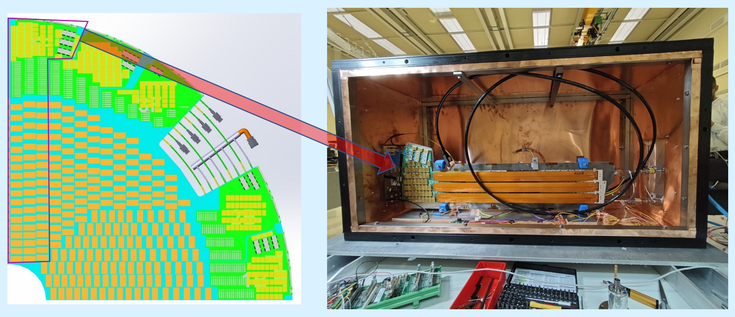

Figure 8. HGTD Demonstrator at CERN

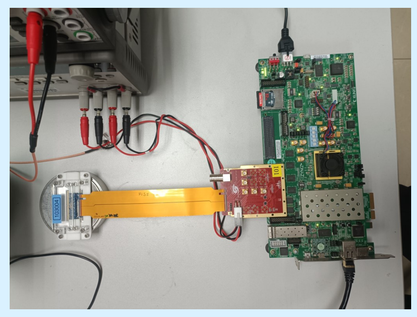

Figure 9. Single module test bench

- High Speed signal transmission performance
  - ➢Do optical eye diagram scanning to determine the optimal pre-emphasis settings for lpGBT

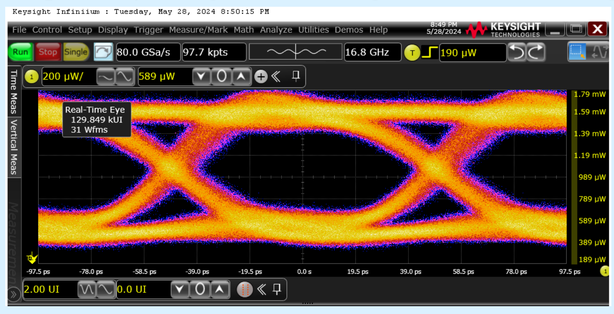

Figure 10. Optical eye diagram

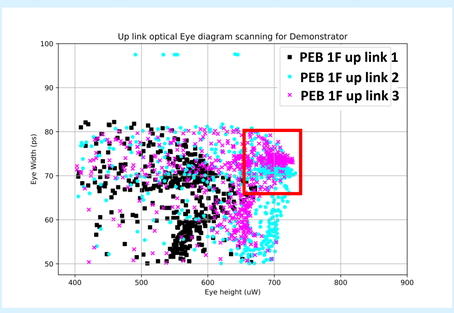

Figure 11. Optimal range for pre-emphasis settings

- Performance comparison between demonstrator and single module test bench
  - ➢No significance difference in noise level
  - ➢The noise level of the demonstrator is lower at low temperature

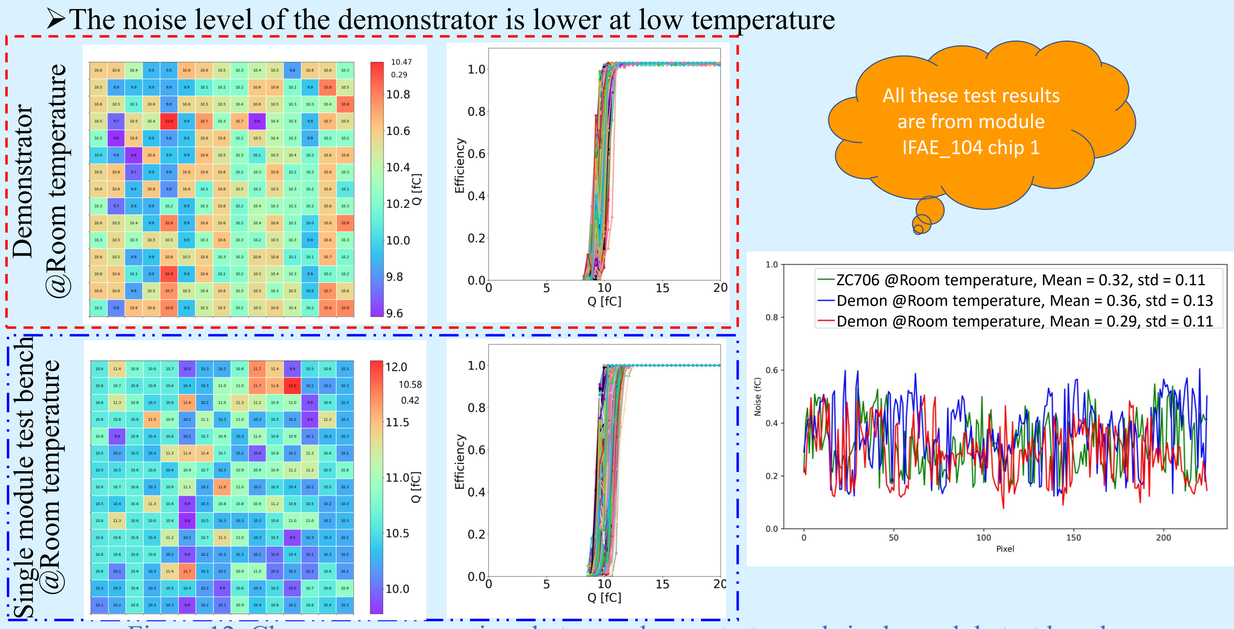

Figure 12. Charge scan comparison between demonstrator and single module test bench
(left) Threshold of 225 pixels; (middle) Charge S-curve; (right) Noise level obtained from S-curve fitting

Conclusion and outlook

We present the test results of PEB 1F, including single board test, full system test and also some comparison test with the single module test bench. These test results indicates that the designed and produced PEB 1F satisfy specifications. Through the comparison test results, it shows that the PEB does not introduce additional noise significantly. The noise scanning test at different temperature reveals that the lower the temperature, the lower the noise level. All these test results provide valuable experience for later PEB design and also for other systems.

Reference

[1] ATLAS Collaboration, Technical Design Report: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade, ATLAS-TDR-031.

[2] R. C. Mohr et al., ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS, presented at TWEPP 2019.

[3] FADA project, atlas-hgtd / Electronics / FADA · GitLab (cern.ch)