Contribution ID: **116** Type: **Poster**

Tests of the Prototype Peripheral Electronics Board for the High Granularity Timing Detector

To mitigate the impacts of pileup caused by luminosity increase in the ATLAS Phase-II upgrade, the High Granularity Timing Detector (HGTD) is proposed to measure the timing of tracks precisely. The Peripheral Electronics Board (PEB) is an important part of the HGTD, which acts as a bridge between the front-end modules and the off-detector electronics. We have designed and produced a prototype PEB board, named PEB 1F. Our tests, especially the comparative testing between the PEB 1F and a dedicated front-end module test setup based on a commercial evaluation board (ZC706), will fully evaluate the performance of the PEB 1F.

Summary (500 words)

The large increase in pileup is one of the main experimental challenges for the High Luminosity LHC project (HL-LHC) physics program. A powerful new way to mitigate the effects of pileup is to use high-precision timing information to distinguish between collisions occurring close in space but well-separated in time. A High-Granularity Timing Detector (HGTD), based on low-gain avalanche detector technology, is therefore proposed for the ATLAS Phase-II upgrade. The detector is located in the gap region between the barrel and the end-cap calorimeters. It improves the forward object reconstruction.

The Peripheral Electronics Board (PEB) is an important part of the HGTD, which acts as a bridge between the front-end modules and the off-detector electronics. According to the different read-out rows, six types of PEB boards are needed for a layer quadrant but are identical between quadrants. One PEB board receives the data of up to 55 modules. It encodes, aggregates, and transmits them via optical links to the off-detector electronics. The data rate of each link is up to 10.24 Gbps. In the downlink direction, the board transmits the trigger commands and clock to the front-end modules. Additionally, this board distributes the DC voltage to all front-end modules using DC-DC regulators and the High Voltage to the sensors. The board also handles voltage and temperature monitoring, and parameter setting in the front-end module for the detector control system.

After about two years of pre-research and experimental study, a prototype PEB board, named PEB 1F, was designed and produced at the end of 2023. This board has approximately 400 cmˆ2 layout area and 2.5 mm thickness divided into 22 layers. 82 chips and 55 FPC connectors are placed on the surface of the board. High-density interconnectors are used to route about 4000 nets and 13000 connections.

To fully evaluate the performance of the PEB design, a lot of tests have been performed, such as power check, communication test, time-domain reflectometry test, optical eye diagram test, and so on. These tests belong to PEB self-test, revealing the basic function of the PEB. The PEB joint tests with FELIX card and front-end modules are ongoing, including timing data readout tests, various S-curve scanning tests for the front-end modules, PEB noise tests, and so on. The test results are compared to the results from a dedicated front-end module test setup based on a commercial evaluation board (ZC706) to understand the effect of the PEB on the whole detector system. Further, make improvements in later designs.

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Track Classification: Module, PCB and Component Design