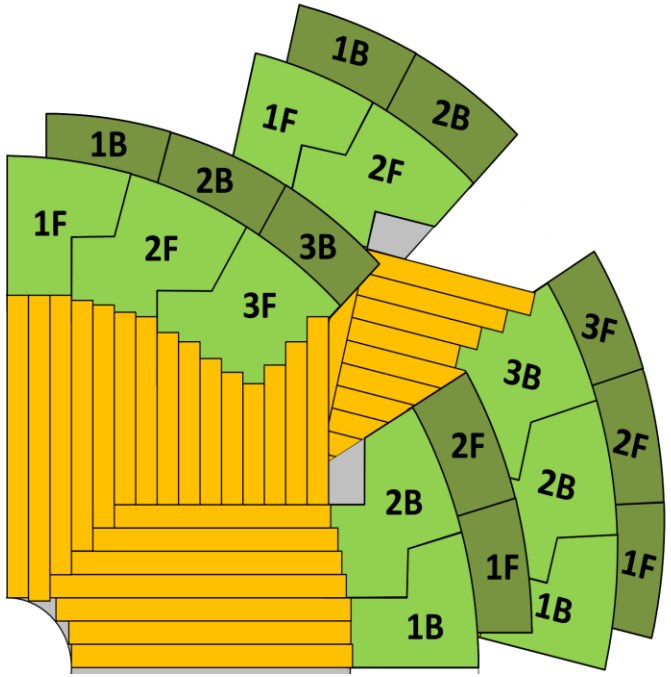
The Prototype of the Peripheral Electronics Board - a Component of the HGTD In-detector Electronics for the ATLAS Phase-II Upgrade

Jie Zhang on behalf of the HGTD Electronics Team

HGTD: Peripheral Electronics Board – Scope



One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- The front-end modules are connected via flex tails, arranged in rows, to the PEB @ 660 < r < 920 mm
- Six types of PEB to be designed (front and back side)
  - Board 1F, 2F, 1B and 2B can be used both on front and back
    - According to the optimization of mirror structure for module layout
  - Each board covers three or more readout rows in order to have a similar number of modules

Number of parts

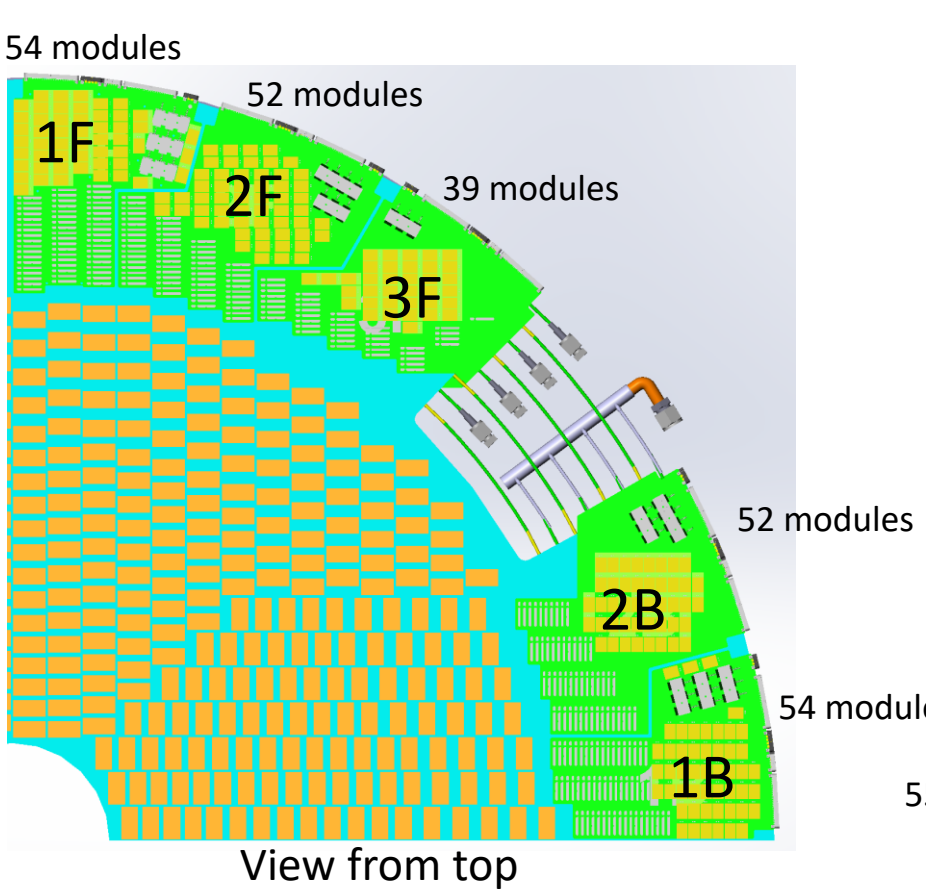
- 80 boards per HGTD vessel, thus 160 boards in total.

1F	2F	3F	3B	2B	1B
32	32	16	16	32	32

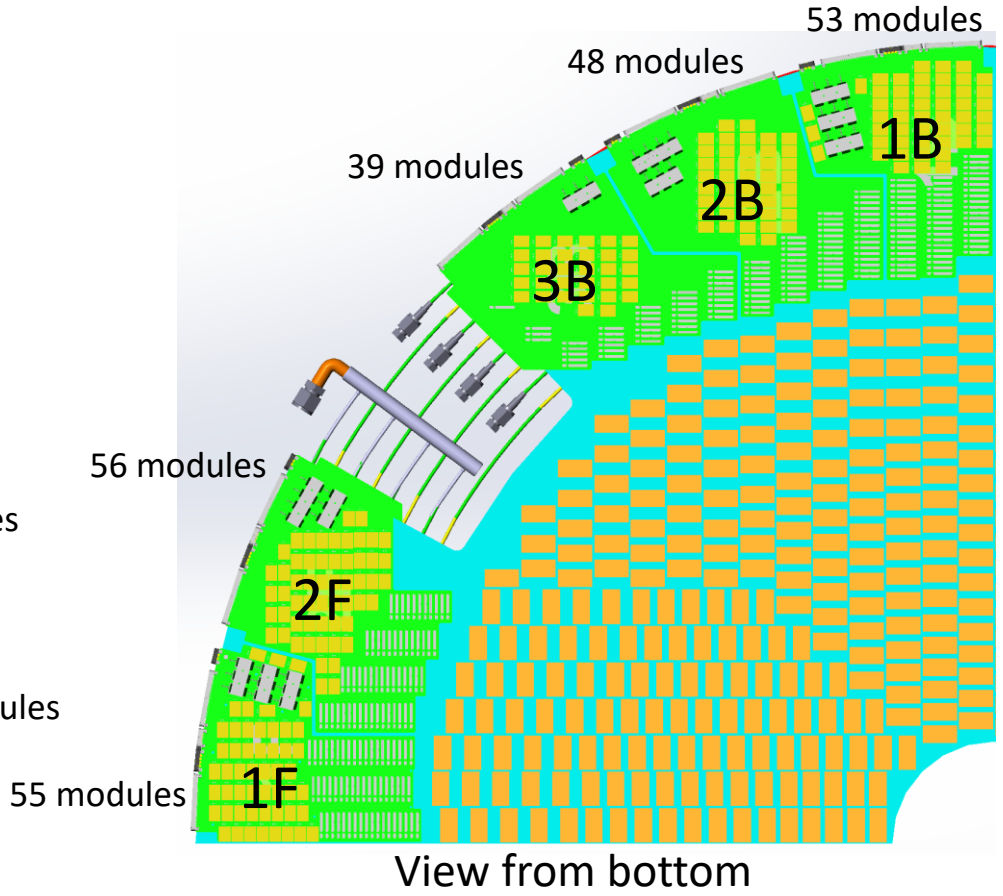
HGTD: Peripheral Electronics Board – Scope

Number of modules attached to the different PEBs at the front and back sides

PEB	Front side	Back side
1F	54 modules	55 modules
2F	52 modules	56 modules
3F	39 modules	-
3B	-	39 modules
2B	52 modules	48 modules
1B	54 modules	53 modules



View from top

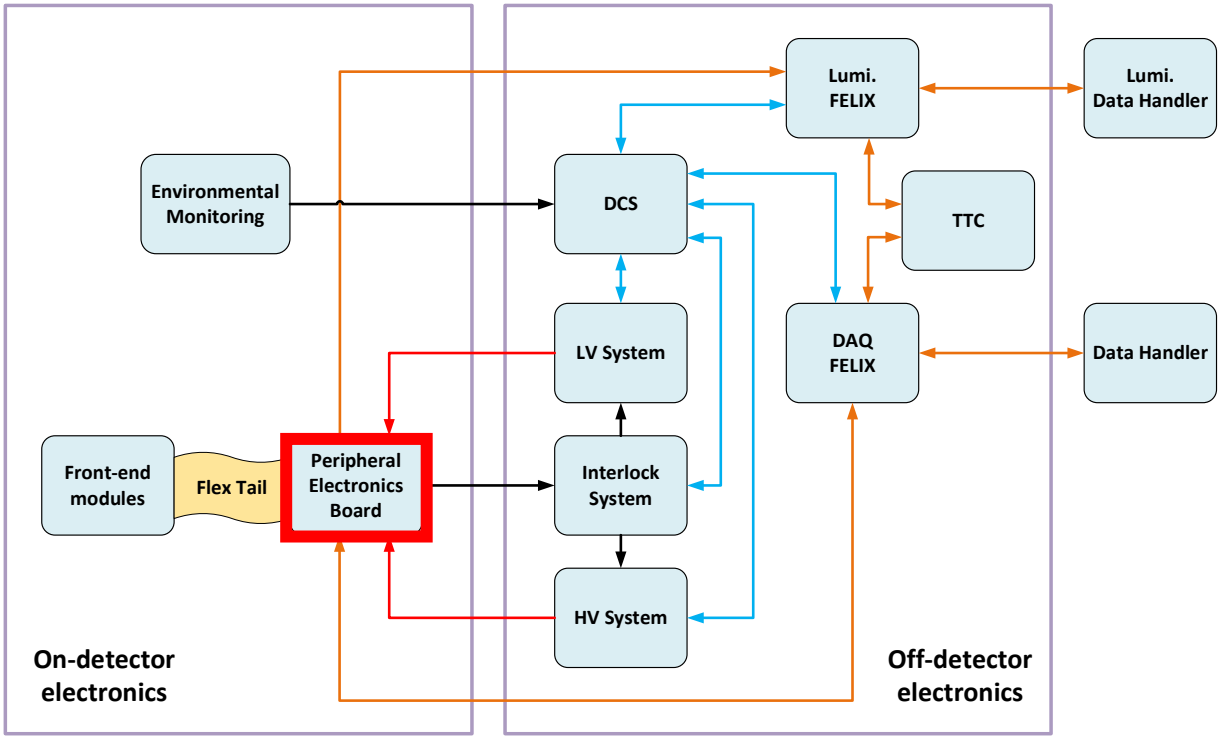


View from bottom

One quadrant of the HGTD front and back side

HGTD: Peripheral Electronics Board – Scope

- On-detector
  - Modules:
    - Module flex PCB
    - Two read-out chips(ALTIROC)
    - Two Low Gain Avalanche Sensors (LGADs)
  - Flex tail cables
  - **Peripheral Electronics Boards (PEB)**
- Off-detector
  - Data Acquisition System (DAQ)
  - Timing, Trigger and Control (TTC)
  - Detector Control System (DCS)
  - Low Voltage (LV)/High Voltage (HV) system
  - Interlock system



- Basic functions of PEB
  - Control, monitoring & data transmission
  - Power-supply distribution: LV & HV
  - Routing of temperature sensors for the interlock system

Peripheral Electronics Board – list of items

Main chips

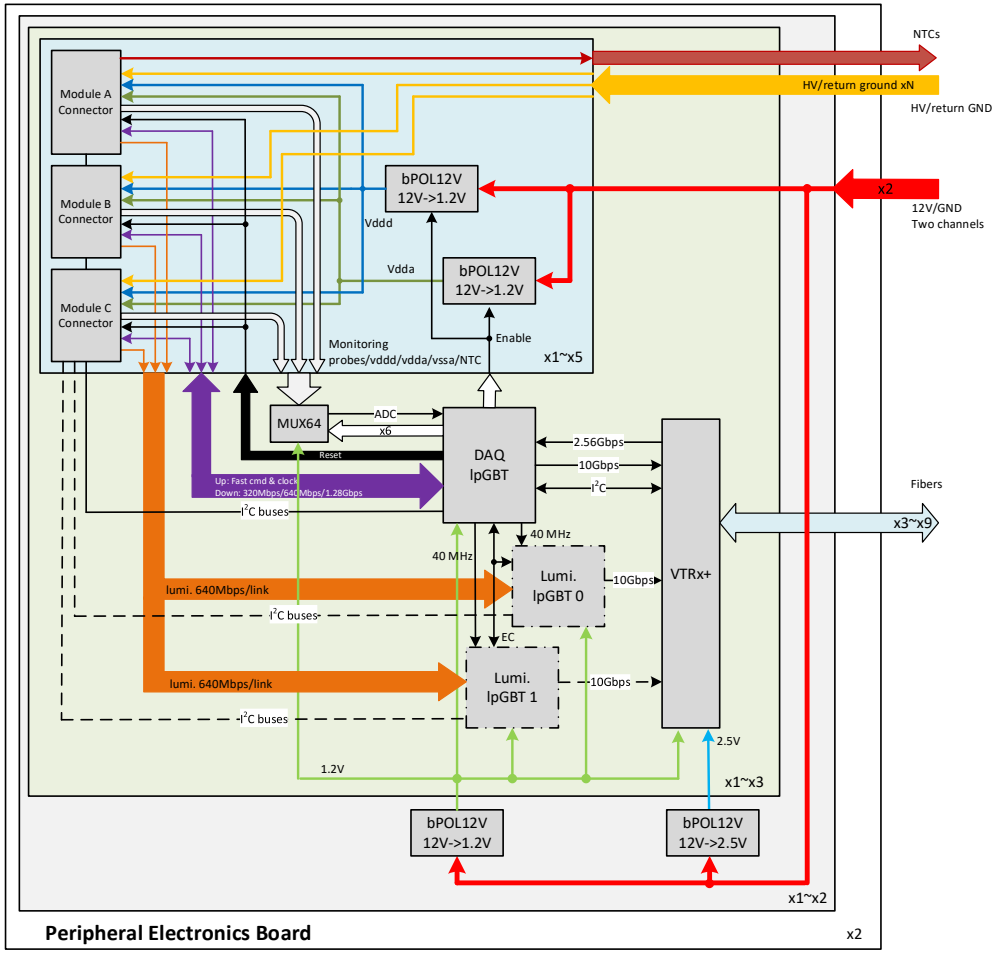
- **8.2.2.6 Monitor MUX**
  - A 64:1 multiplexer is developed by SMU to handle all voltages to be measured. Each multiplexer, which can switch the received voltages from up to 12 modules, is controlled by 6 I/O lines from one lpGBT.

From HGTD

- **8.2.2.7 DC/DC converter**
  - The peripheral electronics will contain DC-DC converters supplying the 1.2V and 2.5V required by the ALTIROC ASICs, the lpGBT ASICs and the Versatile Link.
- **8.2.2.4 lpGBT**
  - The Low Power Giga Bit Transceiver (lpGBT) is developed by CERN for the LHC upgrades. It is a radiation tolerant ASIC that can be used to implement multipurpose high speed bidirectional optical links for high-energy physics experiments.
- **8.2.2.5 VTRX+ optical transceiver**
  - The VTRX+ optical transceivers, development within the Versatile Link plus project at CERN, handle four fibers for transmission and one for receiving.

From CERN

Conceptual design of PEB



- Two LV channels
  - Each up to 12A @ 12V
- Up to 3 modules share two bPOL12v
  - One for analog power, the other for digital power
- One TDAQ lpGBT and 1~2 luminosity lpGBTs share one VTRx+
- Control
  - I2C of lpGBT
    - Module and VTRx+ configuration
    - I2C0 of TDAQ lpGBT is connected to the VTRx+ only
  - Output
    - Module reset
    - Module power on/off
    - MUX64 channel selection
- Monitoring
  - ADC of lpGBT
  - Module state monitoring
    - VDDA, VDDD, GNDA, PROBE0/1(internal state and temperature), NTC
  - PEB state monitoring
    - lpGBT voltage, temperature
    - VTRx+ RSSI(average optical power of the received light) and NTC
    - bPOL12v temperature
    - On board NTC
  - Input of lpGBT
    - bPOL12v power good signal

bPOL12V:
provide the 1.2V analog and digital voltages for the ALTIROCs

lpGBT:
Bi-directional slow control and monitoring communication between the FELIX and the lpGBT is done via the IC and EC channels.

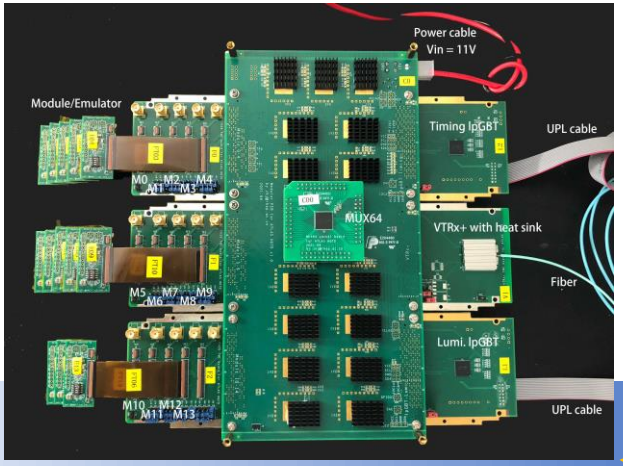
Each lpGBT has a 8 channel multiplexed ADC.
With ~7 modules/lpGBT, an external 64-to-1 MUX is required: **MUX64**

PEB Status Review - from simple to difficult

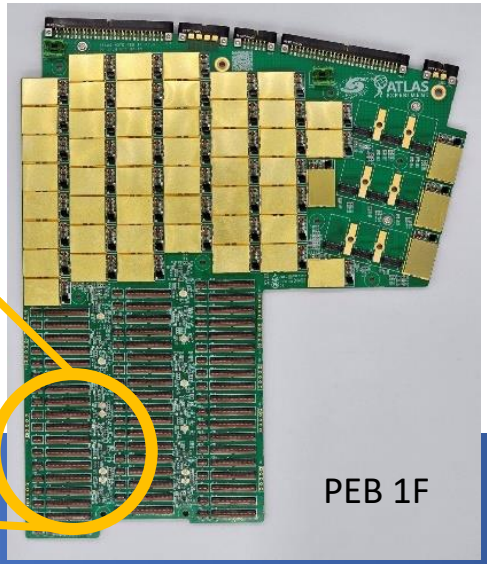
- Modular PEB
  - Start from individual test boards (Front-end module (ALTIROC), MUX64, bPOL12V, lpGBT and VTRx+)
  - To allow testing in the lab as a standalone board to verify functionality and performance separately
  - Function and performance are validated by collaborators
- PEB 1F
  - Most complex PCB in 6 types of PEB, up to 22-layer PCB
  - Process the maximum number of lpGBT in 6 types of PEB, up to 12 pcs

Site	CERN	IHEP	NJU	Nikhef	KTH	Clermont
Modular PEB	-	1	1	1	1	1
PEB 1F	1	1 + 1(under assemble)	-	-	-	-
Tasks	Demonstrator, System test	QA/QC, Reliability test	Training	TDAQ	Lumi.	Timing

Modular PEB is 1/9 group of PEB 1F



Modular PEB



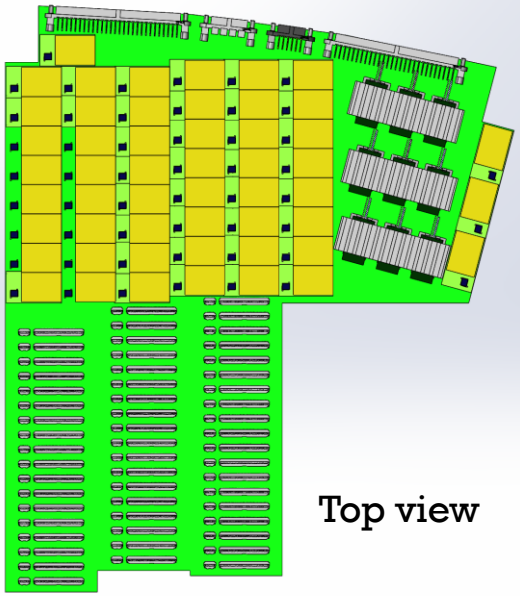
PEB 1F

PEB Status Review - from difficult to simple

Peripheral board	Modules	lpGBT	bPOL12v	MUX	VTRx+
1F	55	9+3	52	9	9

Key dimensions

- Total thickness: 9.7 mm
  - Shielding case: 5.0 mm
  - PCB: 2.5 mm
  - Spacer: 2.0 mm
  - Others: 0.1~0.2 mm
- 55 FPC connectors
  - Center to center distance: 6.5 mm
- 52 bPOL12v power blocks
  - Size: 24 mm x 14.5 mm
  - Height above PCB: 5 mm
  - Height under PCB: 2 mm

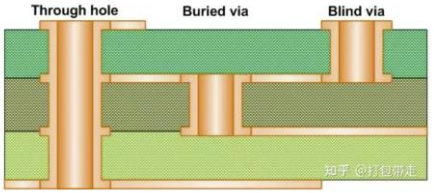


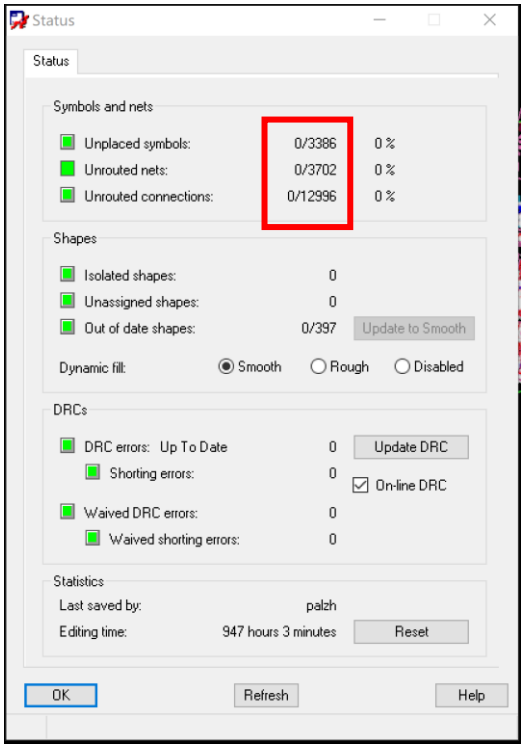
Top view

- **Other shapes: derived from this board, sharing library files, stack-up, and design specifications**

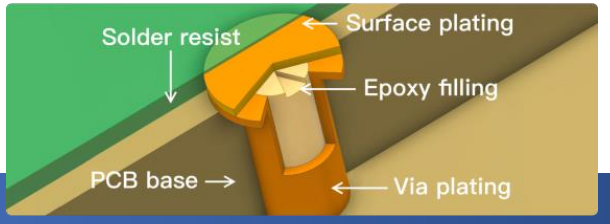
Complex PCB for PEB 1F

- High speed, low loss multi-layer material
  - Impedance control
- Halogen free
  - EM-890 or IT-170/988 or TU-883A
- Symbols and nets
  - 3386 components, 12996 connections
- 22 layers, includes:
  - 8 layers for signals
  - 2 layer for HV and HV return ground
  - 4 layers for ground
  - 8 layers for power
- HDI (High Density Interconnector)
  - Micro via

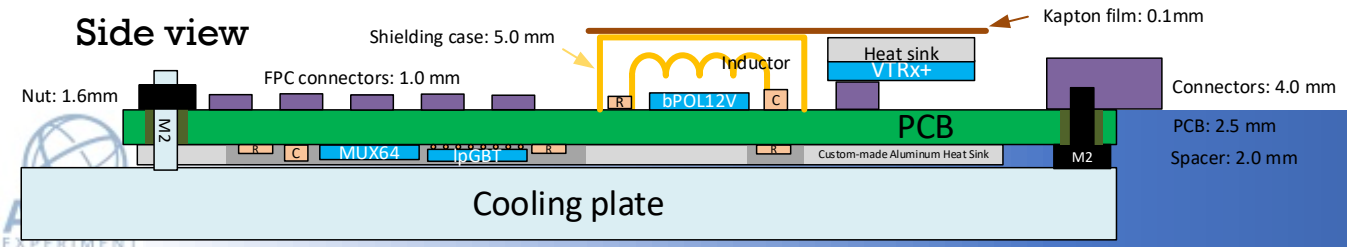




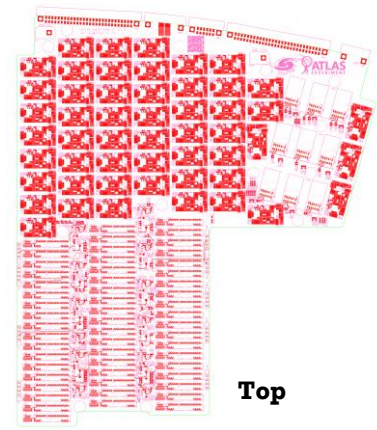
- VIPPO / POFV: Via-in-Pad Plated Over PCB



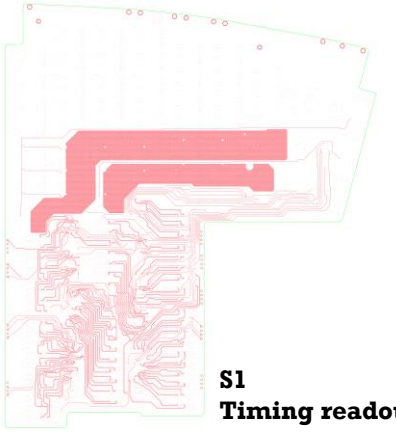
Side view



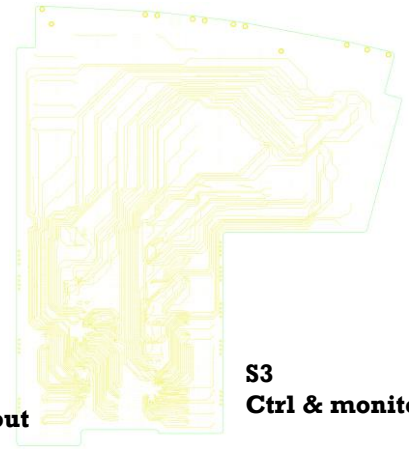
HGTD: Peripheral Electronics Board – 1F routing



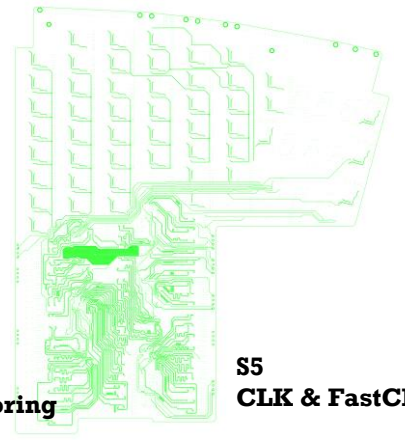
Top



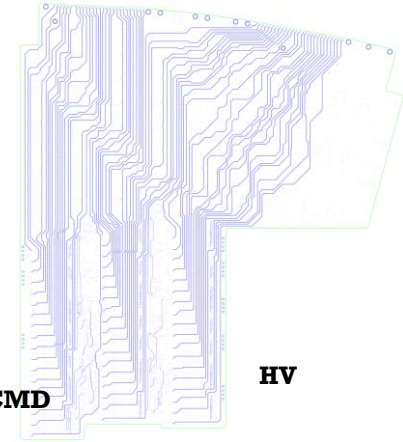
S1
Timing readout



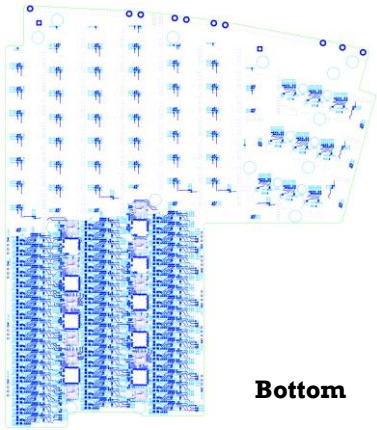
S3
Ctrl & monitoring



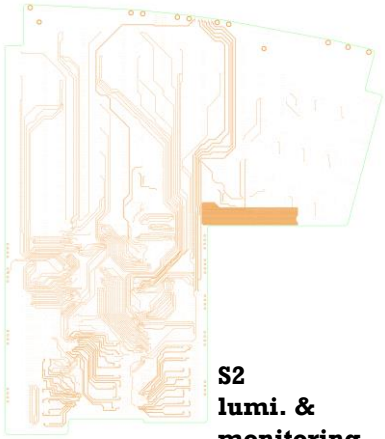
S5
CLK & FastCMD



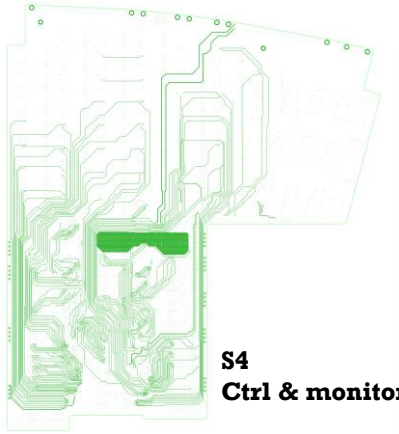
HV



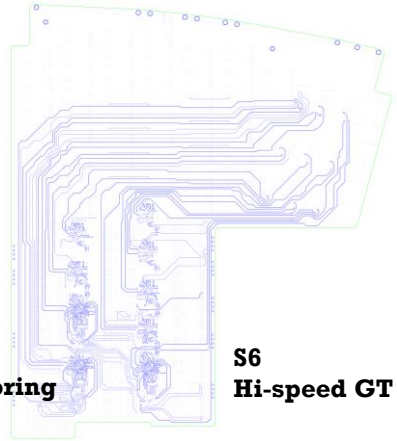
Bottom



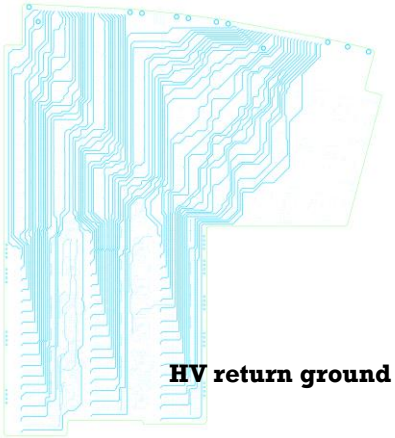
S2
lumi. &
monitoring



S4
Ctrl & monitoring



S6
Hi-speed GT



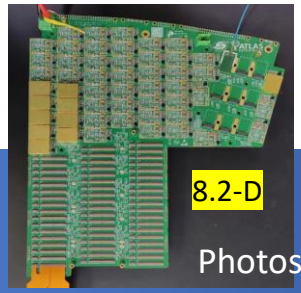
HV return ground

PEB 1F-Prototype fabrication and pre-qualification

- Highly qualified vendor to be chosen for the PCB fabrication and assembly.
  - The qualification process includes participation of the candidate vendors in the PEB prototype, and evaluation of the quality of the delivered product
  - 4 companies joined PEB 1F prototype fabrication

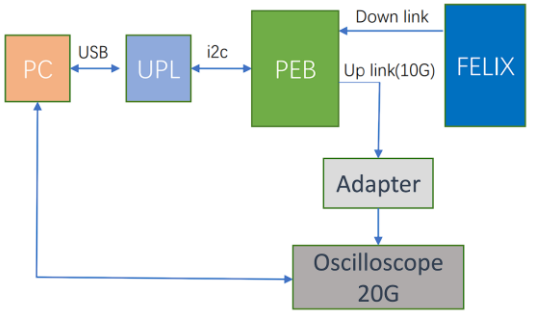
Vendor	2022 annual revenue in China (*)	PCB Material	Start date	Finish date	Fabrication time	Comment	Assembly: To verify the PCB and save the chips, only one group of each board is assembled	
8.2-D	In top20	IT-170	Sep. 27th	Nov. 20th	54 days	Failed to merge the sandwich in the first batch, alignment problem; The second batch is OK	1 group	Finished at Nov. 29th
							-	-
8.2-C	In top100	EM-890K	Sep. 15th	Dec. 13th	89 days	Failed in the first batch; The second batch is OK	1 group	Finished at Dec. 21st
							-	-
8.2-B	In top5	EM-890K	Nov. 10th	Dec. 19th	39 days	High quality, promised fabrication time	1 group	Finished at Jan. 2nd
							Full assembly	2 pcs finished at Jan. 15th One sent to CERN at Jan. 22th One kept in IHEP The third one under assemble (delay due to waiting for the inductors to arrive)
8.2-E	In top75	TU-883A	Nov. 28th	Dec. 18th	20 days	High quality, very fast, but need international transport	1 group	Finished at Dec. 27th
							-	-

*Note: https://www.eet-china.com/mp/a133351.html



Photos of PEB 1F from four manufactures

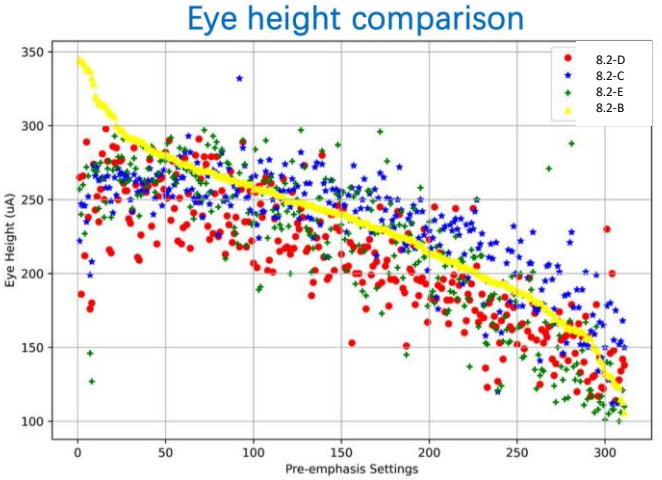
PEB 1F-Pre-qualification



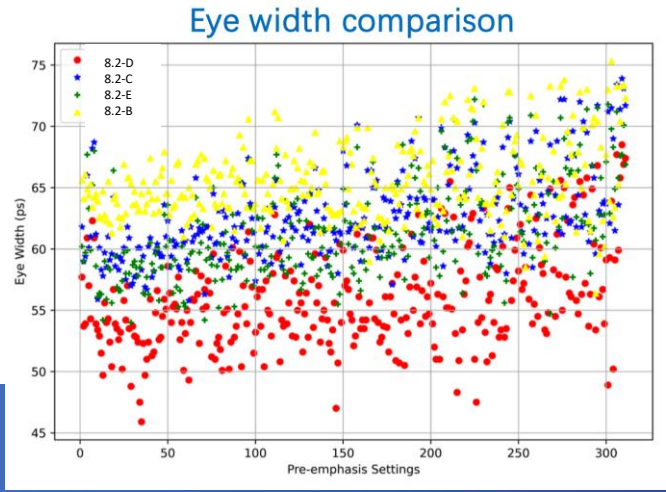
- Eye Diagram Test for 10Gbps
  - Setup
    - Use FELIX to provide down link data for lpGBT clock recovery
    - Use UPL to configure the pre-emphasis parameters of lpGBT
    - Use PC to configure Oscilloscope and record eye diagram parameters and waveforms.
    - Follow the steps below for scanning.

```
for T_modulation_current in range (47,128,3):
    for T_emphasis_enable in range (1,2):# always enable
        for T_emphasis_short in range (0,2):
            for T_emphasis_amp in range (20,101,3):

                try:
                    peb.timing.lpgbt.line_driver_setup(
                            modulation_current = T_modulation_current,
                            emphasis_enable = T_emphasis_enable,
                            emphasis_short = T_emphasis_short,
                            emphasis_amp = T_emphasis_amp
                        )
```



- Test result
  - Eye height: 8.2-B, 8.2-C are better than 8.2-D, 8.2-E
  - Eye width: 8.2-B > 8.2-C > 8.2-E > 8.2-D
  - The result is consistent with the materials used by each vendor
  - We plan to use 8.2-B as the qualified vendor
    - One of the "official" vendors from CERN,
    - Also the vendor for JUNO large PMT electronics, HEPS X-ray detector and COMET electronics in IHEP, we have years of close cooperation, built a deep relationship, accumulated rich experience

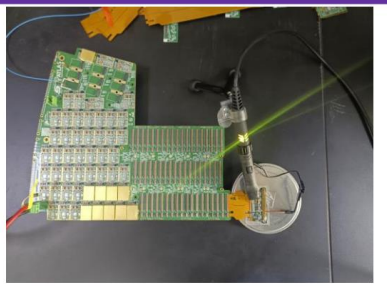


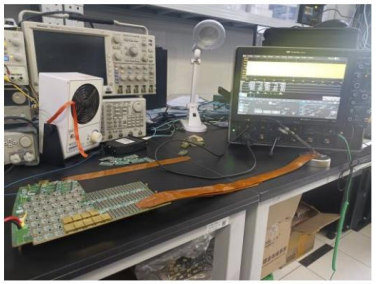
Testing-Jitter (FELIX-PEB-flex tails-module flex)

Clock Measurement on PEB 1F

❑ **Result**

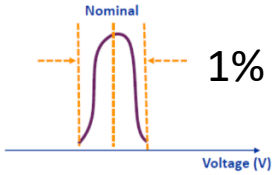
	Jitter-TIE (ps)		Duty(%)	
Length of flex tail (mm)	40M	320M	40M	320M
32.4	3.107	4.048	50.19	51.22
73.4	2.905	3.992	50.15	51.00
114.5	2.964	3.769	50.19	51.70
155.6	2.953	3.759	50.21	51.63
196.8	2.903	4.231	50.18	51.26
231.8	3.03	4.392	50.16	50.79
266.8	3.059	4.571	50.20	51.36
301.8	3.14	4.404	50.22	51.06
336.8	3.224	4.303	50.18	51.17
371.8	3.19	4.707	50.23	50.92
640.5	3.743	4.97	50.23	50.13
~700	4.222	5.359	50.22	51.10





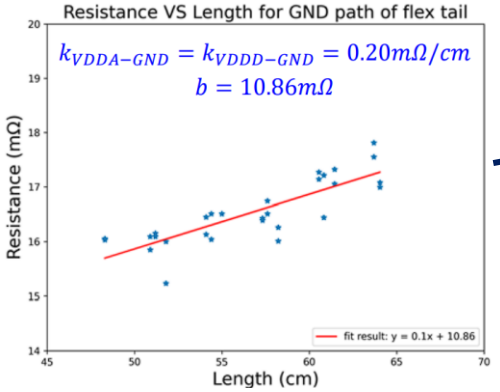
https://indico.cern.ch/event/1356490/#2-test-results-of-the-jitter-a

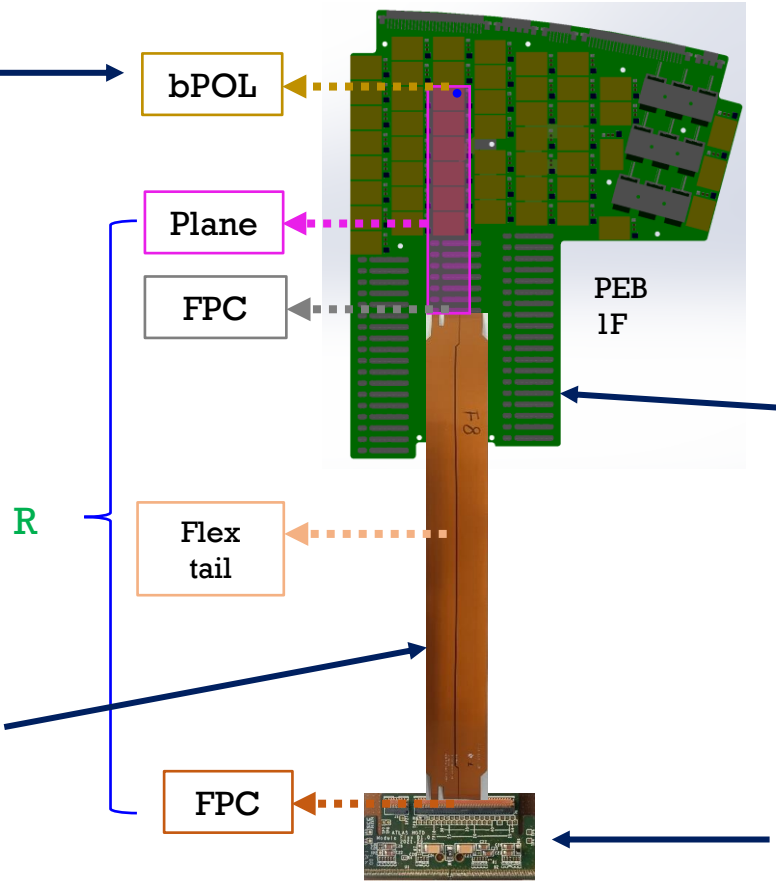
Challenges - PEB Power Settings

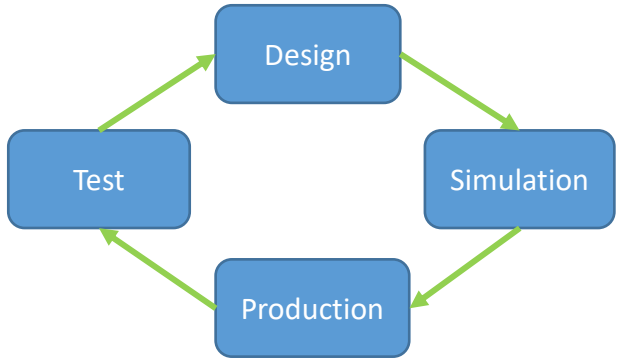


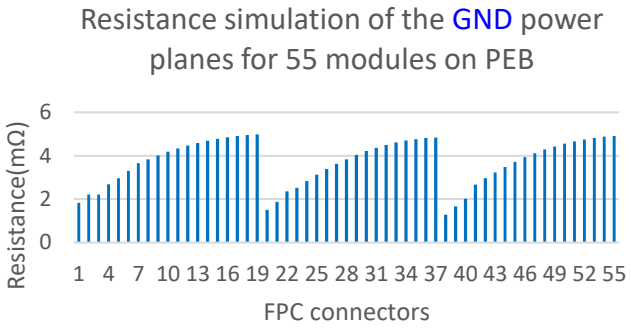
1%

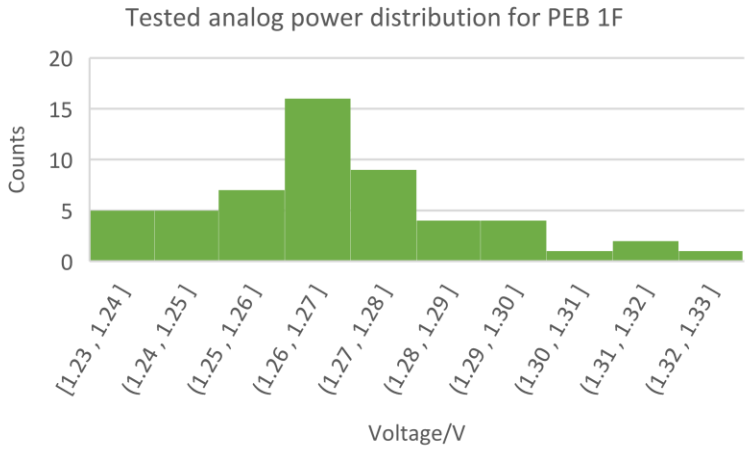
bPOL output distribution from the modular PEB











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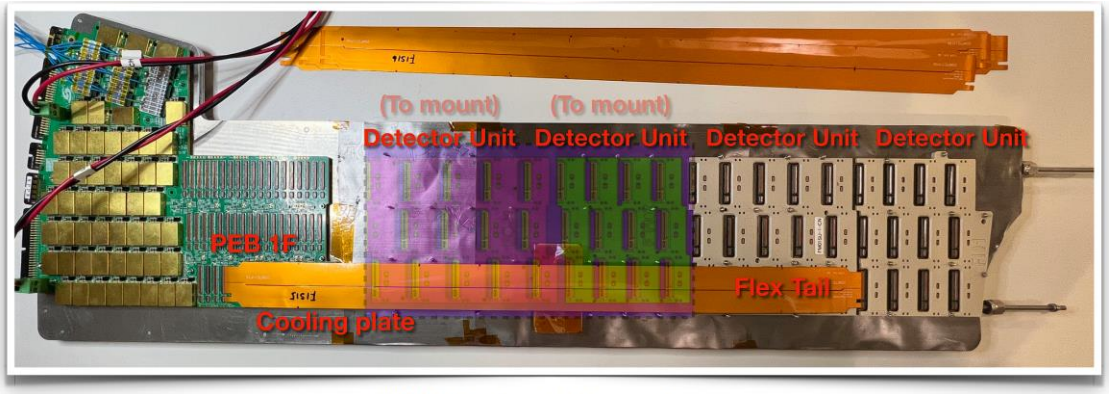
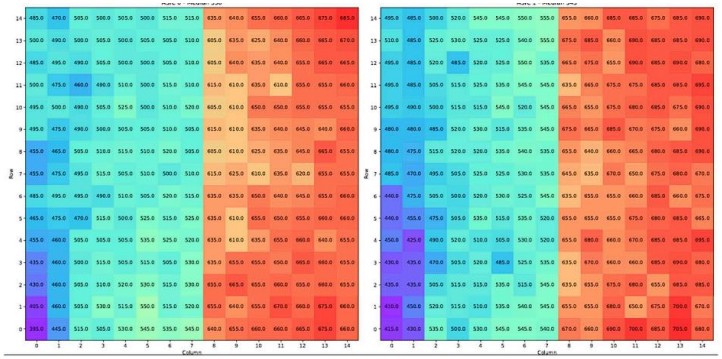
PEB 1F-joint tests



HV, LV, Cooling plate prototype
Electronics : PEB 1F + flex tails + 54 modules mounted on 4 support units (detector unit)



Module threshold scan obtained in demonstrator test

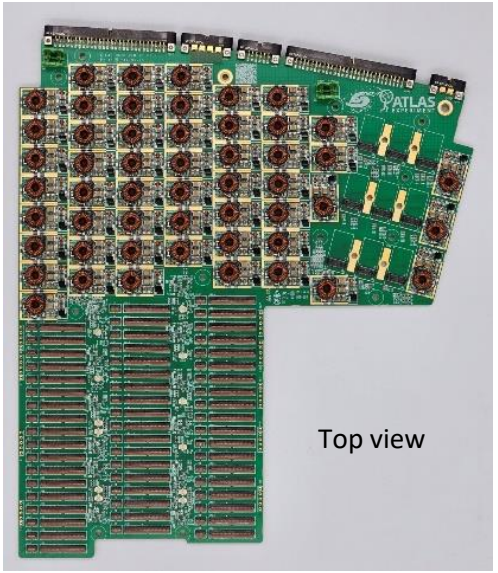
- Thermal imaging test
  - Temperature rise is about 33 ℃

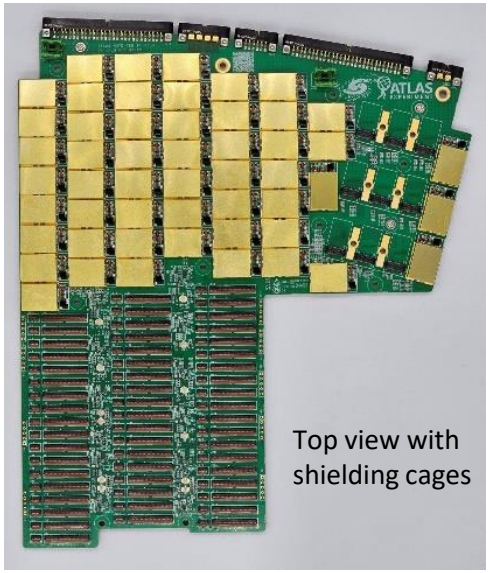
With 20 thermal emulators

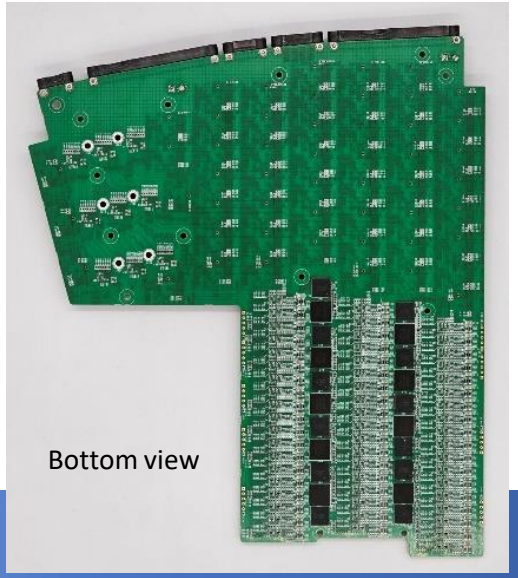
- Todo
  - Lumi readout
  - System-level noise levels
  - TDC Calibration implement at system-level
  - System-level time resolution and clock jitter
  - Grounding scheme evaluation

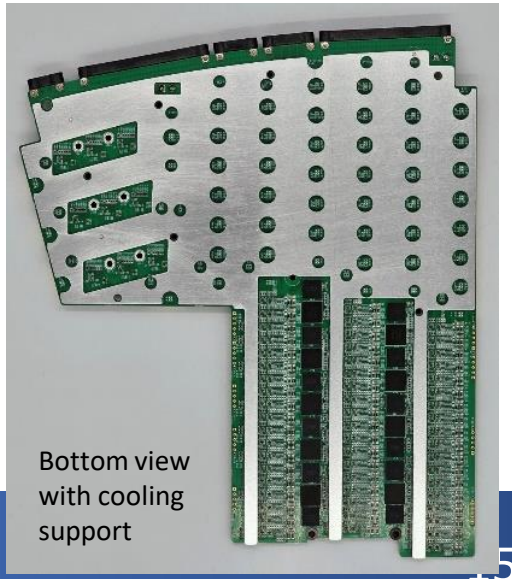
Peripheral Electronics Board – Summary

- PEB 1F prototype finished production
  - No major issues
  - Finished vendor qualification
- Focus on the module evaluation in full demonstrator
  - Electronics : 54 modules mounted on 4 support units + flex tails + PEB 1F + LV + HV
  - Cooling plate prototype
  - TDAQ + Lumi. DAQ + DCS
  - Need to be verified
    - Lumi readout
    - System-level noise evaluation
    - TDC Calibration
    - System-level time resolution and clock jitter
    - Grounding scheme evaluation
- Moving towards to the FDR phase


Top view


Top view with shielding cages

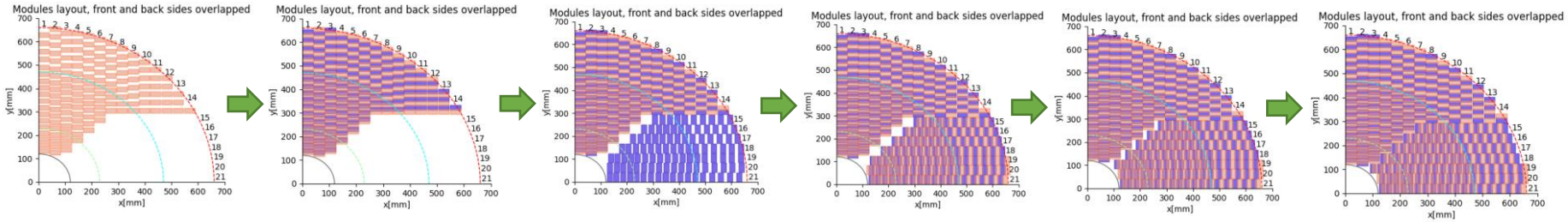

Bottom view


Bottom view with cooling support

THANKS TO YOUR ATTENTION

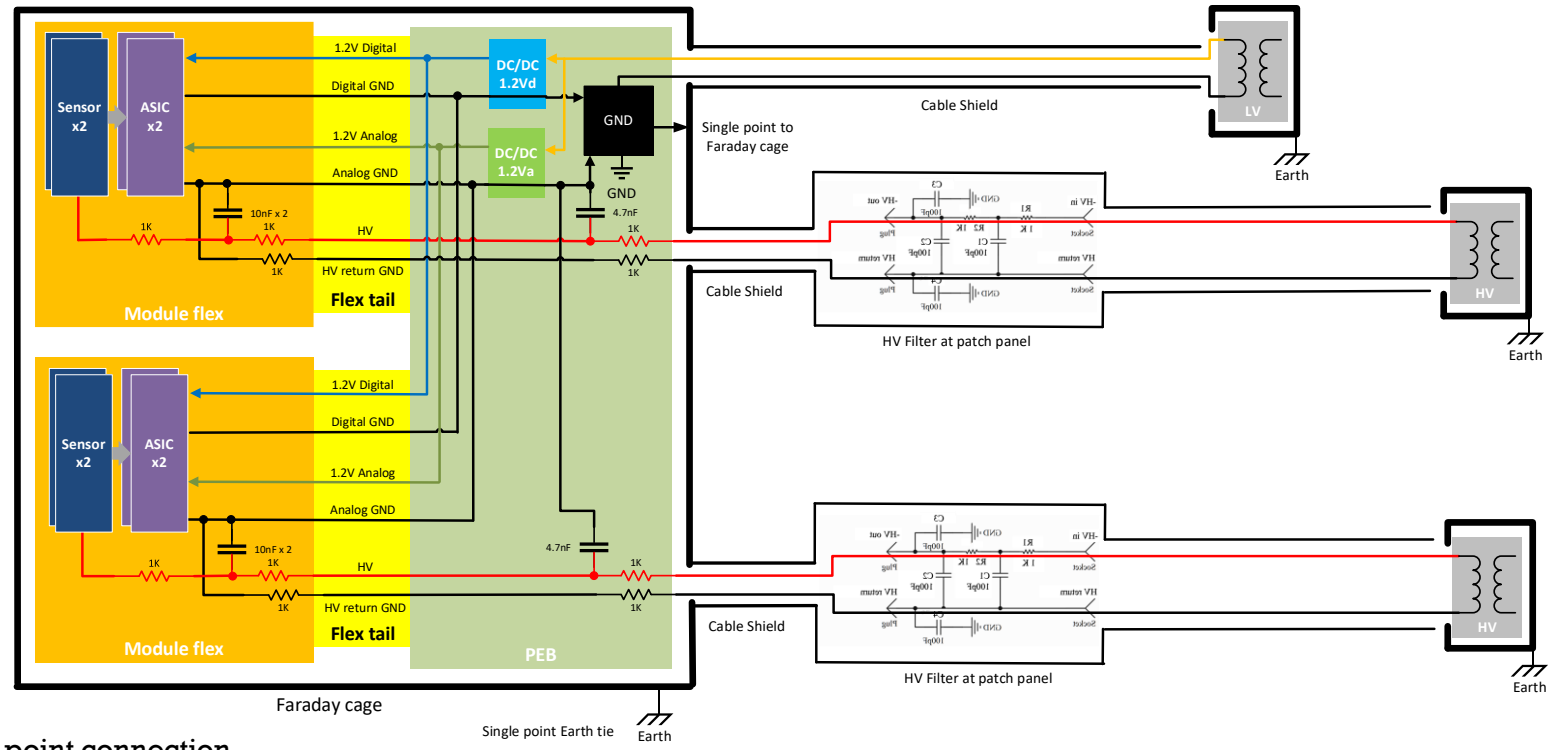
HGTD: Peripheral Electronics Board – Technical Progress and Status

- Module layout adjustment to reduce PEB types from 10 to 6
  - 1F, 2F, 2B and 1B are re-used at both side
  - Reduce the risk of the new design
    - The PCB placement and routing of 1F and 1B, 2F and 2B, have something in common, but readout speed of modules near boundaries are different. This need new channel arrangement for lpGBT
  - Save costs
    - The PCB NRE (Non Recurring Engineering) Cost for rigid-flex is 8~10 times to the price per unit
  - Reduce the risk on the project schedule
    - Design, production and testing
    - Each type of PEB will have different testing setup and software
- Mirror Structure
  - Python3 script is developed according to the constraints from TDR
  - Workflow - 6 steps to generate module layout



- The new layout is evaluated by mechanical design and physical simulation

GROUNDING & SHIELDING



- Single point connection
  - The hermetic vessel acts as the Faraday cage, which is referenced to the experiment ground by a single dedicated copper braid per end cap.
- Each PEB will have be referenced to the Faraday cage by one single low ohmic strap to the conductive layer of the outer ring.
  - The modules and the PEB shall have thermal conductive connection to the cooling plate but be electrically isolated from the cooling plate.
- The stage2 LV supplies are referenced to ground by their return lines being connected to the ground planes of the PEB which they supply.
- The HV at each module is then referenced to ground through the analog ground plane at the module end.

LPGBT ELINK ASSIGNMENT IN HGTD

Model ID	lpGBT Elinks	Mix230	Mix150	Mix310	Mix046(with lumi)	Mix00D(with 2 lumi)
M0	ECLK0, EDIN00, EDIN10, EDOUT00	1280, P0, I2C1	1280, P0, I2C1	1280, P0, I2C1	640, P0, I2C1	320, P0, I2C1
M1	ECLK1, EDIN01, EDIN11, EDOUT01	-	-	-	-	320, P0, I2C1, L640
M2	ECLK2, EDIN02, EDIN12, EDOUT02	-	-	-	640, P0, I2C1	320, P1, I2C2, L640
M3	ECLK3, EDIN03, EDIN13, EDOUT03	-	-	-	-	320, P1, I2C2, L640
M4	ECLK4, EDIN20, EDIN30, EDOUT10	1280, P0, I2C1	640, P0, I2C1	1280, P0, I2C1	640, P1, I2C2	320, P2, L_I2C0, L640
M5	ECLK5, EDIN21, EDIN31, EDOUT11	-	-	-	-	320, P2, L_I2C0, L640
M6	ECLK6, EDIN22, EDIN32, EDOUT12	-	640, P0, I2C1	-	640, P1, I2C2, L640	320, P2, L_I2C0, L640
M7	ECLK7, EDIN23, EDIN33, EDOUT13	-	-	-	-	320, P3, L_I2C1, L640
M8	ECLK8, EDIN40, EDIN50, EDOUT20	640, P1, I2C2	640, P1, I2C2	1280, P0, I2C1	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M9	ECLK9, EDIN41, EDIN51, EDOUT21	-	-	-	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M10	ECLK10, EDIN42, EDIN52, EDOUT22	640, P1, I2C2	640, P1, I2C2	-	320, P2, L_I2C1, L640	320, P4, L_I2C2, L640
M11	ECLK11, EDIN43, EDIN53, EDOUT23	-	-	-	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M12	ECLK12, EDIN60, EDIN62, EDOUT30	640, P1, I2C2	640, P1, I2C2	640, P1, I2C2	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M13	ECLK13, EDIN61, EDIN63, EDOUT31	-	-	-	320, P3 L_I2C2, L640	-

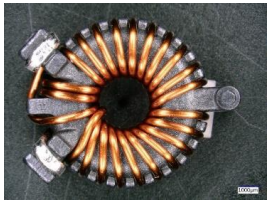
Basic patterns used in PEB, Mix XYZ

- X: number of module run 1.28 Gbps,
- Y: number of module run 640 Mbps,
- Z: number of module run 320 Mbps

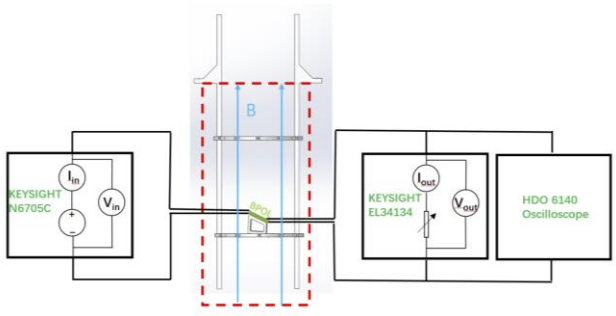
HGTD: Peripheral Electronics Board – DC/DC converter

Bpol12V generates analog and digital 1.2 V to the front-end modules

- Height limitation in HGTD
  - < 10 mm (Including PCB and shielding case)
  - Selection for air-core inductor
    - Custom solenoid coil from CMS



- Tested in low temperature (-35 ℃), OK
- Tested in magnetic field, up to 4 T, OK



BPOL12V test system in magnetic field


Aachen module

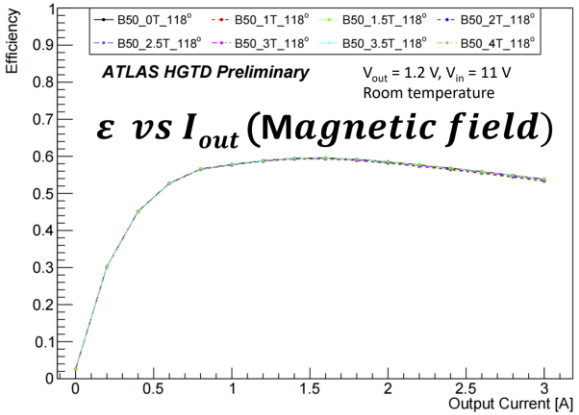
CERN module (FEASTMP)

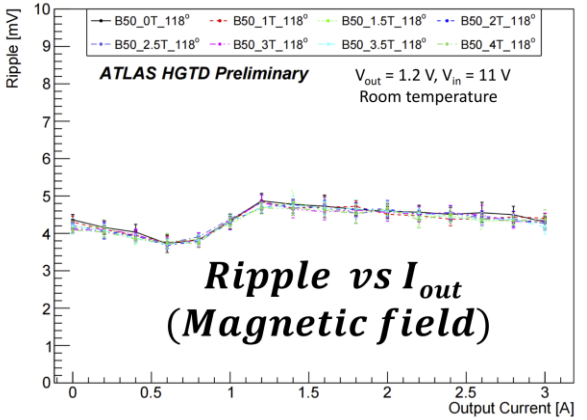
ITK EoS


Commercial inductor


HGTD

Inductor candidates





Efficiency and ripple with respect to *Iout* in magnetic field

LOOK BACK ON PEB 1F DESIGN AND PRODUCTION

Log from Gitlab

all drc clear	zhj	2023/8/23 9:58:54
release to manufacturer	zhj	2023/8/22 22:49:47
Merge branch 'master' of ssh://gitlab.cern.ch:...	zhj	2023/8/22 16:18:35
gerber generated	zhj	2023/8/22 16:18:17
PCB finished in length adjustment for ECLK a...	zhj	2023/8/22 16:11:53
update control two modular_peb at one time	jiezh	2023/8/30 17:24:06
Merge branch 'master' of ssh://gitlab.cern.ch:...	jiezh	2023/8/22 10:19:21
add logo	zhj	2023/8/21 12:43:44
Merge branch 'master' of ssh://gitlab.cern.ch:...	zhj	2023/8/21 1:21:35
update REFDES	zhj	2023/8/21 1:20:30
clear DRC	zhj	2023/8/21 0:11:42
update	zhj	2023/8/20 12:37:29
delete dangling lines and vias	zhj	2023/8/19 21:13:29
all line routed	zhj	2023/8/18 22:57:47
power plane done	zhj	2023/8/17 22:11:17
Merge branch 'master' of ssh://gitlab.cern.ch:...	zhj	2023/8/17 18:15:23
update	zhj	2023/8/17 18:15:02
update	zhj	2023/8/16 23:54:55
update	zhj	2023/8/16 21:45:34
update HV	zhj	2023/8/2 9:25:10
update 1V2 to 1F	zhj	2023/8/1 11:09:01
update via to grid	zhj	2023/8/1 8:30:51
update	zhj	2023/8/1 0:52:21
update	zhj	2023/7/28 21:22:39
update	zhj	2023/7/28 13:47:57
add 10uF x2 for each module	zhj	2023/7/24 17:45:24
change the location of one screw	zhj	2023/7/24 10:34:19
update	zhj	2023/7/21 17:51:09
T3 done	zhj	2023/7/21 0:49:26
update runVthc	jiezh	2023/8/22 10:17:07
T0, T1, T2 almost done	zhj	2023/7/18 23:02:44
update	zhj	2023/7/17 1:07:40
T2 done	zhj	2023/7/16 1:25:30
finish module interface modification	zhj	2023/7/13 17:51:34
before add pull-up/down R for I2C address, a...	zhj	2023/7/13 8:53:20
update	zhj	2023/7/10 23:53:17
T0 done	zhj	2023/7/10 0:18:34
VTRx+ done	zhj	2023/7/5 22:18:12
update monitor	zhj	2023/7/4 0:06:20
T0 routing	zhj	2023/7/3 0:47:19
update via4 and via8	zhj	2023/7/2 9:24:38
update	zhj	2023/7/2 0:20:16
update LV connector part number	zhj	2023/6/28 22:56:33
update power plane	zhj	2023/6/25 22:51:47
update outring connector with low-profile	zhj	2023/6/21 0:16:24
placement done	zhj	2023/6/15 17:21:25
FPC connector update	zhj	2023/6/14 23:03:57
add distribution statistics	zhj	2023/6/13 21:34:28
Merge branch 'master' of ssh://gitlab.cern.ch:...	zhj	2023/6/13 21:23:30
QA/QC for coils batch1	zhj	2023/6/13 21:22:48
update	zhj	2023/6/12 13:44:03
update design according to 1F placement an...	zhj	2023/6/12 8:30:29
update power	zhj	2023/6/10 7:11:52
update	zhj	2023/6/9 20:38:33
update blind via	zhj	2023/6/9 8:33:21
re placement	zhj	2023/6/9 8:21:15
change via to 8mil	zhj	2023/6/8 23:09:45
update via	zhj	2023/6/8 15:04:55
before change elink assignment	zhj	2023/6/6 15:57:14
before change cross section	zhj	2023/6/5 8:28:45
add M2 spacer	zhj	2023/6/3 0:59:44
update differential pairs	zhj	2023/6/2 23:08:11
add coordinates of holes for M2 screws	zhj	2023/6/2 9:13:27
update	zhj	2023/5/31 16:53:26
update HV filter	zhj	2023/5/29 23:13:34
change to holes as 3.0 mm	zhj	2023/5/29 11:49:55
update board	zhj	2023/5/22 23:22:02
add grounding connector	zhj	2023/5/19 9:40:50
use_lumi to enable/disable lumi. channel	zhj	2023/5/13 20:56:06
Merge branch 'master' of ssh://gitlab.cern.ch:...	zhj	2023/5/13 20:44:01

Design tracked and backup by gitlab

Main timeline:

- May 2: Update heat sink for VTRx+, use M2 screws to lock
- May 5: Add pull-down resisters for MUX64 according to the feedback from radiation tests
- May 19: Add grounding connector
- May 29: Change the holes to 3.0 mm, add HV filter according to ASIC group recommendation
- June 3: Add M2 spacers
- June 9: Update blind via
- June 12: Update design according to 1F placement and routing
- June 21: Change the outring connectors with low-profile
- July 13: Finish module interface modification
- July 14~Aug 1: Routing
- Aug 1: Update HV
- Aug 2~Aug 17: Power/GND plane partition
- Aug 22: PCB finished in length adjustment for ECLK and EDIN.
- Aug 23: All DRC cleared
- Aug 23: Submit to 8.2-D -> Sep. 4: NJU seals the contract -> Sep. 15: finish EQ, and start production
- Sep. 15: Submit to 8.2-C -> Sep. 27: NJU seals the contract -> Sep. 27: start production
- Oct. 21: Submit to 8.2-B -> Nov. 8: NJU seals the contract
- Sep. to now: Determine the bPOL output voltage
  - Module operating current at a specific hit rate(output data speed, lumi. enable)
  - Flex voltage drop (measured)
  - PEB voltage drop (simulated)

Pre-sequencing tasks
1. PCB outline and PEB envelope height confirmation by mechanical group
2. Fixation style confirmation by mechanical group
3. Outer ring connectors confirmation by cable group

Summer holiday from July. 31 to Aug. 13

41 workdays for PEB 1F design

More than 13 days for business process in NJU

PCB MATERIALS

		8.2-D	-	8.2-B/C	8.2-E
		IT-170	IT-988	EM-890K	TU-883A
Dk, dielectric constant	1GHz	4	3.21	2.93	3.91
	2GHz	3.9	3.21	2.89	
	5GHz	3.9	3.21	2.88	3.9
	10GHz	3.8	3.21	2.84	3.89
	20GHz		3.21	2.81	3.86
Df, loss factor	1GHz	0.006	0.0014	0.0018	0.0024
	2GHz	0.0063	0.0014	0.0021	
	5GHz	0.0075	0.0014	0.0022	0.0031
	10GHz	0.008	0.0014	0.0024	0.004
	20GHz		0.0015	0.0025	0.0044