

# The Prototype of the Peripheral Electronics Board

## A Component of the HGTD In-detector Electronics for the ATLAS Phase-II Upgrade



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### Introduction to HGTD (High Granularity Timing Detector)

Silicon detector with coarse spatial resolution but precise timing for the ATLAS experiment

- ~3.6 million  $1.3 \times 1.3$  mm<sup>2</sup> pixels with LGAD (Low-Gain Avalanche Detector) technology
    - 6.1 m<sup>2</sup> active area
  - Pileup rejection
    - Time resolution at the start (end): 30 (50) ps per track / 35 (70) ps per hit
  - Luminosity measurement
    - Count number of hits at 40 MHz (bunch-by-bunch)
    - Goal for HL-LHC: 1% luminosity uncertainty
  - Two end-caps
    - $z \approx \pm 3.5$  m from the nominal interaction point
    - $110 < r < 1000$  mm
    - Active detector region:  $2.4 < |\eta| < 4.0$
  - Each end-cap
    - Two instrumented disks, rotated by 15°
- On each disk:
- Double-sided layers mounted on a cooling plate
  - 3 ring layout for front-end modules

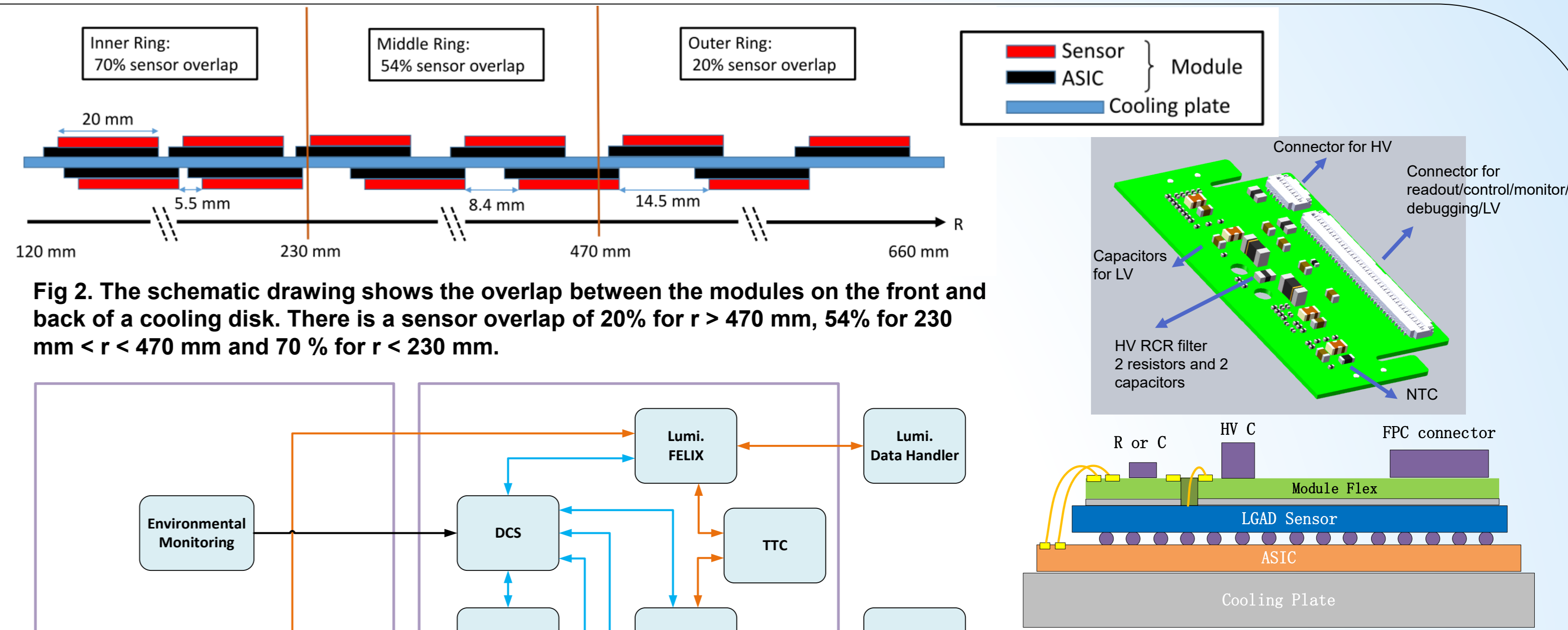
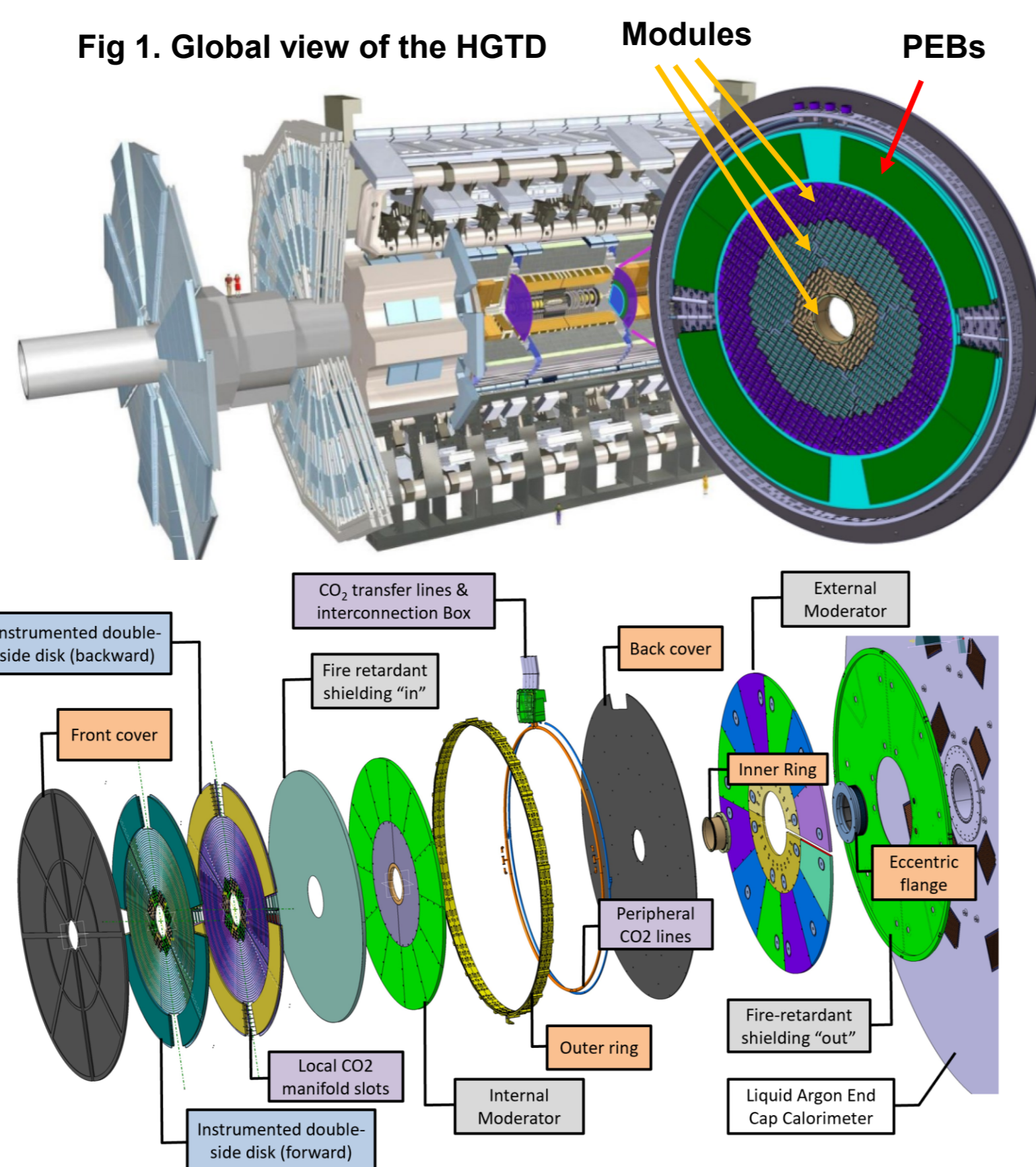


Fig 2. The schematic drawing shows the overlap between the modules on the front and back of a cooling disk. There is a sensor overlap of 20% for  $r > 470$  mm, 54% for  $230$  mm  $< r < 470$  mm and 70 % for  $r < 230$  mm.

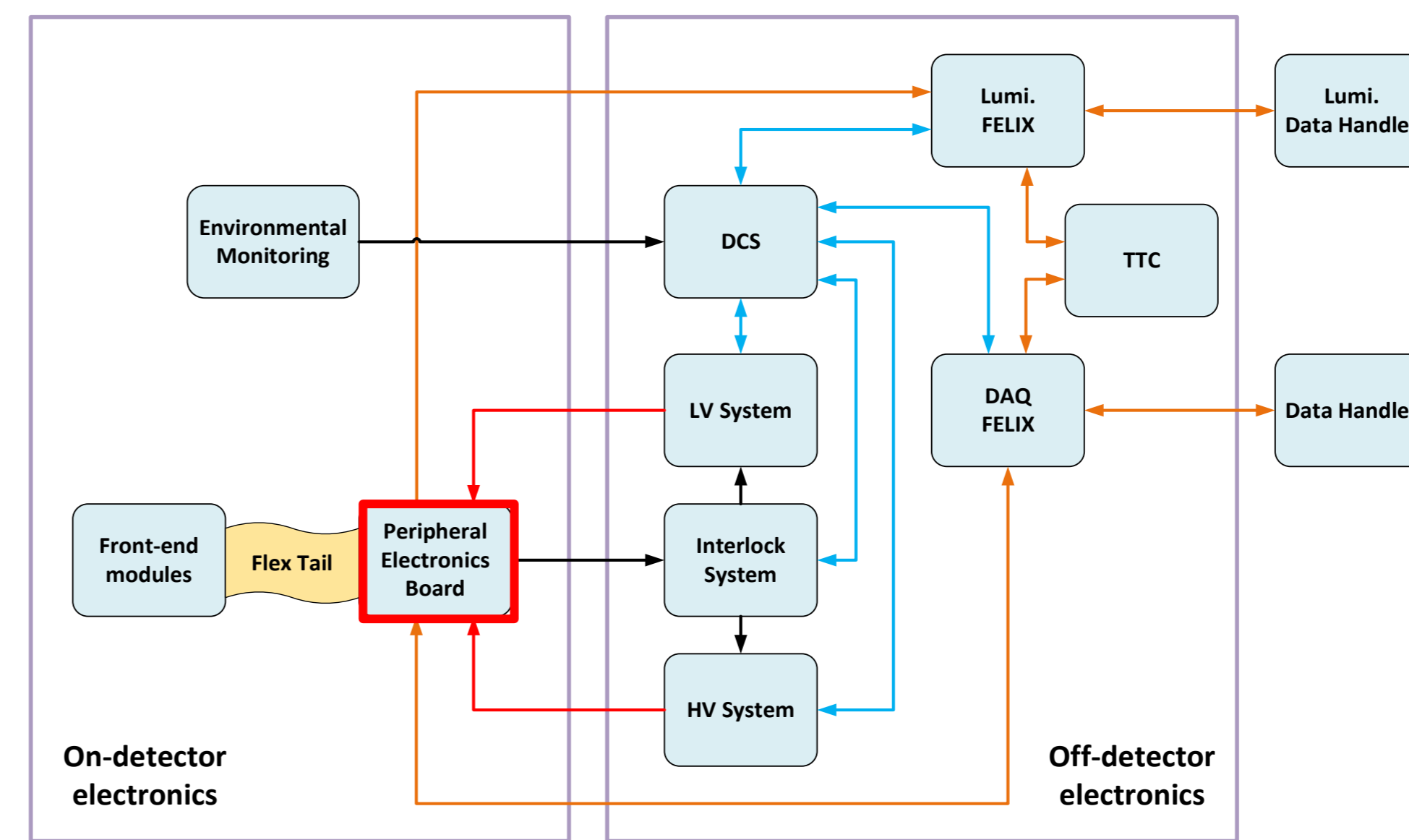


Fig 4. HGTD electronics architecture.

#### Basic functions of PEB

- Control, monitoring & data aggregation and transmission
- Power-supply distribution
  - Low voltage (LV) & High voltage (HV)
- Thermistor connection between the front-end modules and the interlock system

### Peripheral Electronics Board (PEB)

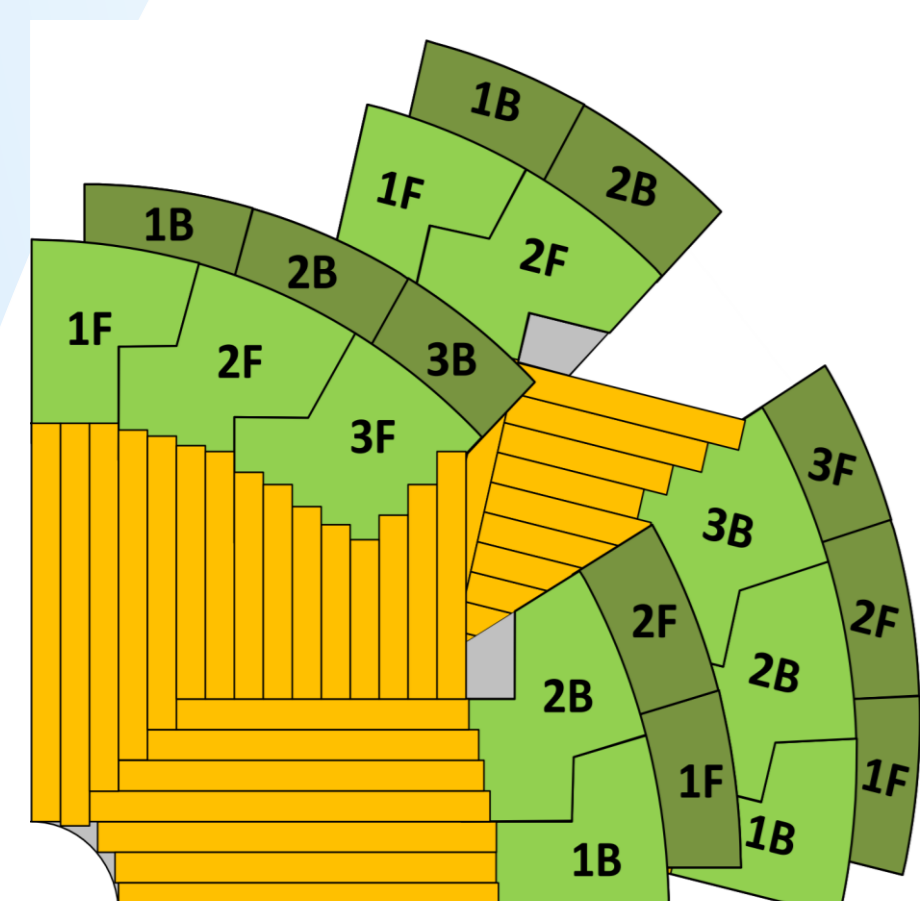


Fig 5. One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- Six types of PEB to be designed (front and back side) according to the installation location.
  - Board 1F, 2F, 1B and 2B can be used both on front and back
- The front-end modules are connected via flex tails, arranged in rows, to the PEB @  $660 < r < 920$  mm

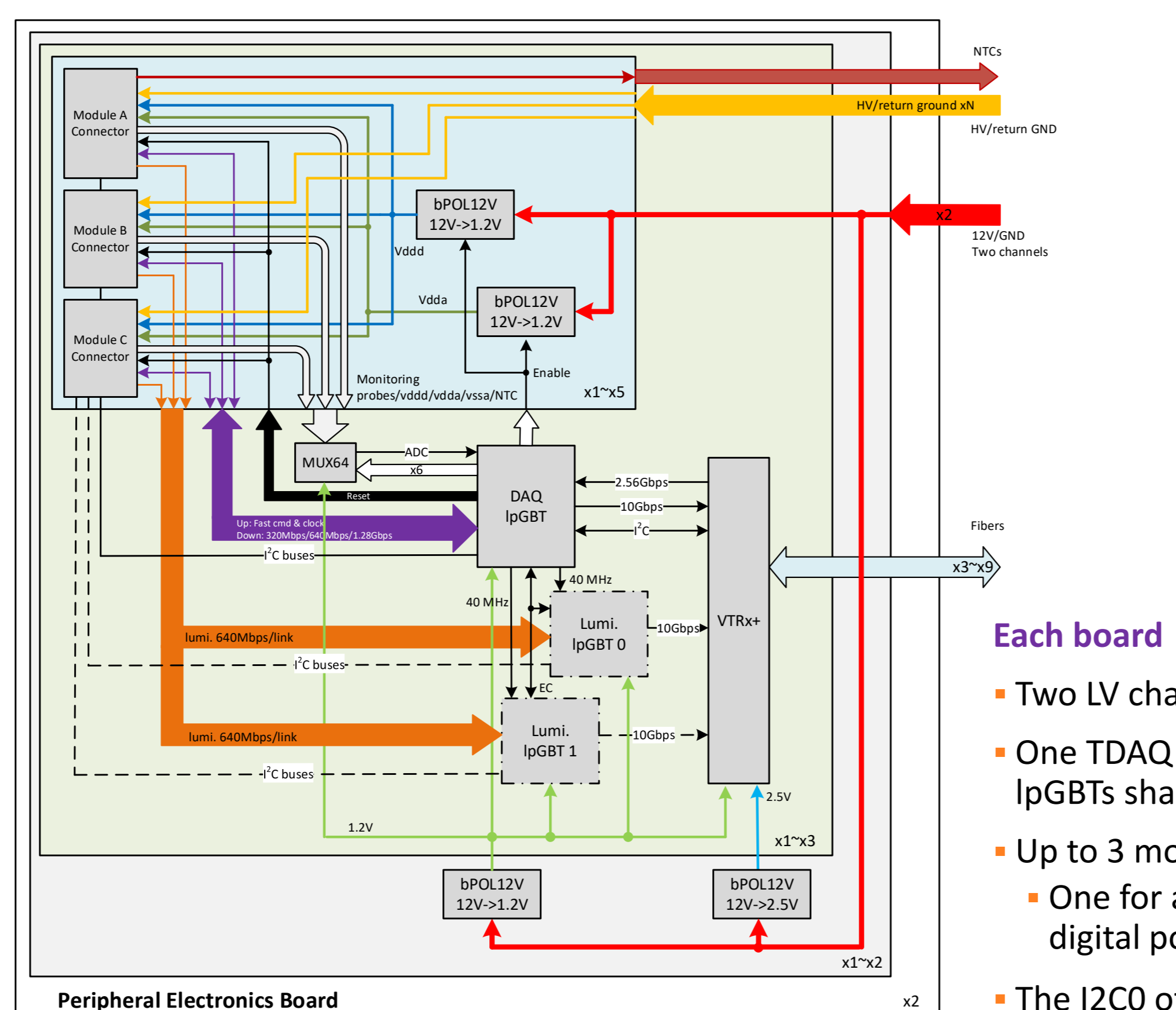


Fig 6. Conceptual design of the PEB

#### Each board

- Two LV channels
- One TDAQ IpGBT and 1~2 luminosity IpGBTs share one VTRx+
- Up to 3 modules share 2 bPOL12V
  - One for analog power, the other for digital power
- The I2C0 of TDAQ IpGBT is connected to the VTRx+ only

Tab 1. IpGBT elink assignments

Model ID	IpGBT Elinks	Mix230	Mix150	Mix310	Mix046(with lumi)	Mix00D(with 2 lumi)
M0	ECLK0, EDIN00, EDIN10, EDOUT00	1280, P0, I2C1	1280, P0, I2C1	1280, P0, I2C1	640, P0, I2C1	320, P0, I2C1
M1	ECLK1, EDIN01, EDIN11, EDOUT01	-	-	-	-	320, P0, I2C1, L640
M2	ECLK2, EDIN02, EDIN12, EDOUT02	-	-	-	640, P0, I2C1	320, P1, I2C2, L640
M3	ECLK3, EDIN03, EDIN13, EDOUT03	-	-	-	-	320, P1, I2C2, L640
M4	ECLK4, EDIN20, EDIN30, EDOUT10	1280, P0, I2C1	640, P0, I2C1	1280, P0, I2C1	640, P1, I2C2	320, P1, I2C2, L640
M5	ECLK5, EDIN21, EDIN31, EDOUT11	-	-	-	-	320, P2, L_I2C0, L640
M6	ECLK6, EDIN22, EDIN32, EDOUT12	-	640, P0, I2C1	-	640, P1, I2C2, L640	320, P2, L_I2C0, L640
M7	ECLK7, EDIN23, EDIN33, EDOUT13	-	-	-	-	320, P3, L_I2C1, L640
M8	ECLK8, EDIN40, EDIN50, EDOUT20	640, P1, I2C2	640, P1, I2C2	1280, P0, I2C1	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M9	ECLK9, EDIN41, EDIN51, EDOUT21	-	-	-	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M10	ECLK10, EDIN42, EDIN52, EDOUT22	640, P1, I2C2	640, P1, I2C2	-	320, P2, L_I2C1, L640	320, P4, L_I2C2, L640
M11	ECLK11, EDIN43, EDIN53, EDOUT23	-	-	-	320, P4, L_I2C2, L640	320, P4, L_I2C2, L640
M12	ECLK12, EDIN60, EDIN62, EDOUT30	640, P1, I2C2	640, P1, I2C2	640, P1, I2C2	320, P3, L_I2C2, L640	320, P4, L_I2C2, L640
M13	ECLK13, EDIN61, EDIN63, EDOUT31	-	-	-	-	320, P3, L_I2C2, L640

#### Basic patterns used in PEB, Mix XYZ

- X: number of module run 1.28 Gbps,
- Y: number of module run 640 Mbps,
- Z: number of module run 320 Mbps

#### Physical Constraints

- Height < 10 mm
- The space available for the electronics in the z-dimension is also very small: 9 mm with a 1 mm margin.

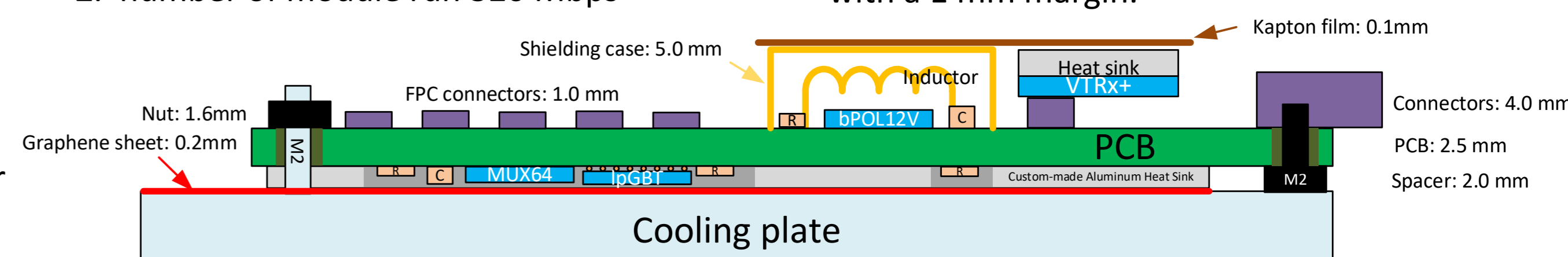


Fig 7. Side view of PEB 1F

### PEB 1F prototype

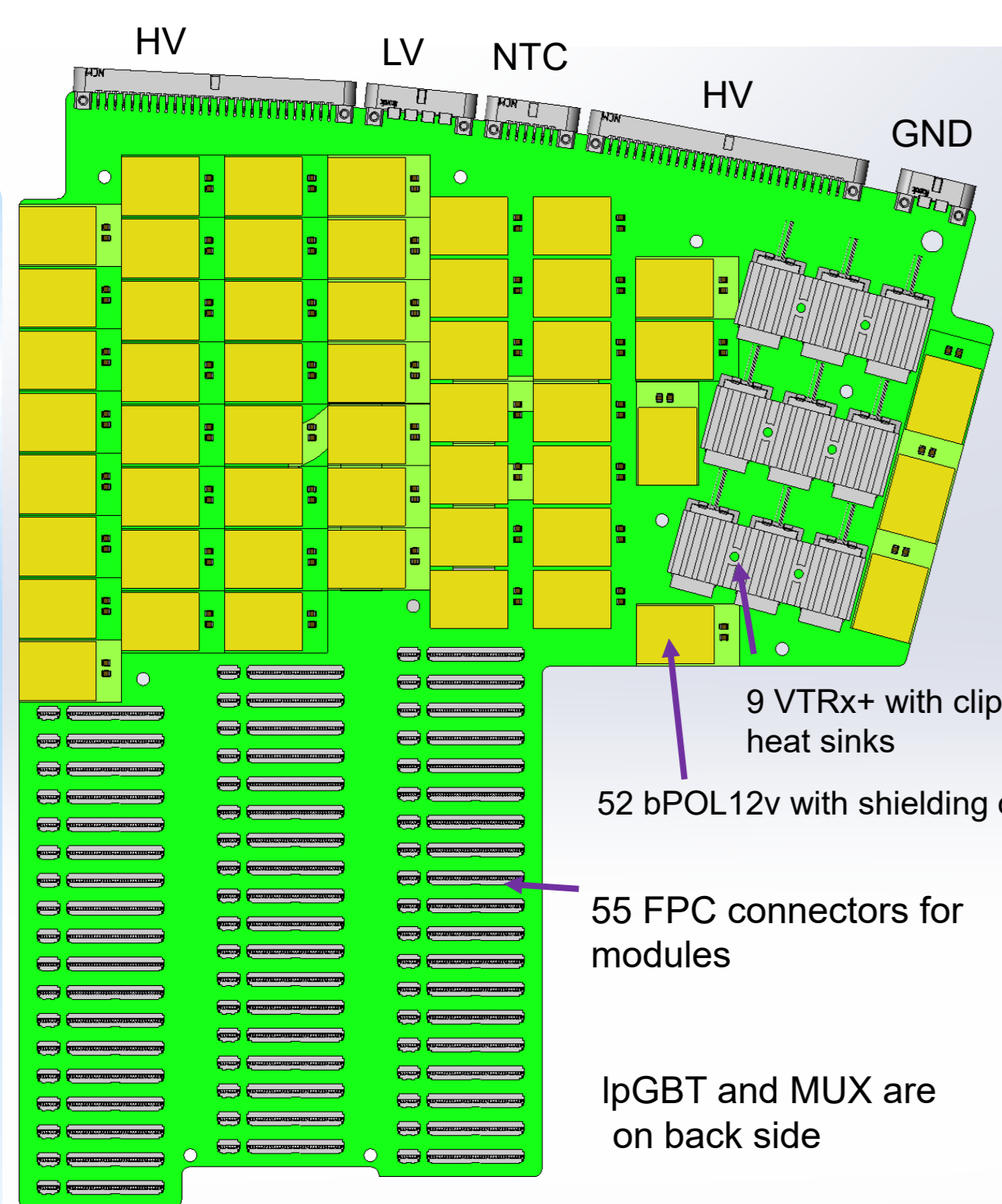
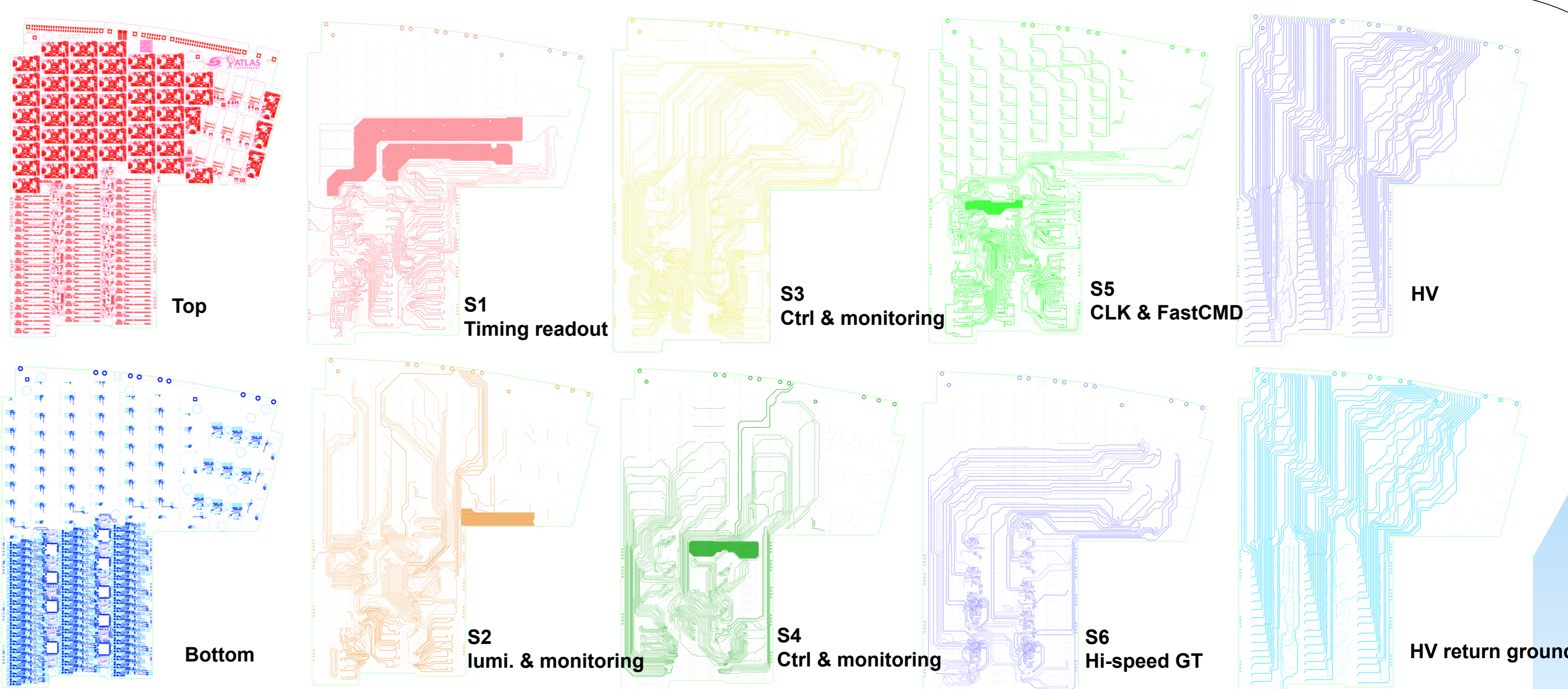
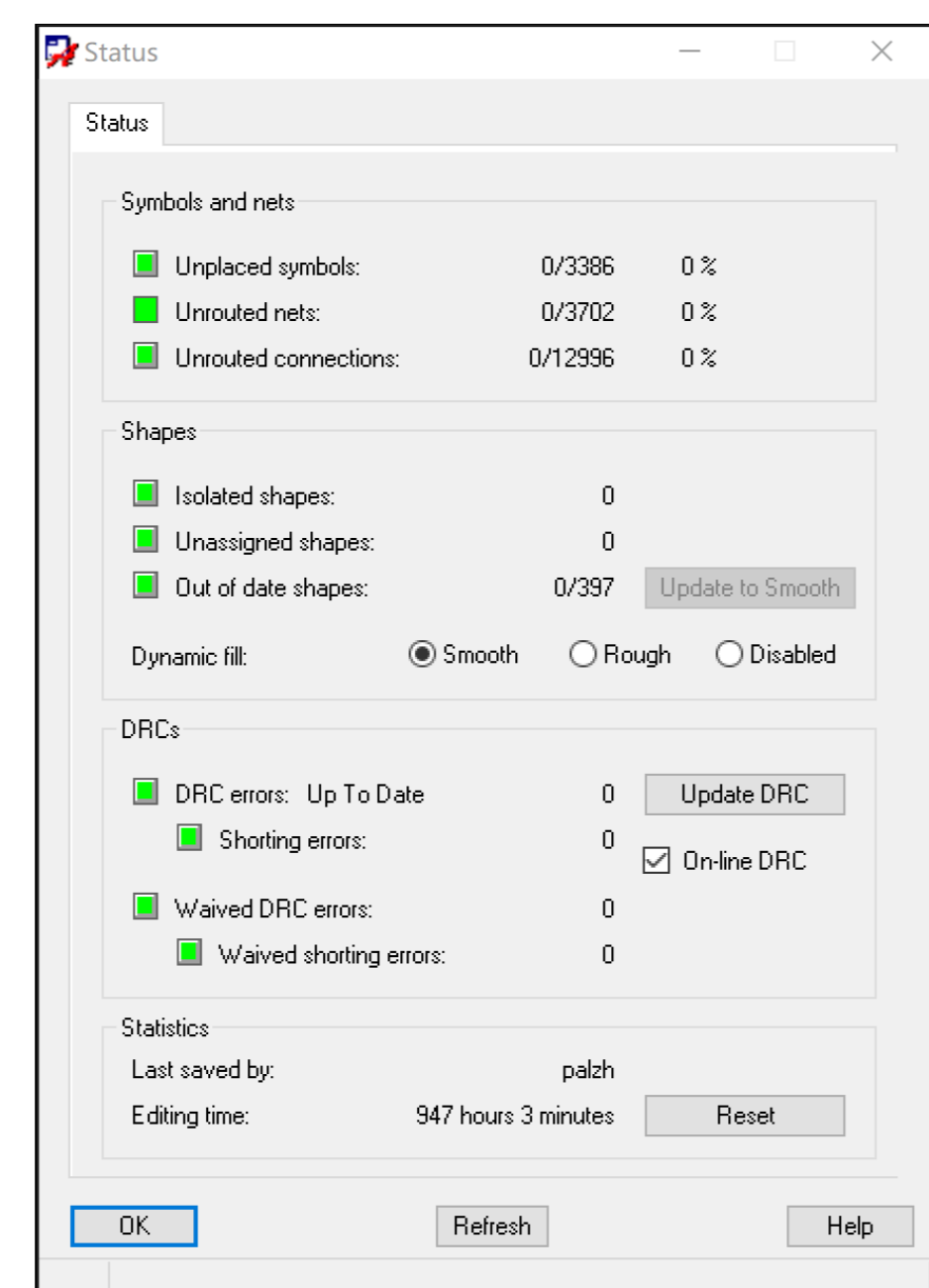


Fig 8. Top view of PEB 1F

#### Complex PCB

- High speed, low loss multi-layer material
- Halogen free
  - EM-890 or IT-170/988 or R-5375(E)
- Impedance control
- 22 layers PCB for PEB 1F, includes:
  - 8 layers for signals
  - 2 layer for HV and HV return ground
  - 4 layers for ground
  - 8 layers for power



#### PEB 1F-Prototype fabrication and pre-qualification

- Highly qualified vendor to be chosen for the PCB fabrication and assembly.
- The qualification process includes participation of the candidate vendors in the PEB prototype, and evaluation of the quality of the delivered product
- 4 companies joined and passed PEB 1F prototype fabrication

Tab 3. Number of components in PEB 1F

Peripheral board	Modules	IpGBT	bPOL12V	MUX	VTRx+
1F	55	9+3	52	9	9

- PEB 1F, re-used on back side
  - 9 IpGBTs for timing
    - Front-end modules in 3 speeds according to occupancy
  - 3 IpGBTs for luminosity
    - 7 outermost modules in each row

#### HDI (High Density Interconnector)

- Micro via
  - Through hole
  - Buried via
  - Blind via
- VIPPO / POVF: Via-in-Pad Plated Over PCB
  - Solder resist
  - Surface plating
  - Epoxy filling
  - Via plating

