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The Prototype of the Peripheral Electronics Board - a Component of the HGTD In-detector Electronics for the ATLAS Phase-II Upgrade

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The HGTD is a novel detector introduced to augment the new all-silicon Inner Tracker in the pseudo-rapidity range from 2.4 to 4.0, adding the capability to measure charged-particle trajectories in time as well as space. A prototype of Peripheral Electronics Board (PEB), which supports up to 55 front-end modules with 12 lpGBT, 9 VTRx+ and 52 bPOL12v, is developed to work as a bridge between the front-end modules and the off-detector TDAQ. The on-going R&D effort carried out to study the readout and transmission chips, and the other components, supported by laboratory test results, will also be presented.

Summary (500 words)

The increase of the particle flux at the HL-LHC with instantaneous luminosities up to ˜7.5 × 10ˆ34 cmˆ-2sˆ-1 will have a severe impact on the ATLAS detector reconstruction and trigger performance. The High Granularity Timing Detector (HGTD), an ATLAS Phase II upgrade project, will provide an accurate measurement of the time of the tracks (< 50 ps) in order to mitigate the effect of the pile-up in the object reconstruction as the jets, the electrons or the b-jets. In addition, the number of collected hits being proportional to the luminosity, it will provide an instantaneous measurement of the luminosity, which will be read out at 40 MHz. HGTD is composed of 8032 front-end modules. Each module consists of two Low Gain Avalanche Detectors (LGADs) of approximately 2 × 2cmˆ2 bump-bonded to two ATLAS LGAD Timing Integrated Read-Out Chips and held together by a module flex. These modules are arranged with overlap on the two sides on each disk. Each module will be connected to the PEB through a flex tail. The connections between on-detector and off-detector electronics are performed via optical fibers, high/low voltage cables, interlock cables and monitoring signal cables. The PEB acts as a bridge between the front-end modules and the off-detector systems. The optical fibers provide shared data streams for Timing, Trigger and Control (TTC), Detector Control System (DCS) and Data Acquisition System (DAQ), and dedicated data streams for the luminosity system through the low-power GigaBit Transmission chip (lpGBT) and the Versatile Link + Transceiver (VTRx+). The PEB also includes the 12 V to 1.2 V DC-DC converters (bPOL12v) for the digital and analog voltages supplied to the front-end modules. The supply voltages are monitored using the internal multiplexed ADC on the lpGBTs. According to the optimization of mirror structure for the layout of the modules, 6 types of PEBs need to be designed for HGTD.

Based on previous development experience, the PEB 1F was chosen to be designed first as a prototype since it is the most complicated PEB type, supporting up to 55 front-end modules with 12 lpGBT, 9 VTRx+, and 52 bPOL12v in a very limited space. The PCB is completed using a 22-layer buried via process to address its complexity. The PEB 1F prototype is a full-size board, designed as closely as possible to the final PEB. It is crucial to select highly qualified PCB vendors for the PCB fabrication. The qualification process included the participation of the four candidate vendors in the PEB prototype and an evaluation of the quality of the delivered products. In addition to testing and evaluation at the single-board level, the FEB 1F prototype undergoes an integration test. In this test, a full-size PEB 1F, including 54 real modules (about 0.7% of the full system), as well as the associated components (interlock, DCS, TDAQ, cooling system, support unit, cabling, etc.) are assembled and tested.

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