



# EMCI-EMP: Developments and Experience with the Novel Detector Control Solution



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## Motivation & Requirements

- The Detector Control System (DCS) [1] of the ATLAS detector ensures safe and coherent operation by controlling and monitoring the operational parameters of detector sub-systems and infrastructure independent from other systems such as readout.
- The reliability of the DCS must be ensured also during the High-Luminosity LHC (HL-LHC) era.
- Common slow-control solutions must meet HL-LHC requirements such as increased radiation levels, and increased I/O performance and density.

The challenges were addressed by developing the **Embedded Monitoring Processor (EMP)** and the **Embedded Monitoring and Control Interface (EMCI)**.

[1] <https://iopscience.iop.org/article/10.1088/1748-0221/3/05/P05006/pdf>

## Hardware

### EMCI

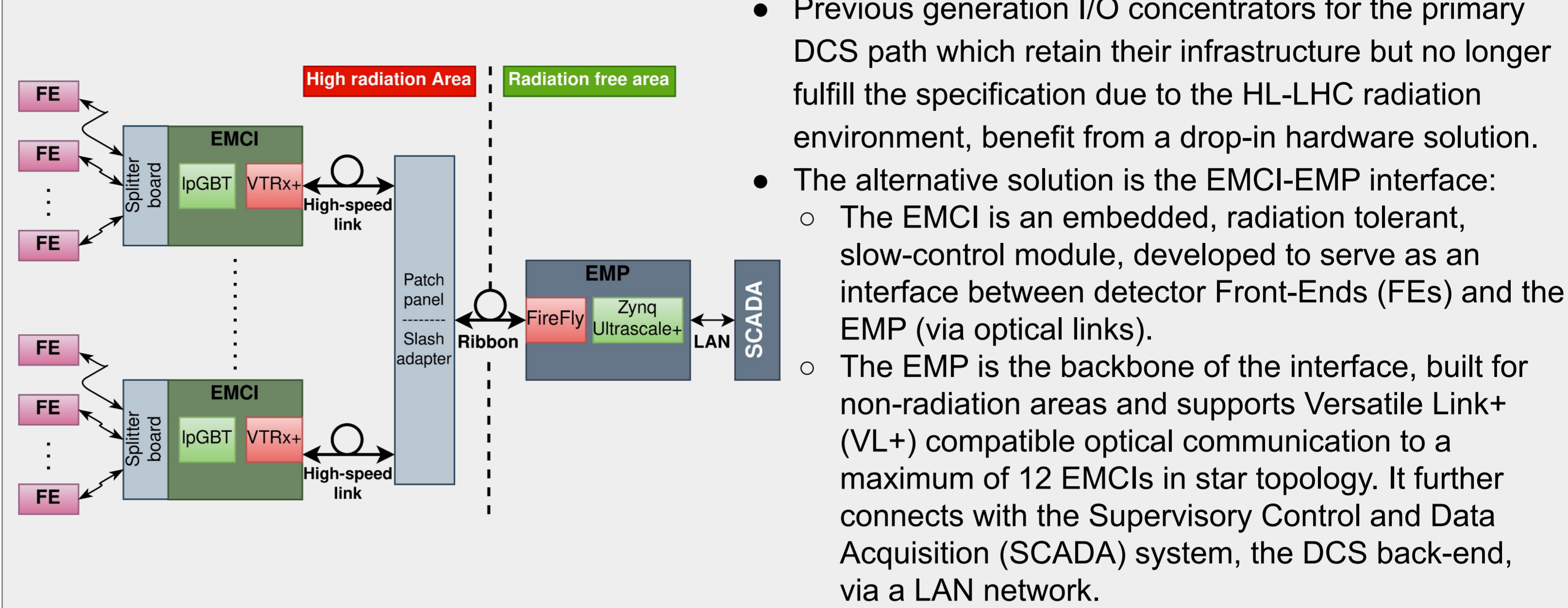
- Bidirectional interface between EMP and detector FEs, based on CERN developed, radiation tolerant components (>100Mrad TID tolerance):
  - low power GigaBit Transceiver (IpGBT)
  - Versatile Transceiver (VTRx+)
  - FEASTMP DC-DC converter
- FE devices can be connected via electrical Links (eLinks), 16 up/down links (80 Mb/s)
- Additional interfaces: I2C, ADC, DAC, eLink clocks, GPIOs

### EMP

- Optical transceiver backbone for non-radiation areas
- Based on a highly flexible AMD Zynq Ultrascale+ MPSoC module
  - 64-bit quad-core ARM Cortex-A53 (APU)
  - Programmable Logic
- Interfaces with up to 12 EMCI towards FEs via Samtec FireFly™ Transceivers (MGTs) in accordance with VL+ standards
- Connects via dual ethernet with the distributed LCS
- Provides additional 144 single-ended/72 differential IO lines via VITA 57-compliant FMC connector
- Comprehensive memory infrastructure featuring 256 kB EEPROM, 512 MB SPI memory, 4 GB RAM and 16 GB eMMC storage
- Equipped with on-board I2C temperature sensors
- Additional Interfaces: UART, JTAG, XADC, I2C, MIO

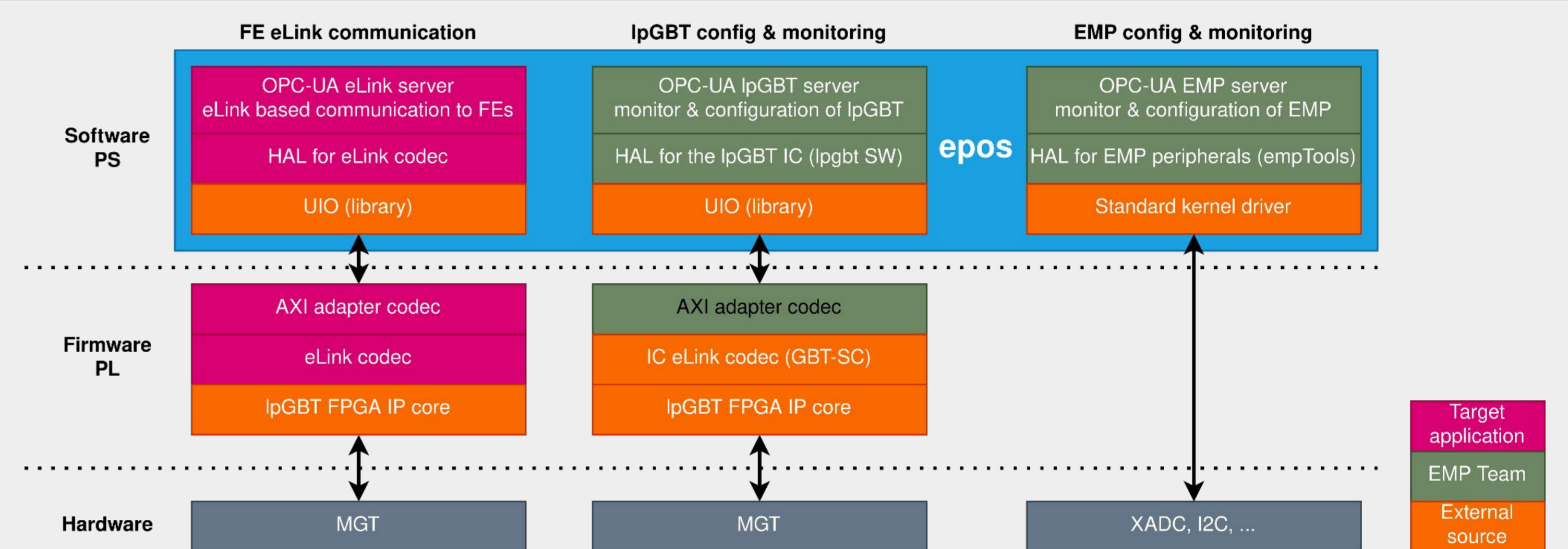


## EMCI-EMP Overview



- Previous generation I/O concentrators for the primary DCS path which retain their infrastructure but no longer fulfill the specification due to the HL-LHC radiation environment, benefit from a drop-in hardware solution.
- The alternative solution is the EMCI-EMP interface:
  - The EMCI is an embedded, radiation tolerant, slow-control module, developed to serve as an interface between detector Front-Ends (FEs) and the EMP (via optical links).
  - The EMP is the backbone of the interface, built for non-radiation areas and supports Versatile Link+ (VL+) compatible optical communication to a maximum of 12 EMCI in star topology. It further connects with the Supervisory Control and Data Acquisition (SCADA) system, the DCS back-end, via a LAN network.

## EMP Software & Firmware Architecture



SW & FW architecture must cover three different functionality modes:

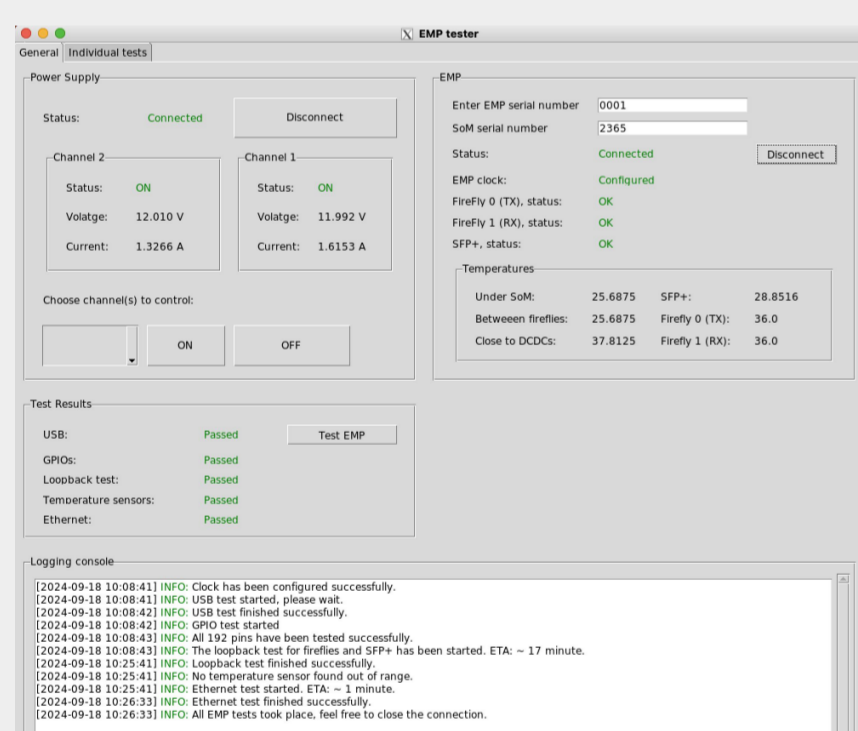
- eLink communication (specific to targeted FE device)
- EMCI configuration & monitoring
- EMP configuration & monitoring

The architecture generates a common need for generic EMP SW & FW components like an Operating System, basic software support for EMP peripherals & common FW building blocks

## Testing

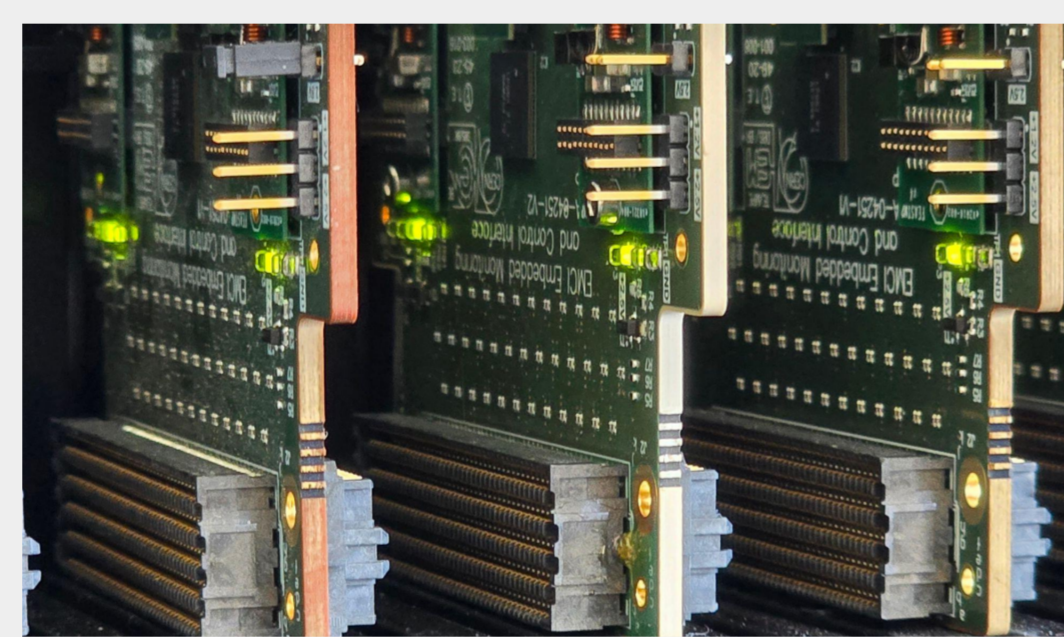
### EMCI & EMP Testbenches

- The EMCI and EMP testbenches were developed with the objective to ensure the functional integrity of new hardware
- Each setup must demonstrate the functionality of every interface available on the EMP and EMCI
- Both testbenches are standalone setups, based on dedicated SW and FW applications, integrated into user-friendly GUIs
- High-quality optical communication on every EMP with a BER of 10<sup>-13</sup> is verified via the IBERT-core



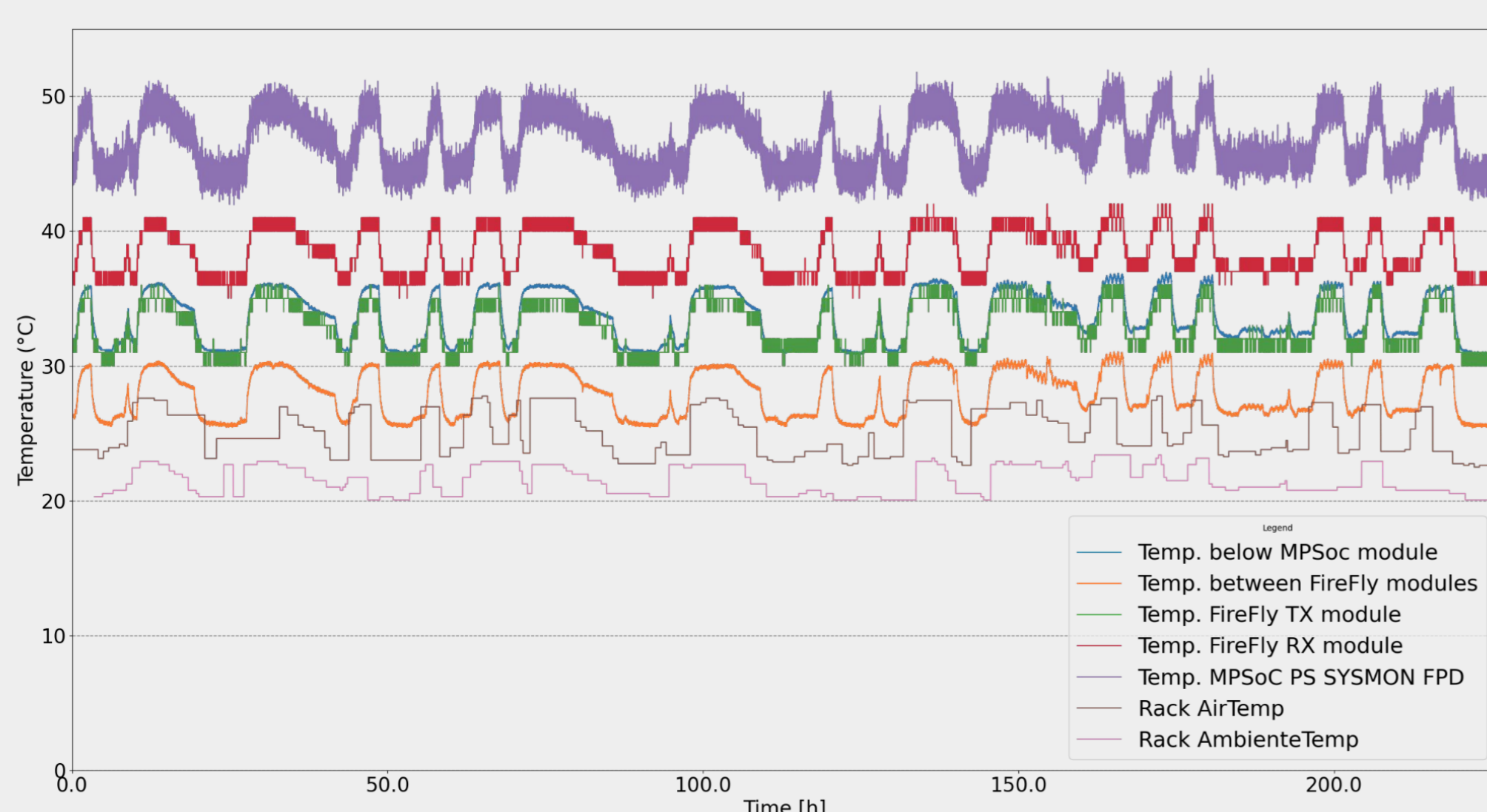
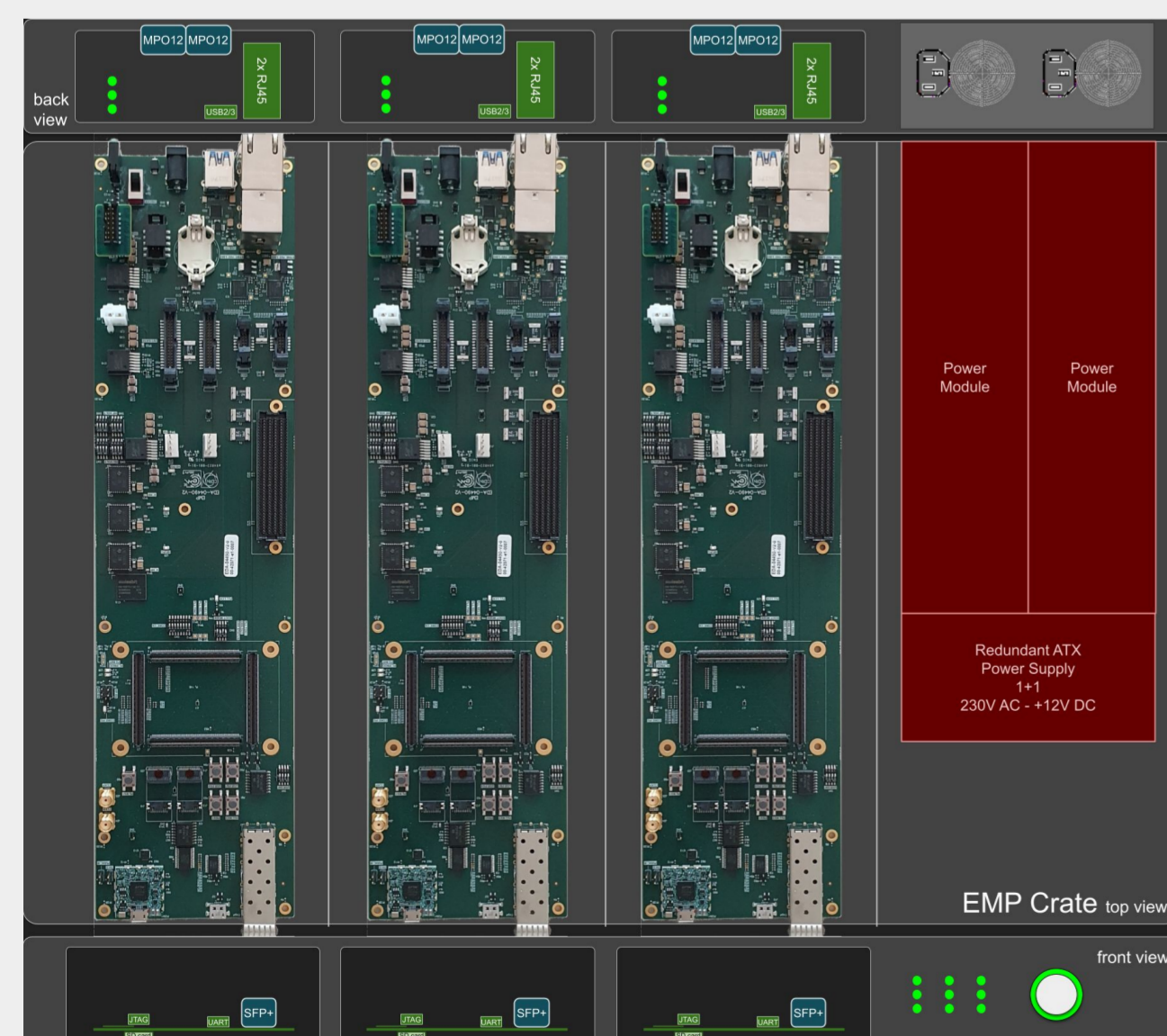
### Benchmarking of the EMCI-EMP eLink communication

- 12 EMCI connected to one EMP configured to loopback downlink eLink frames back to the EMP
- The parallel and synchronized communication between each of the 12 EMCI and the EMP showed a maximum achievable request/reply rate of >20 kHz (peak 8.5 Mbps for payload data) for a register-map based interaction scheme, limited by the Zynq processing system.



### Thermal study

- The EMP is operated in a crate that can host a maximum of three EMPs and one redundant server supply, deployed in a production rack with horizontal backdoor ventilation
- Studies had to be conducted to verify the required cooling of the components and verify crate design.
- The behavior of a fully populated crate was verified during a multi-week test:
  - Study of environmental effects (room and rack temperature) on EMP components
  - Showed that EMPs can be operated well within temperature operation limits of FireFly (50°C) and MPSoC modules (80°C)



## EMP Software & Firmware Architecture

### Objectives for the development of generic Software & Firmware components:

- High level of standardization for DCS interfaces largely reduces development and maintenance effort.
- Reduces user effort to FE-related development

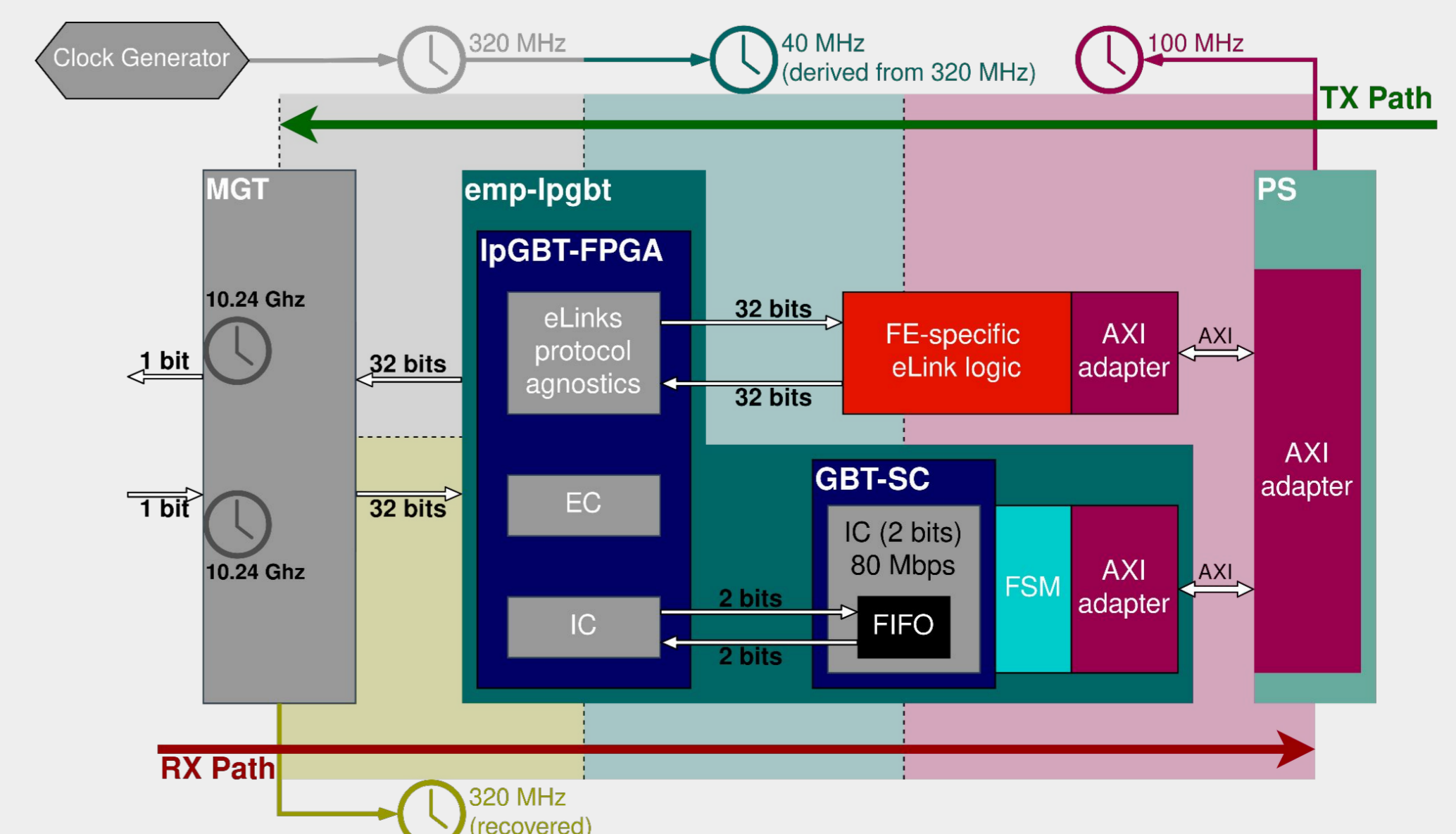
### Software components

- epos - The EMP Operating System**
  - epos-bsp comprises a Petalinux board support package (BSP) defining EMP device tree, Linux kernel configuration and U-Boot configuration
  - epos-rootfs comprises a set of tools to create a CERN IT compliant AlmaLinux9 rootFS for EMP
- Hardware Access Library (HAL) layer**
  - Hardware Access Libraries are APIs to access and control hardware modules from applications.
  - The LpGbtSw provides access to the functionalities of the IpGBT via a polymorphic API for register based interaction, implementing configuration & slow-control interface support (ADC, GPIO, I2C).
  - empTools are a set of software tools to configure, control and monitor EMP peripherals. They interface the EMP firmware via an AXI register map to provide access to monitoring information and reset signals and interfaces the EMP peripherals via standard kernel drivers.
- OPC UA servers**
  - Provide standardized access for DCS back-end software via network, created using the quasar [1] framework
    - FE eLink communication server (needs to be implemented by use case)
    - The IpGBT server
    - The EMP monitoring+configuration server



### Firmware framework

- The EMP firmware framework covers the communication path from the PS (via AXI register maps) to the MGT lanes (connected to the FireFly transceiver modules) and consists of several IP cores:
  - emp-lpGBT IP**
    - PL backend counterpart to the IpGBT ASIC, implementing up-/downlink coding schemas
    - Wraps IpGBT-FPGA [1], GBT-SC IP cores [2] and an IC channel specific AXI adapter & FSM
  - Multi Gigabit Transceiver IP** (for GTH) interfacing 12 FireFly and 1 SFP+ transceiver @ 10.24 Gbps
  - Airhdl [3] register maps**
  - Zynq Ultrascale+ MPSoC IP**
    - Preconfiguration of the Zynq PS (PS-PL communication, MIO definition, Interrupts, ...)
  - eLink interface IP**, an example IP core for eLink benchmarking test



[1] <https://quasar.docs.cern.ch>, [2] <https://gitlab.cern.ch/gbtsc-fpga-support/gbt-sc>, [3] <https://gitlab.cern.ch/gbt-fpga/lpGBT-fpga>, [4] <https://airhdl.com/#/>