Contribution ID: **176** Type: **Poster**

EMCI-EMP: Developments and Experience with the Novel Detector Control Solution

The Embedded Monitoring Processor (EMP) is a state-of-the-art multi-processing System on Chip (MPSoC) based platform, designed for the Detector Control System (DCS) of the ATLAS experiment upgrade. Utilizing the advanced capabilities of the Xilinx Ultrascale+ architecture, the EMP interfaces with the monitoring and control functionalities of its radiation hard front-ends through high-speed optical transceivers. The firmware and software infrastructure comprises the EMP operating system (epos), quasar-based OPC UA servers, a set of firmware IP blocks and associated software libraries that form an integrated ecosystem. This contribution focuses on the current hardware verification and firmware/software developments.

Summary (500 words)

The Embedded Monitoring Processor (EMP) is a state-of-the-art multi-processing System on Chip (MPSoC) based platform, designed to enhance the Detector Control System (DCS) of the ATLAS experiment within the frame of the High Luminosity LHC (HL-LHC) upgrade.
The EMP will serve as an optical link transceiver backbone for non-radiation areas, interfacing with a maximum of 12 optical links towards the detector Front-End (FE) and via an Ethernet interface towards the distributed Supervisory Control and Data Acquisition (SCADA) system. Based on a highly flexible Xilinx Zynq Ultrascale+ architecture, the EMP utilizes the integrated processing platform to run an embedded Linux operating system, allowing easy integration within the control system.
Towards the Front-Ends, the EMP interfaces via optical links with the Embedded Monitoring and Control Interface (EMCI), a novel slow-control module. Based on radiation hard components, as CERN's Low Power GigaBit Transceiver (lpGBT) ASIC, the EMCI will serve as the counterpart of the EMP, enabling a bidirectional communication between various detector FE technologies and the EMP.

With the EMP hardware now available, current efforts can be divided into two domains. The development of a hardware verification test bench to ensure a comprehensive functionality assessment as well as investigation of the thermal behavior of the EMP baseboard components during operation. Initial tests confirmed the heat dissipation of the optical transceivers to be a key challenge to be addressed in order to avoid accelerated aging effects. Furthermore, it has been confirmed that an appropriate air flow provides the desired cooling performance to mitigate these effects. Therefore, a dedicated test was set up to verify the thermal behavior of several EMPs under specific loads within the envisaged production environment.

Current efforts in firmware development aim towards a common firmware framework, offering generic building blocks for the EMP-EMCI communication, self-monitoring capabilities and enabling easy integration of FE-specific logic blocks. These components are brought together in the so-called "emp-reference-project", a firmware that implements the generic uplink and downlink communication with the lpGBT, a general set of lpGBT functions as well as monitoring functions for the firmware itself. One challenge during development was properly implementing Cross Domain Clocking (CDC) circuitry to enable flawless communication between the core logic, transceiver circuits and other interfaces. The integration of the Programmable Logic (PL) with the Processing System (PS) of the MPSoC is achieved through the utilization of an AXI4-lite (Advanced eXtensible Interface) bus protocol, enabling direct control over the implemented firmware functionality from the embedded Linux system.

On the software side, current efforts are focused on generic solutions for the embedded Linux EMP operating system (epos) as well as on common software libraries (lpGBT software, emp-tools) and the adoption of OPC

UA (Open Platform Communications Unified Architecture) as middleware solution towards the DCS Back-End. Exploiting the quasar framework, the full EMP functionality provided via the firmware and onboard peripherals is being mapped into OPC UA servers and integrated by dedicated Hardware Access Libraries (HAL).

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Track Classification: Module, PCB and Component Design