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Optimisation and Validation of Power Delivery Networks for Multi-Gigabit Data Links

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The performance of ASICs for high-bandwidth communications is heavily influenced by the interconnection with the hosting module and paired devices, including the bonding scheme and the PCB layout. The validation campaign of the DART28 high-speed transmitter has highlighted that a coordinated simulation and design of the power delivery network is required to obtain satisfactory performance. In this context, the results obtained from two variants of test-bench board are compared, examining how optimisation of layout and wire-bond placement are reflected in improvements of the serial link characteristics. Electromagnetic simulations support the analysis and provide guidelines for developing the subsequent versions.

Summary (500 words)

In the framework of CERN's Experimental Physics R&D programme, the Electronic Systems for Experiments Group is pursuing the engineering of novel solutions for HEP data transmission in radiation environments. The increased data density, foreseen in future generations of detectors, will require the use of devices that feature high-speed serialisation (25.6 Gb/s), power efficiency, radiation hardness (>10 MGy TID) and low material budget.

The Demonstrator ASIC for Radiation-Tolerant Transmitter in 28 nm (DART28) has been developed to evaluate the compatibility of targeted CMOS technology with the stated objectives. The prototype was delivered in August 2023 and the validation campaign has already delivered promising results. Within the test bench assembled using an initial carrier PCB variant, the system achieved a rise time of 20 ps (10-90%) and a jitter of 250 fs while generating a clock pattern at 12.8 GHz. These values confirmed that the implemented output driver does not constitute a bandwidth limitation.

Subsequently, different test patterns, including PRBS, were transmitted to simulate the conditions of real use cases. This revealed an observable degradation of the eye diagram characteristics, which would worsen with the maximum run length of the sequence transmitted. Therefore, a study of the possible causes was undertaken, which involved joint simulations of the ASIC, the bond wire scheme, and the PCB layout. It attributed the issue to current transients caused by the lane driver, which result in a peak-to-peak voltage ripple of tens of millivolt on the main supply rail (0.9V). This leads to the modulation of the output delay, introducing data-dependent jitter.

The first solution explored concerned the development of a variant of the carrier board, equipped with more extended power planes in proximity to the device under test. According to the simulations, the new layout would allow an improvement of signal quality, benefiting the continuation of characterisation. Although the number of accessible lanes has been reduced to only one out of the four provided by the device, such a solution proved effective. In particular, the eye jitter was reduced by ˜30% while transmitting a PRBS7 pattern.

The comparison of measurements is reported together with the procedures and models adopted for the electromagnetic simulations. These can offer an effective way for approaching signal and power integrity problems on co-designed assemblies and adopting appropriate mitigation techniques. Consequently, the performance of the system can be predicted, while costs and lead time can be reduced compared to a purely hardware based investigation.

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