

Development of a Test System for Data Links of the ATLAS Inner Tracker (ITk) Upgrade Silicon Pixel Detector



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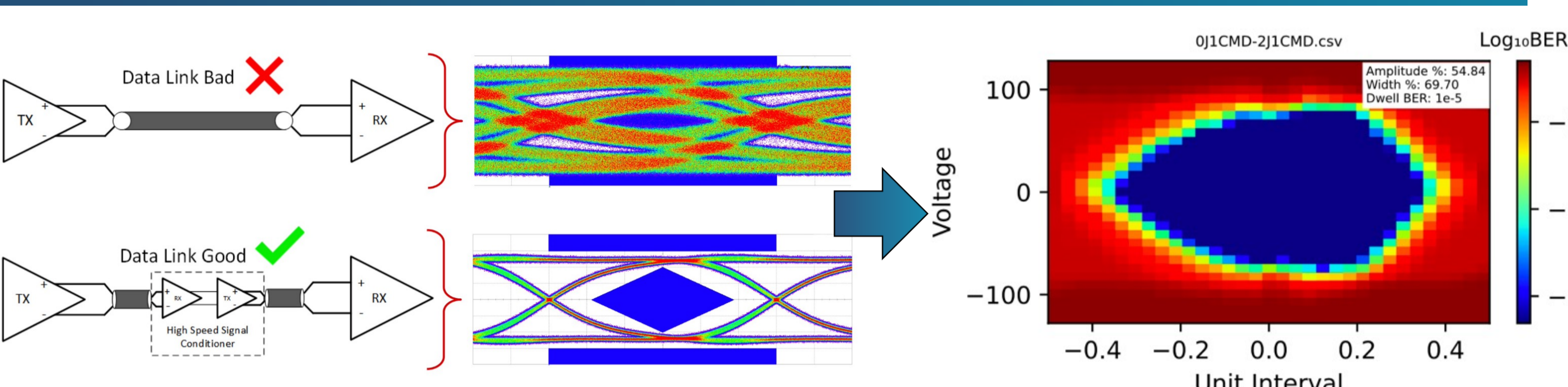
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1. Introduction

The ATLAS experiment 2026 Inner Tracker (ITk) upgrade will include silicon pixel detectors, requiring high-bandwidth readout. A total of approximately or up to 26,000 CMD and data links, operating at a rate of 1.28 Gbps, will be needed to read out the three ITk subsystems (Outer Endcaps, Outer Barrel and Inner System). The high-irradiation environment requires up to six-meter-long copper links between the front end and conversion to optical signals. The links must be of the lowest possible mass, radiation hard and match the allocated signal loss budget of 13dB at 640MHz. Custom developments of gauge 34 AWG Twinax cables with polyethylene dielectric and aluminium shield have been demonstrated to fulfil the specifications. The signal loss of readout chain elements in single links has been validated using eye diagrams on fast oscilloscopes, a method unsuitable for testing all ITk links. The work presented the development of an FPGA-based data acquisition system capable of conducting simultaneous Bit Error Rate (BER) tests and recording virtual eye diagrams for up to 32 links per connected assembly, scalable to test multiple assemblies at the same time, at the ATLAS ITk pixel data rate of 1.28Gbps.

2. Eye Diagram & Bit Error Rate (BER)



- ❖ Illustrates the quality of signal transitions between **0 and 1** values by overlaying multiple signals during transmission.
- ❖ Evaluates high-speed data quality and high-speed transmitter/receiver performance.
- ❖ **The BER** is characterised by the ratio of incorrectly received bits to the total transmitted bits.
- ❖ Provides similar transmission outputs, however faster and more productive than eye diagram analysis.

4. Vector Network Analyser (VNA) & Matrix Conversion

The aim is to define the correlation between **insertion loss (dB)** and the **time/voltage offsets** of the virtual eye diagram.

N9918A FieldFox 2-Channel VNA was employed to characterize these cables.

Matrix conversion (mixed mode S-parameters) method is used to find the loss of the differential links [1].

Differential Pair

$$SDD21 = \frac{1}{2} (S21 - S23 - S41 + S43)$$

Mixed-Mode		Common-Differential	
Differential-Differential	SDD11	SDD12	SDC11
Differential-Differential	SDD21	SDD22	SDC21
Differential-Common	SCD11	SCD12	SCC11
Differential-Common	SCD21	SCD22	SCC21

Figure 5: Mixed-Mode Differential Pair Matrix

5. Results

Analyzing the **channel-by-channel variation of signal loss** for the calibration of the QC test system channels.

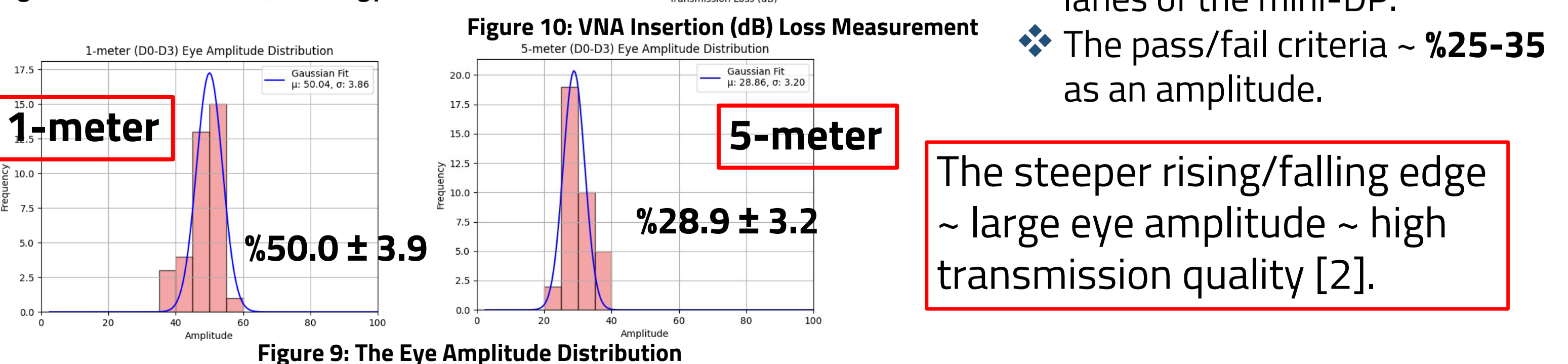
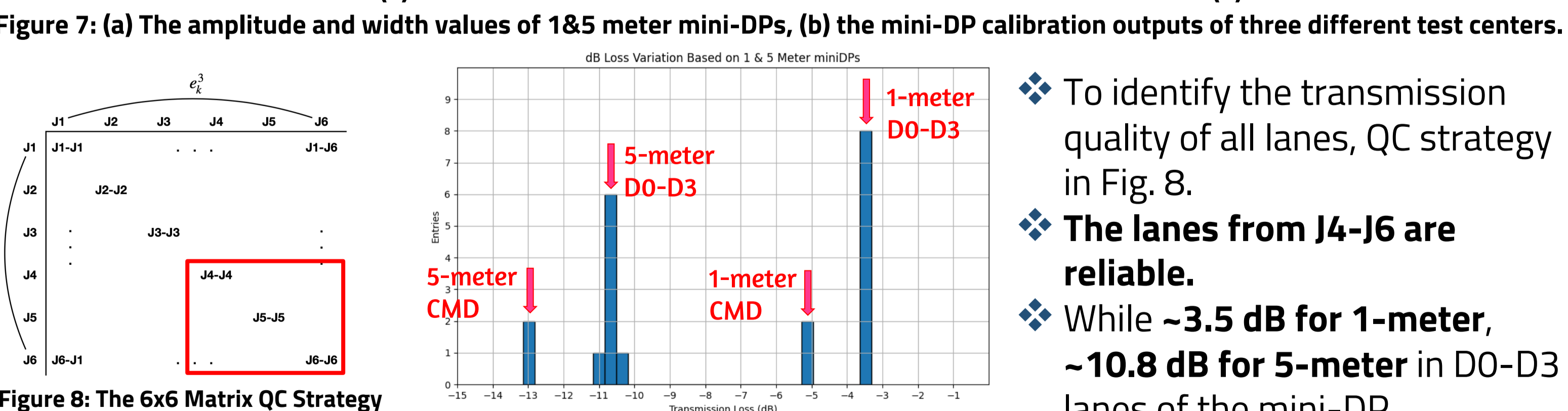
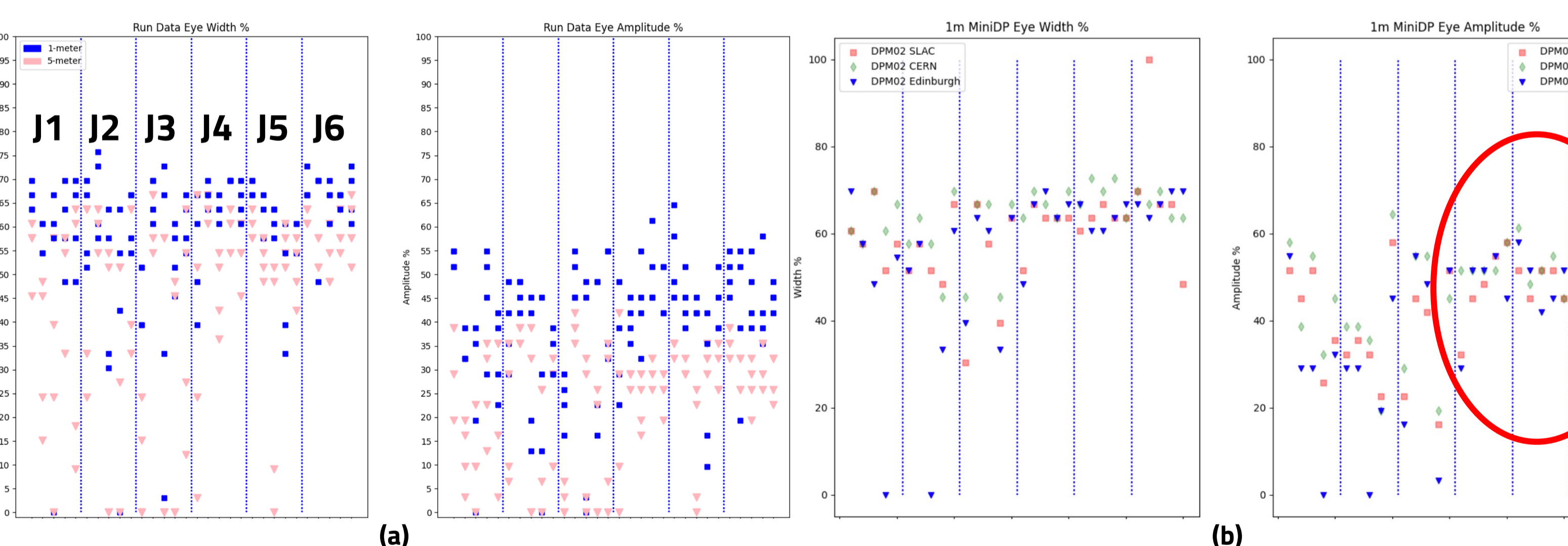
DUT → Industry-standard **mini-DP cables** of various lengths.

Each mini-DP has **five lanes**,

- ❖ CMD-CMD, D3-D0, D2-D1, D1-D2 and D0-D3

The total test time **~10mins**.

- ❖ The calibration / finding out the weak & unsuitable channels of the DAQ channels in Fig 7.
- ❖ **J4-J6 channels have high transmission quality.**



3. Multi-channel DAQ FPGA-based Framework

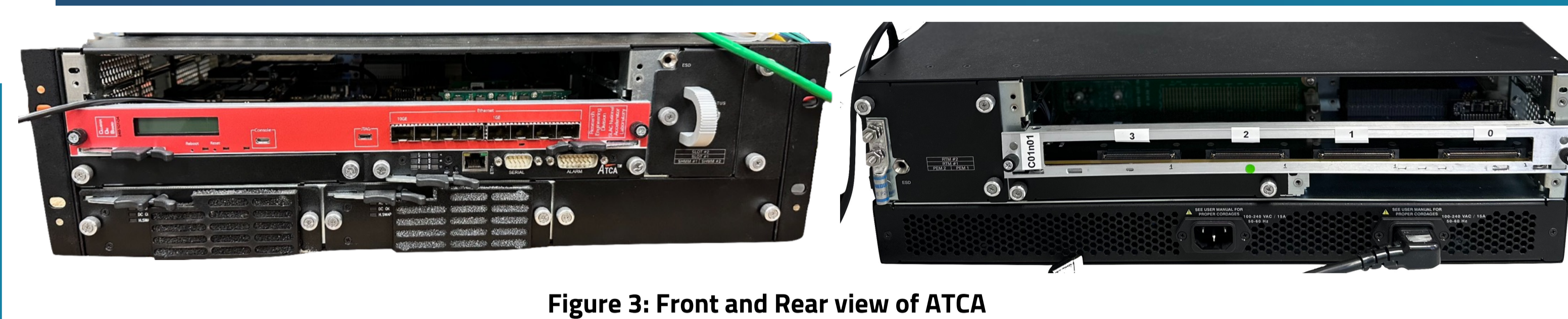


Figure 3: Front and Rear view of ATCA

- ❖ Created with an **Advance Telecommunication Computing Architecture** system which is a custom system.
- ❖ The advantages: redundancy, hot swap, easy integration COBs and RTMs

Cluster on Board (COB):

- ❖ Reconfigurable Cluster Element (**RCE**): System-on-chip design based upon the Xilinx Zynq family of FPGAs.
- ❖ Data Processing Module (**DPM**):
- ❖ Data Transmission Module (**DTM**):
- ❖ External trigger system

Rear Transmission Module (RTM):

- ❖ Each RCE node receives data from experiments via high-speed serial links through an RTM.
- ❖ Experiment specific
- ❖ **4 channels (DPM0 - DPM1 are TX / DPM2 - DPM3 are RX)**
- ❖ Connection with RTM provided by Device Under Test (DUT) specific adapters.

Figure 4: Cluster on Board (COB)

DUT (Type-1 Twinax Bundle) Connection

- ❖ The DUT changes to **Type-1 Data links** sample.
- ❖ FF1 3040 ± 10 mm, FF2 3150 ± 10 mm.
- ❖ Each FF has **10 links (CA1-CA5 / CA7-CA12)**.
- ❖ The total test time **~6mins**.

Figure 11: DUT (Type-1 Twinax Bundle) Connection

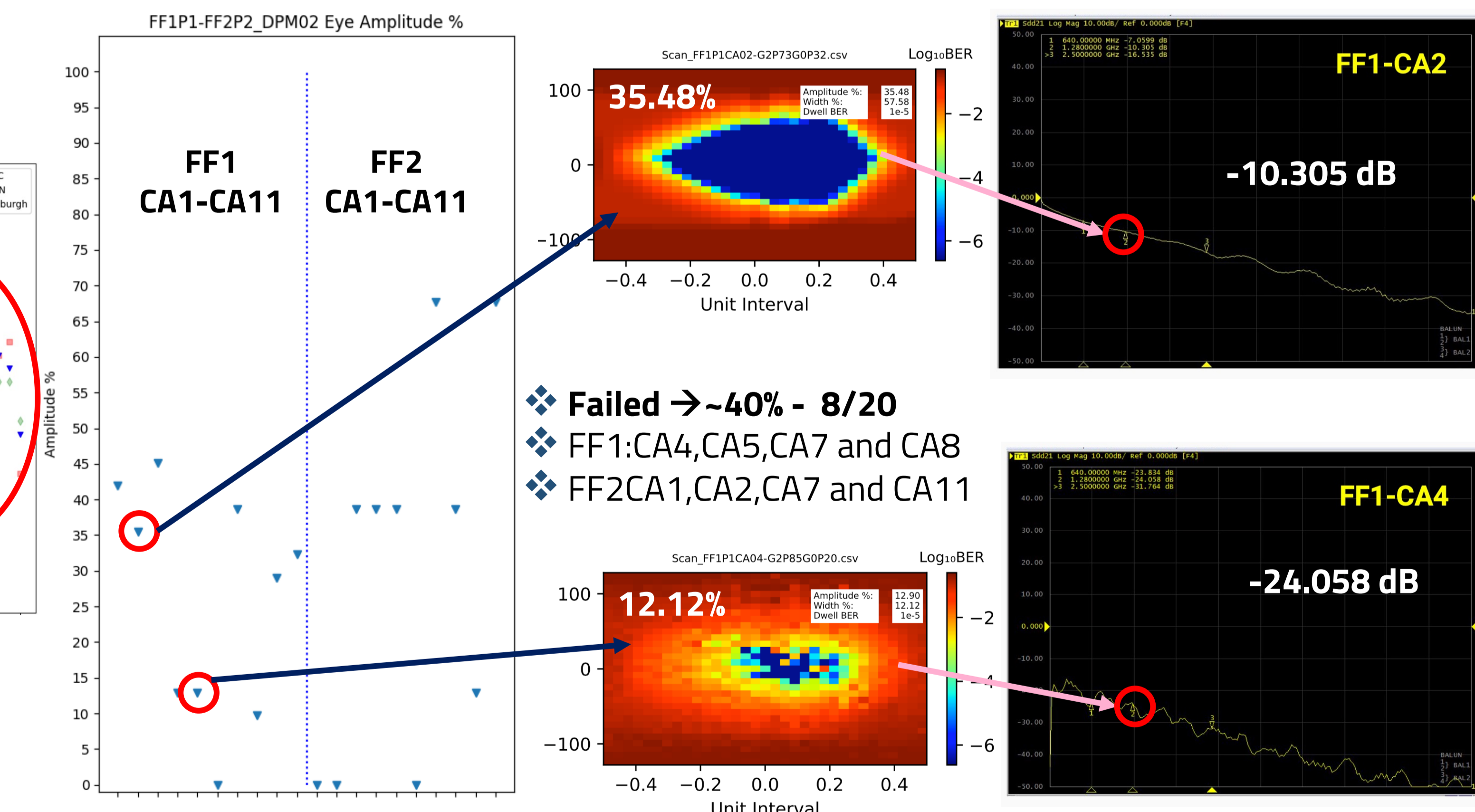


Figure 12: Eye Diagram vs Insertion (dB) Measurement on Type-1 Data Links

6. Conclusion & Further Plans

- ❖ The proposed DAQ system has been tested in three different locations and **gives parallel outputs**.
- ❖ The calibration of DAQ channels, **usable channels found out**.
- ❖ **Parallel correlation between insertion (dB) loss/amplitude of eye diagram.**
- ❖ The first prototype of Type-1 data bundle tested **based on pass/fail condition**, pin solders do not have good quality.
- ❖ **The further plan:** assembly will be done by **laser-stripping method**.

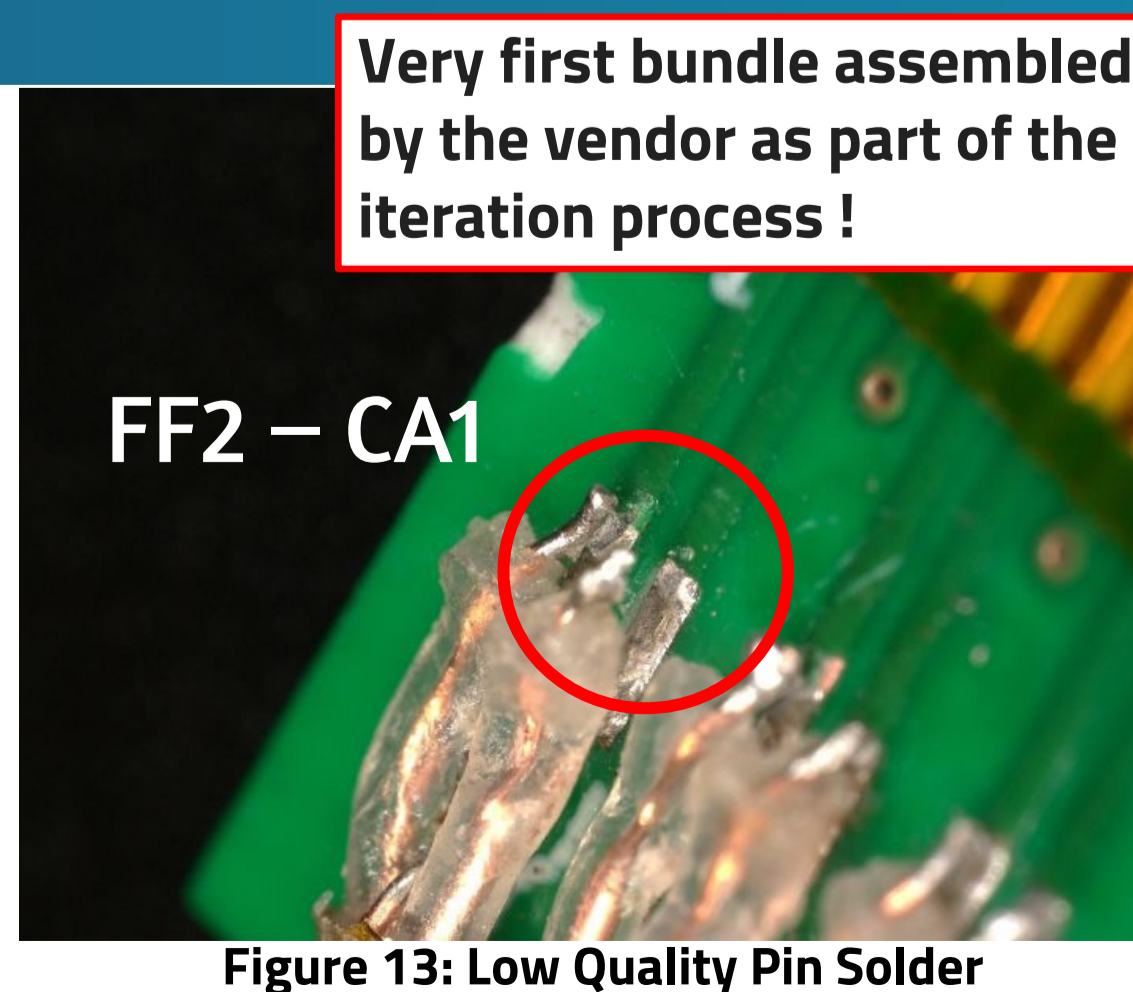


Figure 13: Low Quality Pin Solder

References

- [1] Z. Wang, J. Gao, G. T. Flowers, G. Xie and R. Ji, "The Impact of Electrical Contact Degradation on Differential Signal Transmission of High-Speed Channel," 2018 IEEE Holm Conference on Electrical Contacts, Albuquerque, NM, USA, 2018, pp. 340-346.
- [2] E. Bogatin, Signal and Power Integrity: Simplified, 2nd Edition Edited, Electronics Industry Press, 2015.