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Development of a Test System for Data Links of the ATLAS Inner Tracker (ITk) Upgrade Silicon Pixel Detector

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This contribution introduces a novel test system developed to evaluate the signal transmission quality in high-speed data links for the 2026 Inner Tracker upgrade of the ATLAS experiment. Using an FPGA-based data acquisition framework, the setup can run simultaneous Bit Error Rate (BER) tests for many channels and generate virtual eye diagrams, for qualifying the ~26K electrical links of ATLAS ITk, data rate of 1.28Gbps. The presentation will include results from system calibration yielding its contribution to the measured losses, and preliminary results from tests of prototype and pre-production assemblies of on-detector links of the three ATLAS ITk Pixel subsystems.

Summary (500 words)

The ATLAS experiment 2026 ITk upgrade will include silicon pixel detectors, requiring high-bandwidth read-out. A total of O(26k) CMD and data links, operating at a rate of 1.28Gbps, will be needed to read out the three ITk subsystems (Outer Endcaps, Outer Barrel and Inner System). The high-irradiation environment requires up to six-meter-long copper links between the front end and conversion to optical signals. The links must be of the lowest possible mass, radiation hard and match the allocated signal loss budget of 13dB at 640MHz. Custom developments of gauge 34 AWG Twinax cables with polyethylene dielectric and aluminium shield have been demonstrated to fulfil the specifications. The signal loss of readout chain elements in single links has been validated using eye diagrams on fast oscilloscopes, a method unsuitable for testing all ITk links.

The work presented comprises the development of an FPGA-based data acquisition system capable of conducting simultaneous Bit Error Rate (BER) tests and recording virtual eye diagrams for up to 32 links per connected assembly, scalable to test multiple assemblies at the same time, at the ATLAS ITk pixel data rate of 1.28Gbps. The system allows for simultaneous BER tests of all connected cable assemblies at the canonical setting for link establishment, within a few minutes. More detailed Quality Control (QC) of Twinax link eye diagrams then follows link-by-link, by scanning across time/voltage offsets using the Xilinx iBERT utility, constructing a map of BER tests, in less than a minute per link. The resulting virtual eye diagram offers insight into the signal loss of the tested link but requires further calibration to obtain quantitative results.

Re-using an existing multi-channel data acquisition FPGA-based framework consisting large number of MGTs supporting iBERT presents some challenges in this work. They can be detailed as the implementation of the BER tests, the development of the scanning, the design and validation of a new I/O unit and custom interfaces, the automation of the tests and the handling of various flavours of link assemblies, and the calibration of the test system.

The presentation will report preliminary results from the test systems set up by the ITk Pixel collaboration at SLAC, CERN, Edinburgh and Göttingen, covering the QC test needs of the ITk subsystems. The channel-by-channel variation of the signal loss by the components of the QC test system has been studied using industry-standard mini-DP cables with various lengths which in turn were characterised by a Vector Network Analyser to define the correlation between the signal loss and time/voltage offsets of the virtual eye diagram. With prototype and pre-production assemblies now available, pass/fail criteria for the ITk Twinax assemblies are currently under development, correlating the parameters extracted from the virtual eye diagrams to the acceptable level of signal loss in the Twinax links.

The presentation will include the latest results from tests on ITk Twinax pre-production assemblies and show how the test systems will enable the ITk Pixel collaboration to perform the QC testing on the quantities of Twinax assemblies needed for the full production.

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