3D Integration of Pixel Readout Chips using Through-Silicon-Vias

TWEPP-2024

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[1]CERN
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[3]UniGe

Supported by CERN EP R&D WP5 and the Medipix4 Collaboration

Outline

1. Through-Silicon-Via (TSV) Overview
2. Why TSV in Particle Detectors
3. TSV Processing of Timepix4
4. Module Design to Test TSV
5. First Results and Future Work

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1. Through-Silicon-Via (TSV) Overview

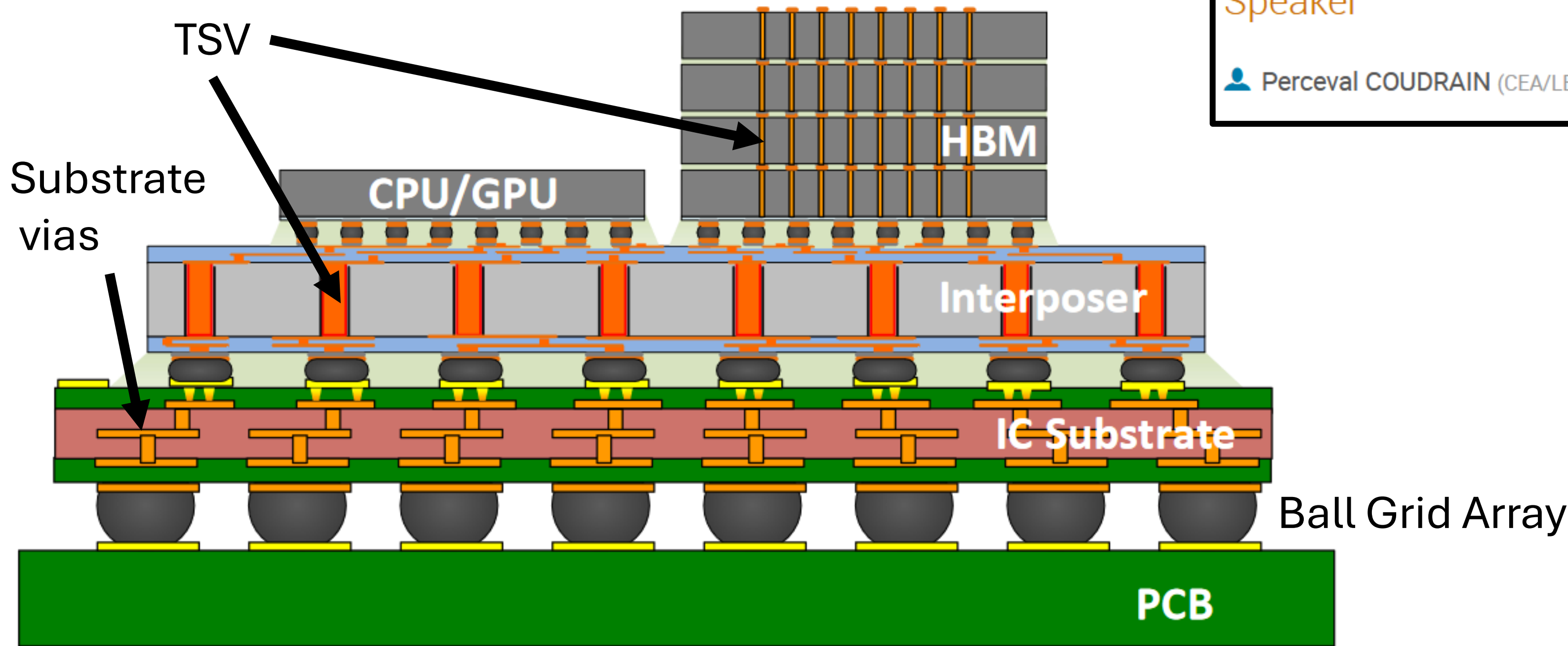
- Similar to PCB vias, but in silicon
- Three types: first, middle, **last**
- For our ASIC technology of today, only TSV-Last is feasible

Redefining electronic boundaries with 3D integration and advanced packaging

Oct 3, 2024, 10:30 AM
45m

Speaker

Perceval COUDRAIN (CEA/LETI)



TSVs allow 3D stacking

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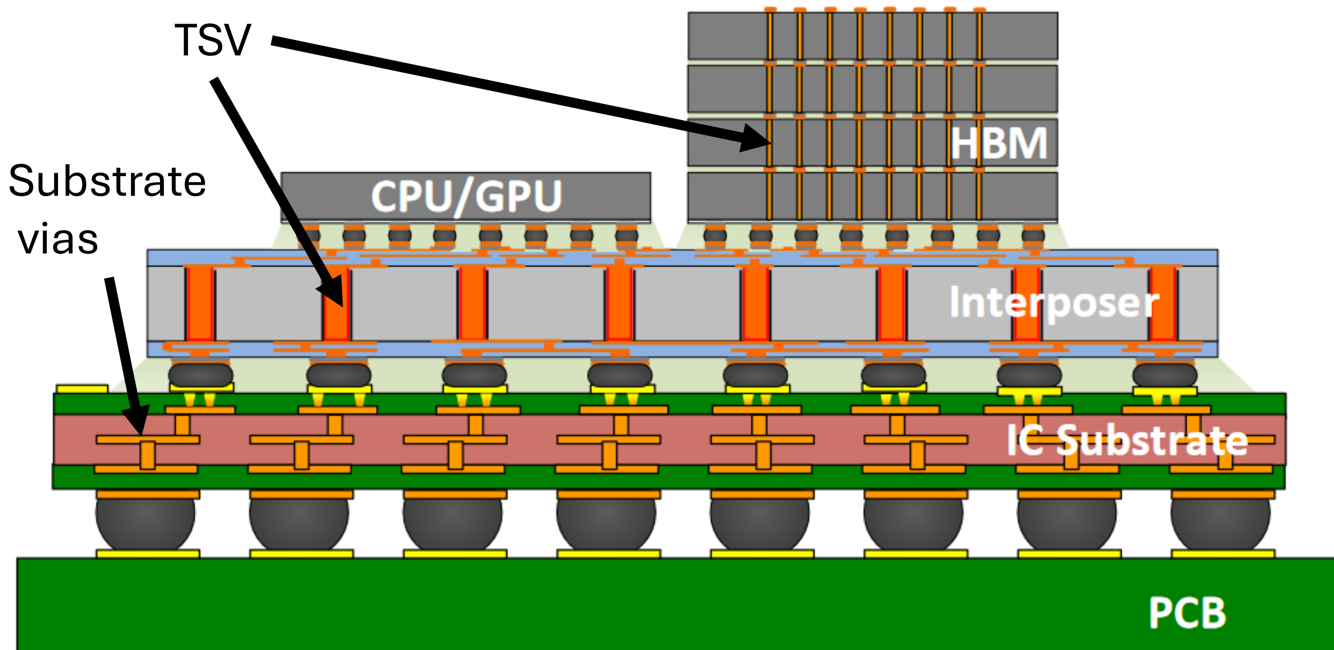

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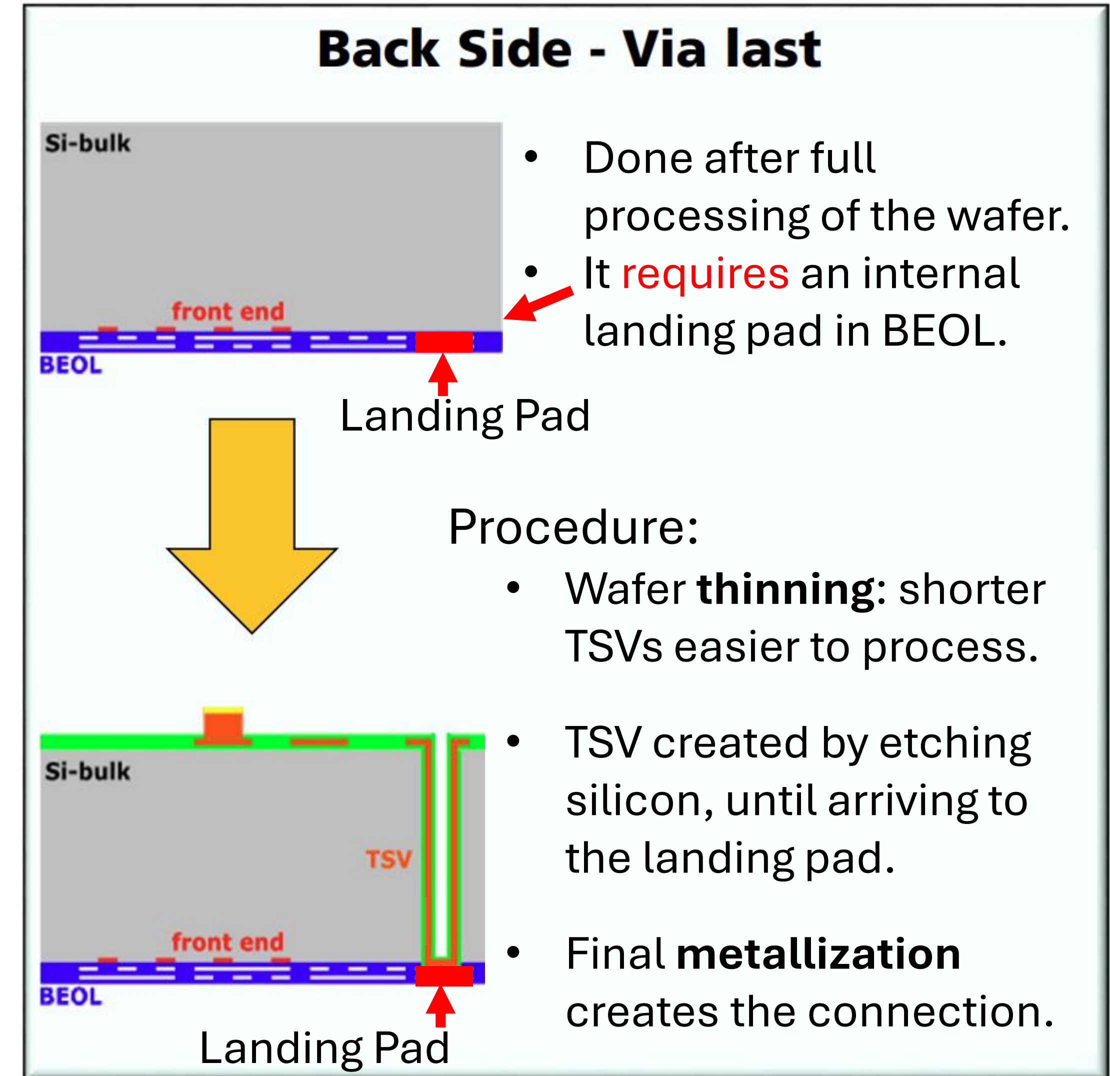

(Fraunhofer, CERN EP-ESE Electronics Seminars, April 12th, 2022)

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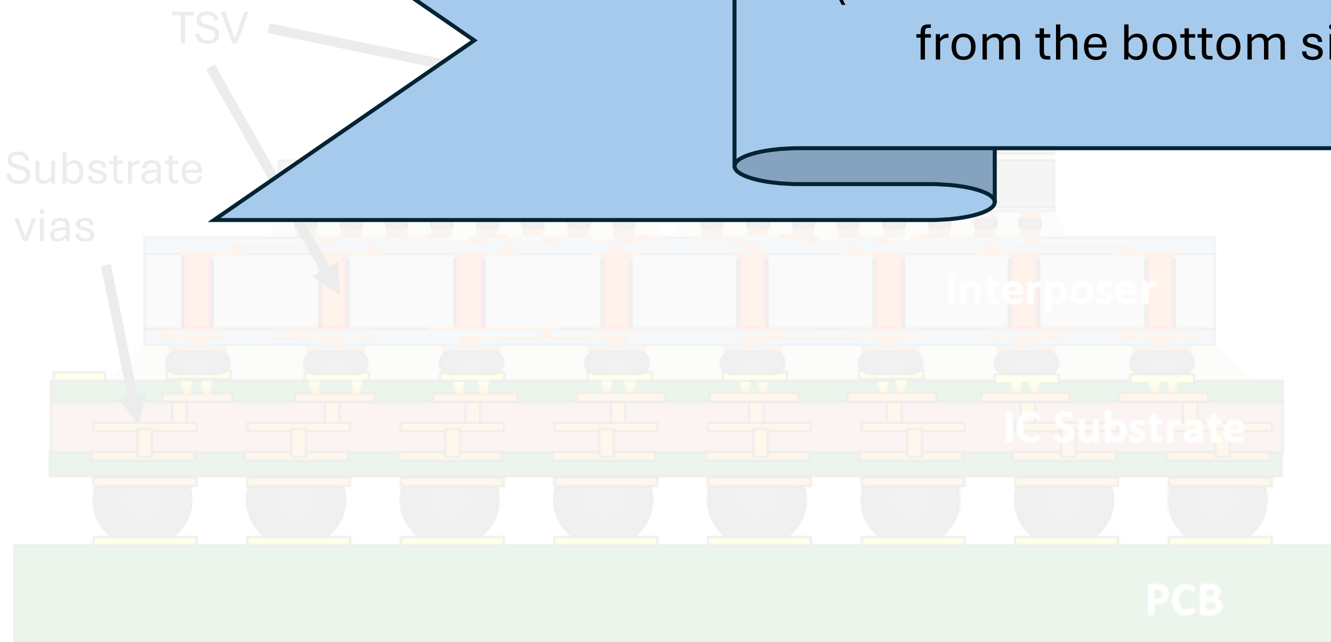

TSVs allow 3D stacking

Back Side - Via last

- Done after full processing of the wafer.
- It requires an internal ... BEOL.
- ...ning: shorter ... process.
- TSV created by etching silicon **(Bosch Process)**, until arriving to the landing pad.
- Final **metallization** creates the connection.

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Main idea

Accessing the active circuitry (located on the front side of the chip), from the bottom side surface.

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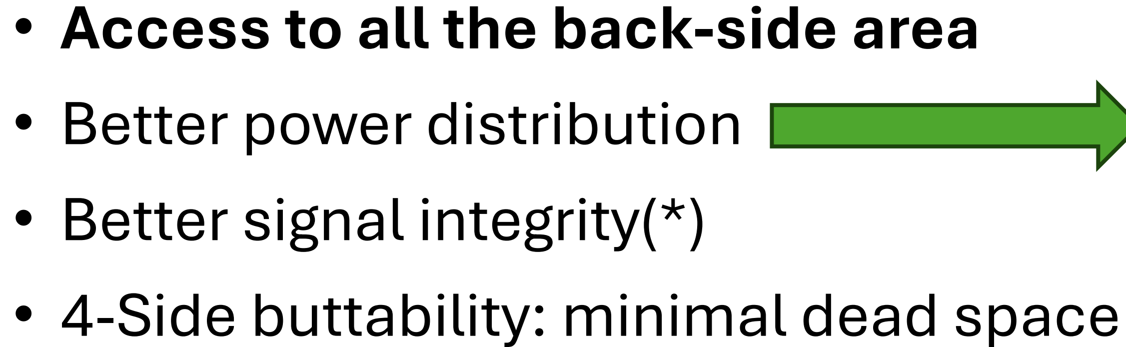
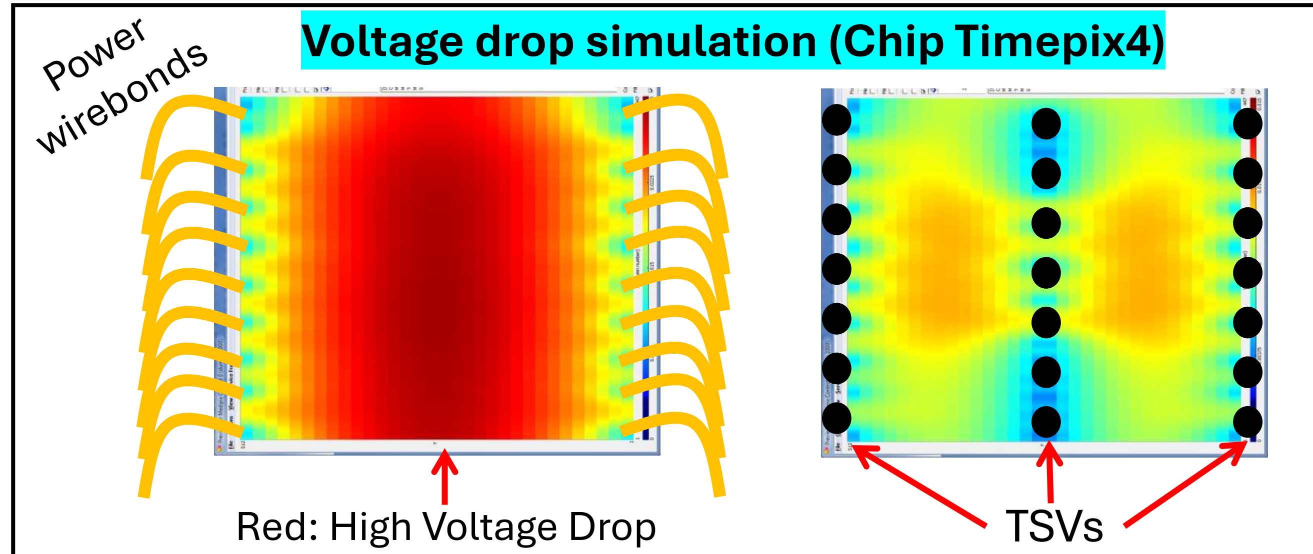
2. Why TSV in Particle Detectors

- **Access to all the back-side area**
- Better power distribution
- Better signal integrity(*)
- 4-Side buttability: minimal dead space





(*) G.Druais et al, *TSV as an alternative to wire bonding for a wireless industrial product: another step towards 3D integration*

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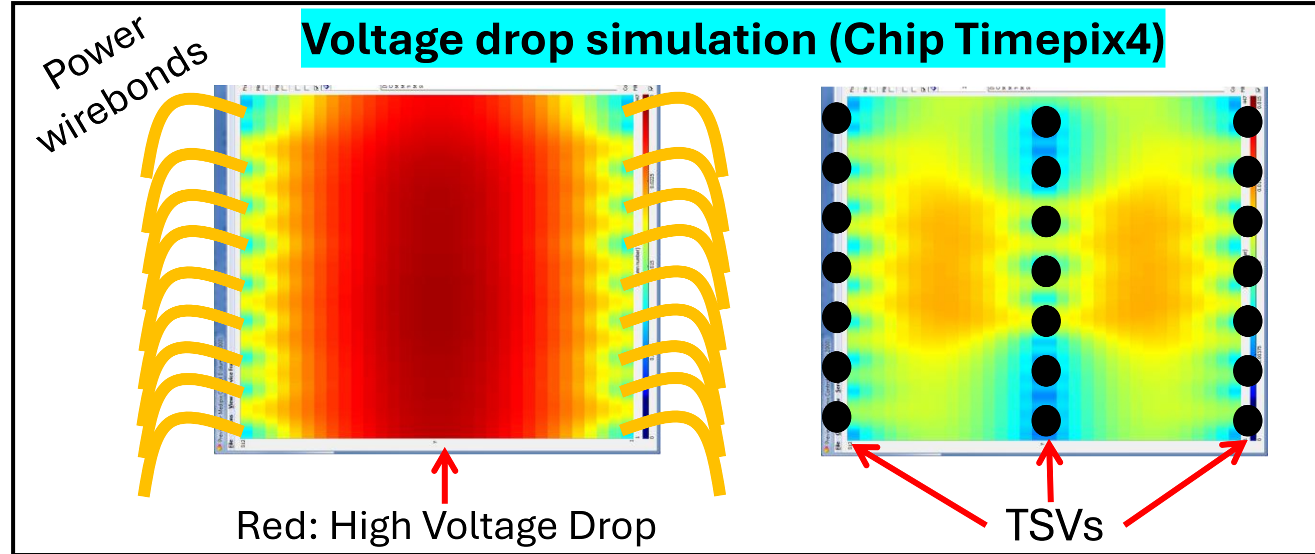

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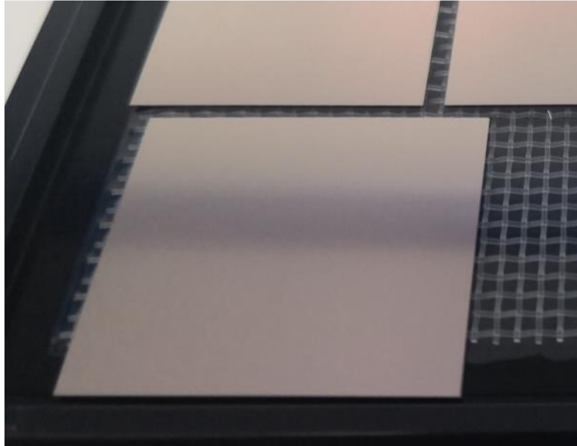
Timepix4: Our test-vehicle for TSV



Timepix4: Hybrid pixel detector

- 29x24mm = almost 7cm^2 sensitive area
- 512x448 pixels
- 16 links up to 5Gbps

Why Timepix4 as test vehicle?

- Wirebond and Ball Grid Array (BGA) dicing options
- Four-side buttability (without bondpads)
- Internal landing pads in Metal 1 ready for TSV

Data

TOP edge Periphery

223 2 1 0

Periphery with data, power and clocks

SPGroup

0 1 15

TOP Matrix
[448 x 256]

0 1 2 221 222 223

Center Periphery

0 1 2 221 222 223

Periphery with power and clocks, **accessible only with TSV**

15 14 0

BOTTOM Matrix
[448 x 256]

0 1 2 221 222 223

BOT edge Periphery

Periphery with data, power and clocks

Data

3. TSV Processing of Timepix4

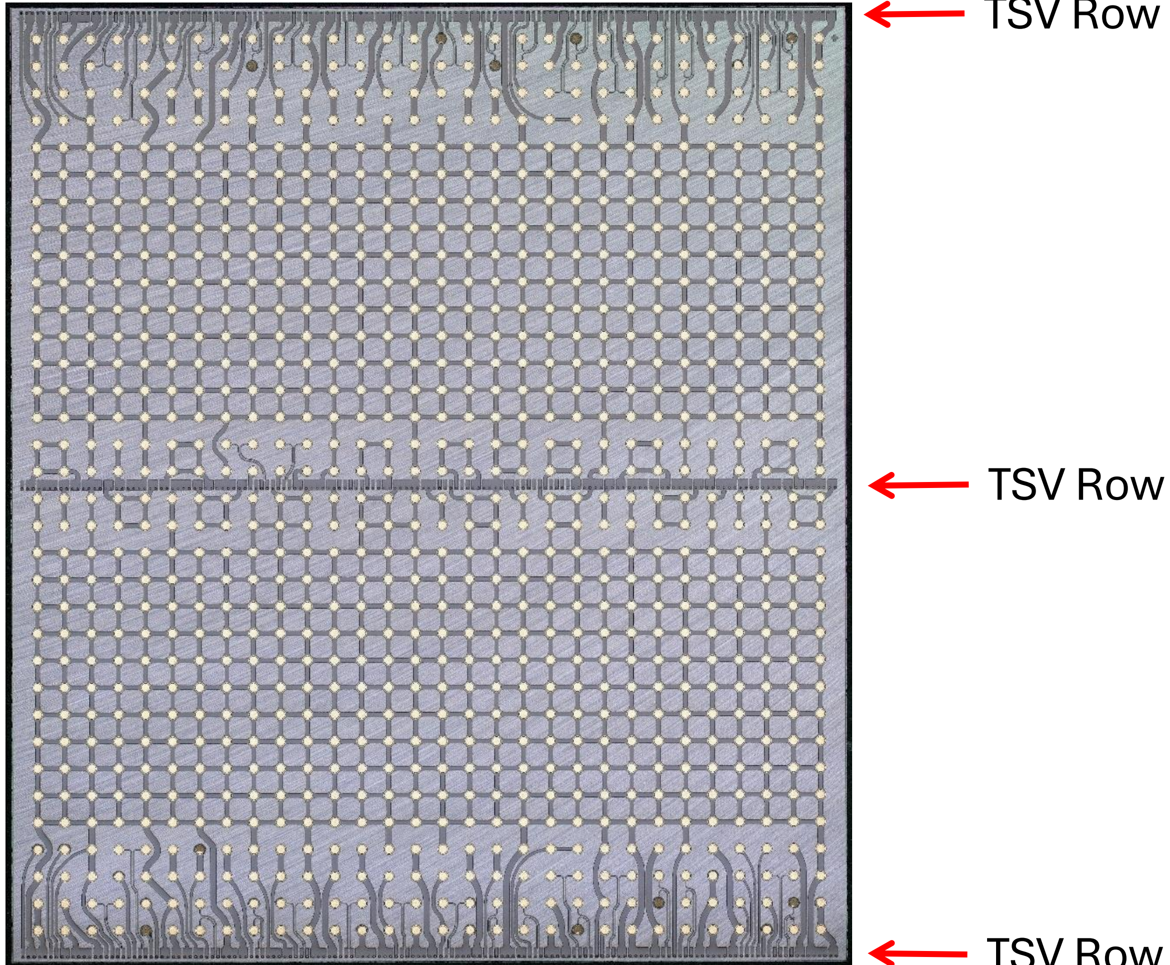
Timepix4 Version	V0	V1	V2 / V3
Considerations	**Excessive jitter** in data links, due to PLL not locking properly. **Chip for electrical tests.**	Same problems on data links as V0. **Chip for electrical tests.**	Versions with PLL problem solved. **Links working at 5Gbps at nominal voltage.**

IZM Fraunhofer TSV Processing:	Two wafers 200mm done	Two wafers 200mm done	Three V3 wafers 200mm **Ongoing TSV processing**

3. TSV Processing of Timepix4

TIMEPIX4 TSV-Processed Back side

Chip thinned to ~120um



TSV Row

TSV Row

TSV Row

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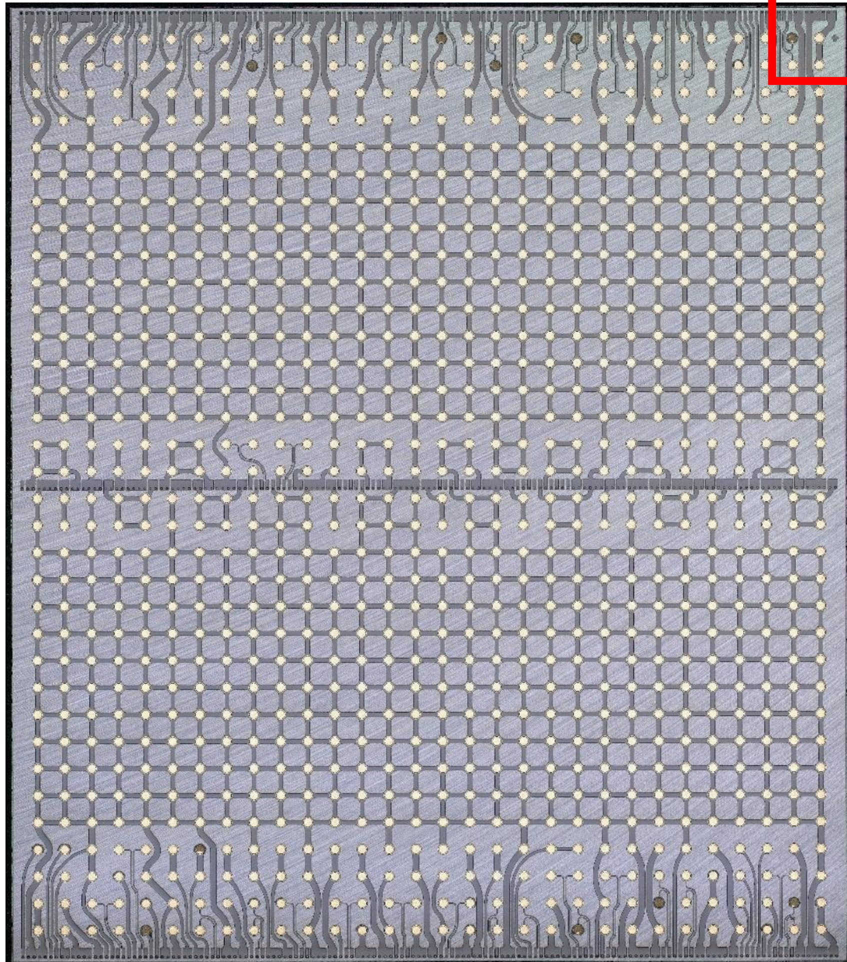

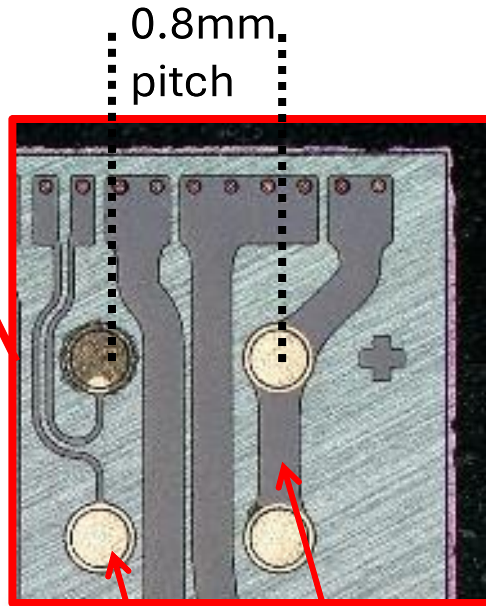

0.8mm pitch

x1020 BGA Pad
Diameter: 300 um

Redistribution
Layer (RDL)

The bondpads are diced out: 4 side buttability

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TIMEPIX4 TSV-Processed Back side

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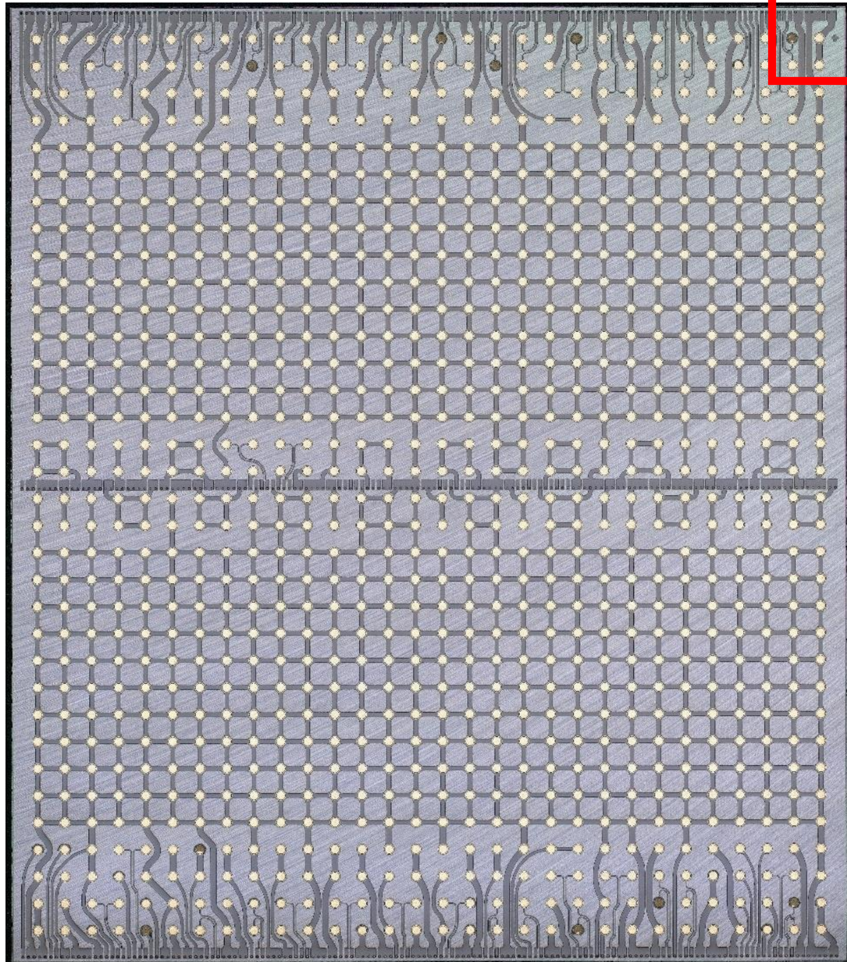

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Through Silicon Via (TSV)

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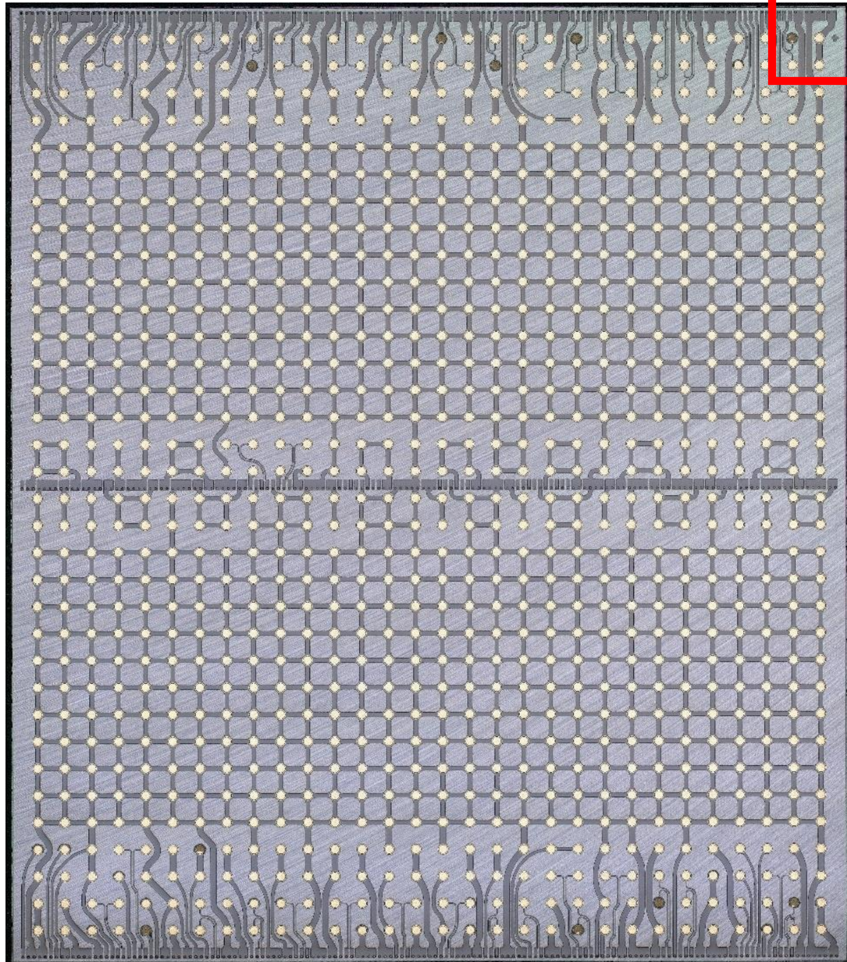

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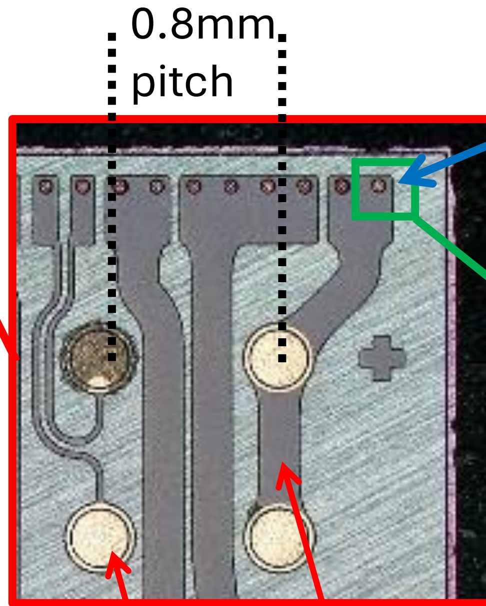

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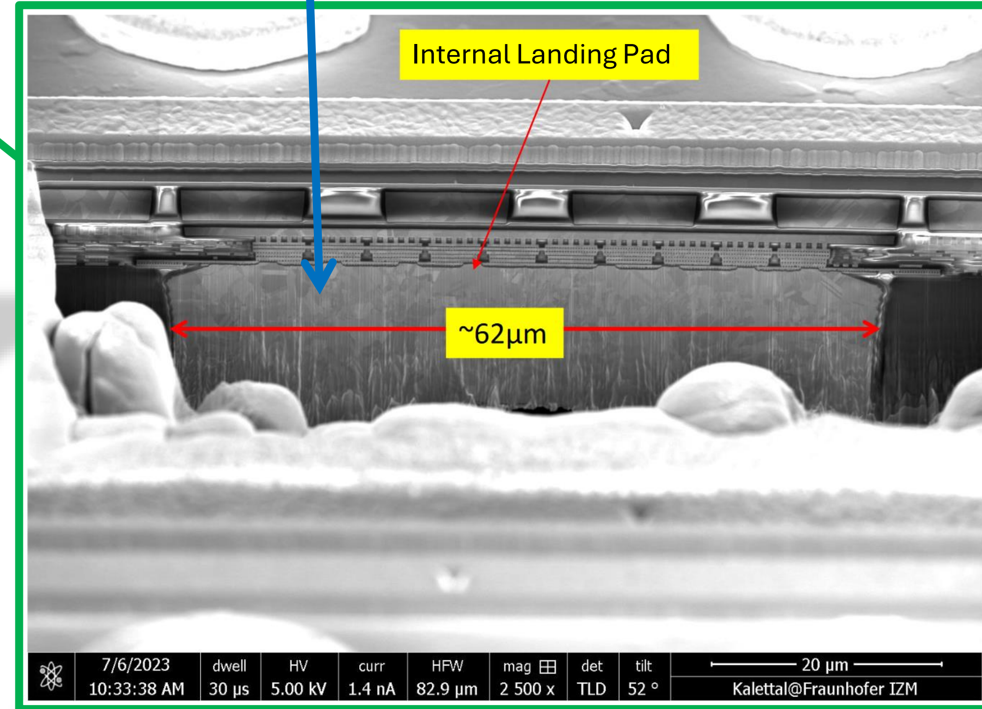


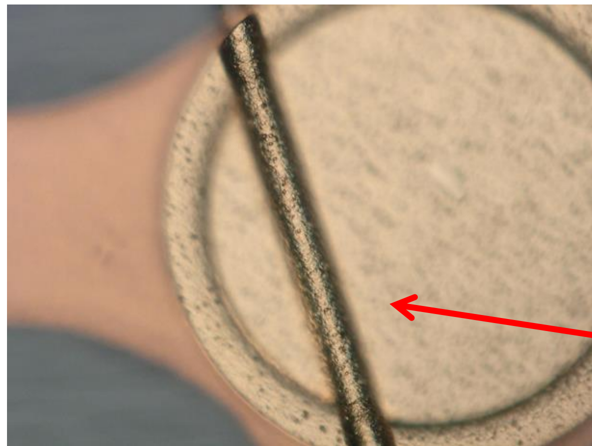
TSV cross section under SEM (Fraunhofer IZM)

The bondpads are diced out: 4 side buttability

3. TSV Processing of Timepix4

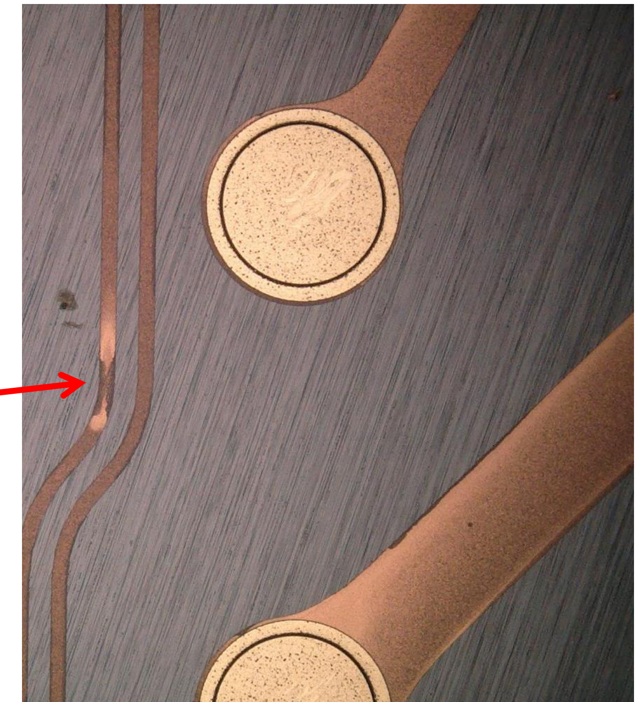
Some difficulties:

- Setup by trial and error: some wafers are consumed for setup
- Wafer level processing
- Post processing for balling
- Defects in RDL or pixel matrix (not common)
- **Visual inspection and good handling is important**



Metal deposition over defects

Damaged track



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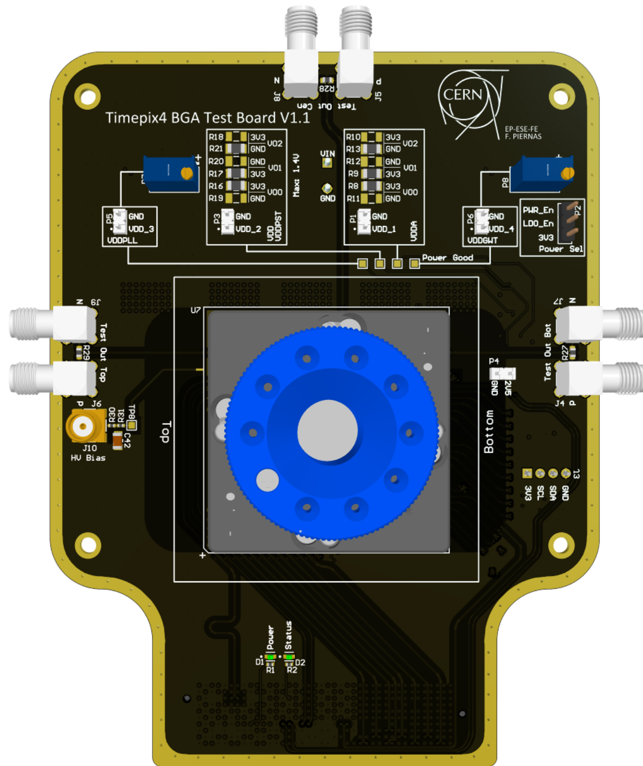
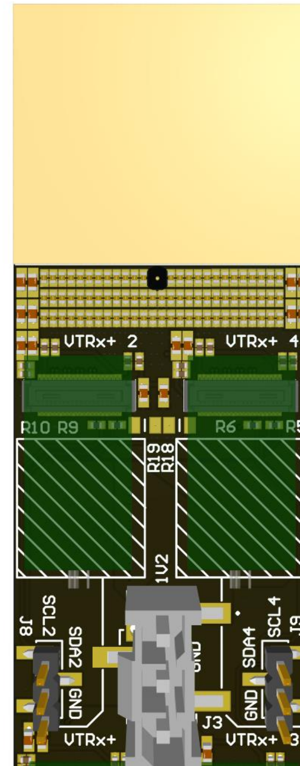
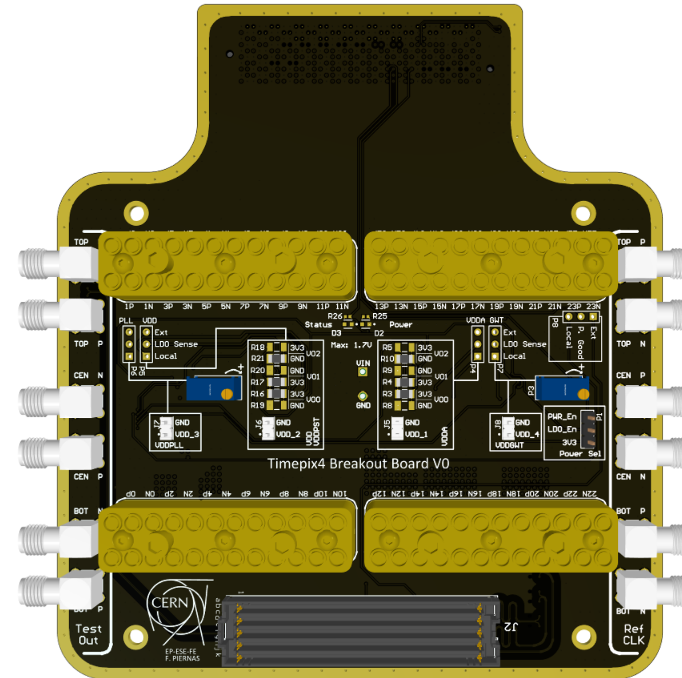
Family of PCBs for testing TSV-processed Timepix4



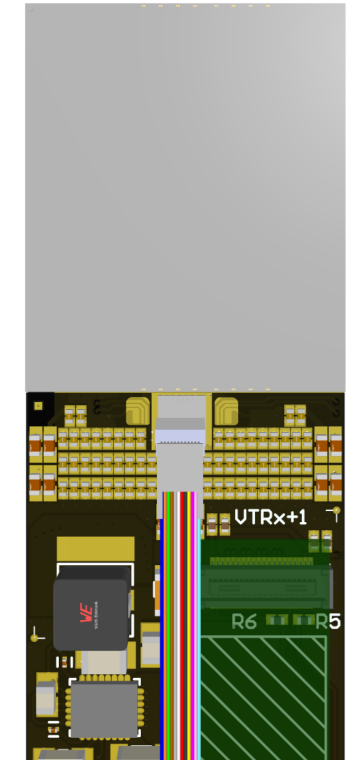
Socket PCB
Electrical Tests



Timepix4 & VTRx+
Optoelectronics Demonstrator



Breakout PCB
Extracting data links and clocks through SMA cables



Timepix4 & SystemPIC
Silicon Photonics

More in progress…

4. Module Design to Test TSV

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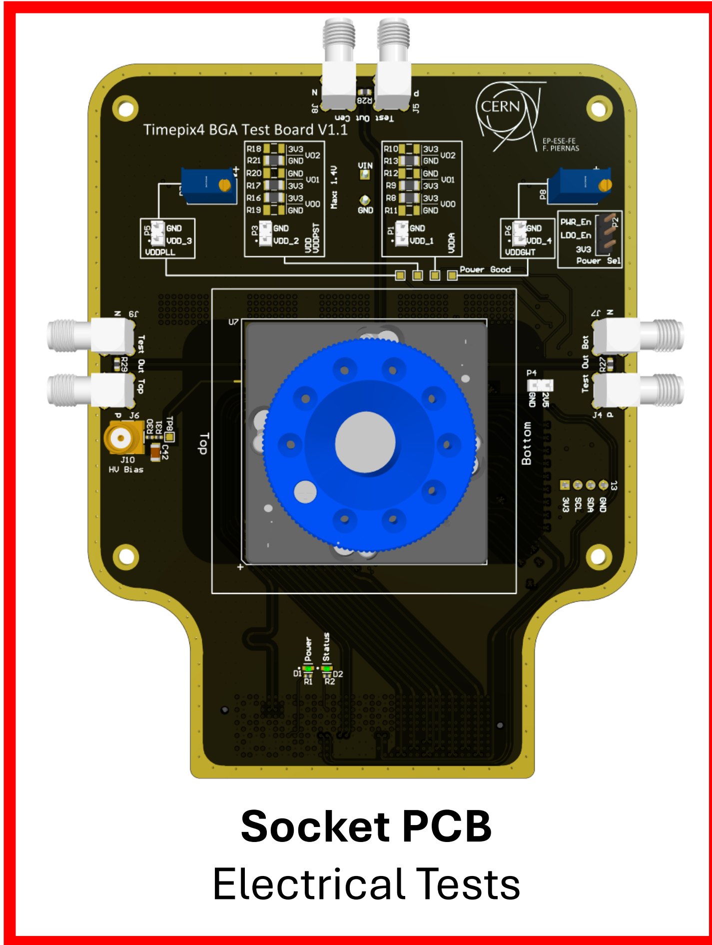

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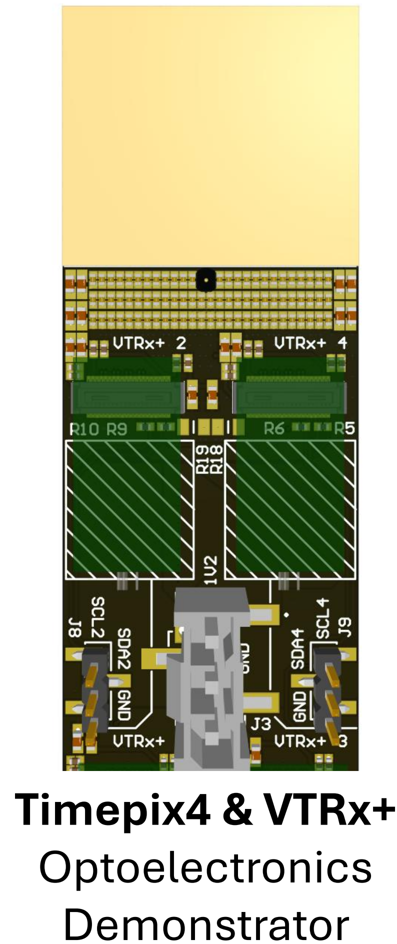

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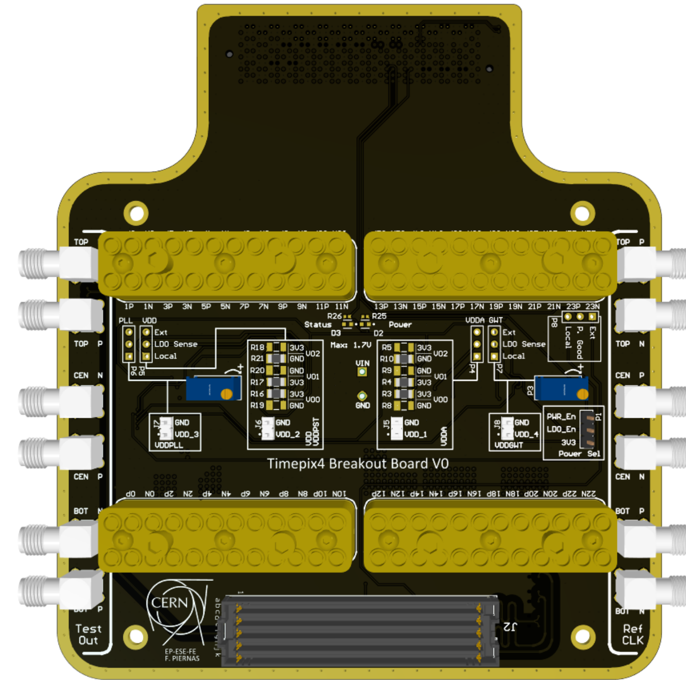

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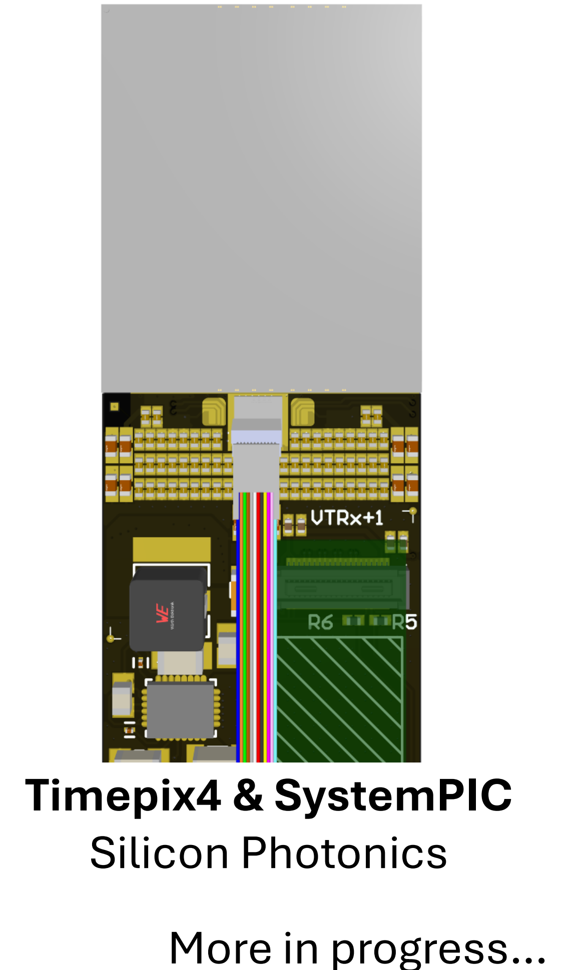

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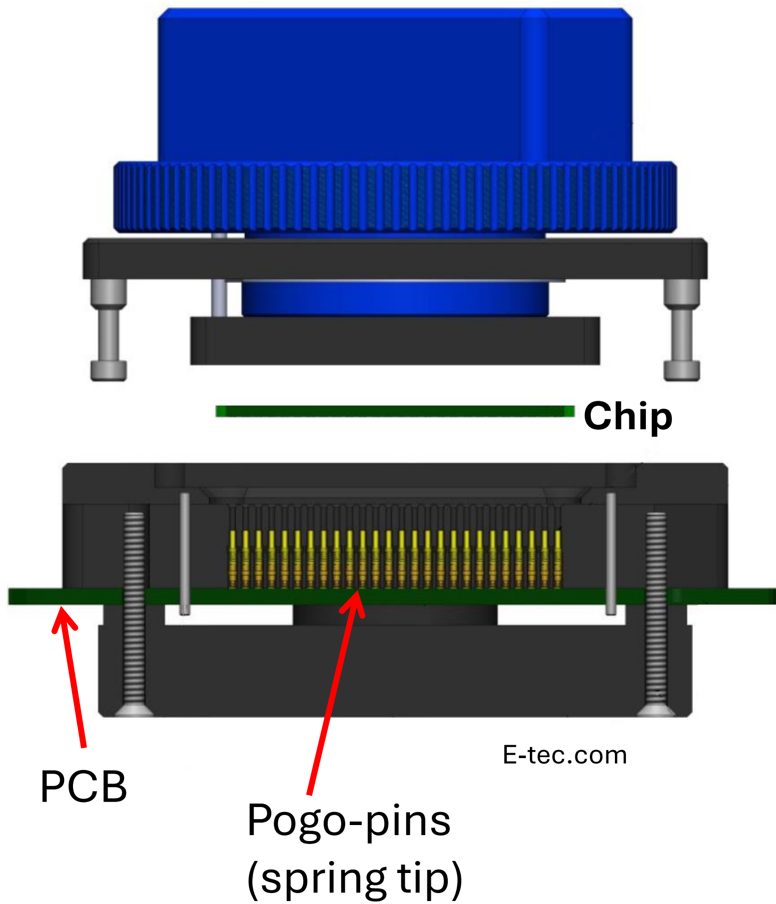
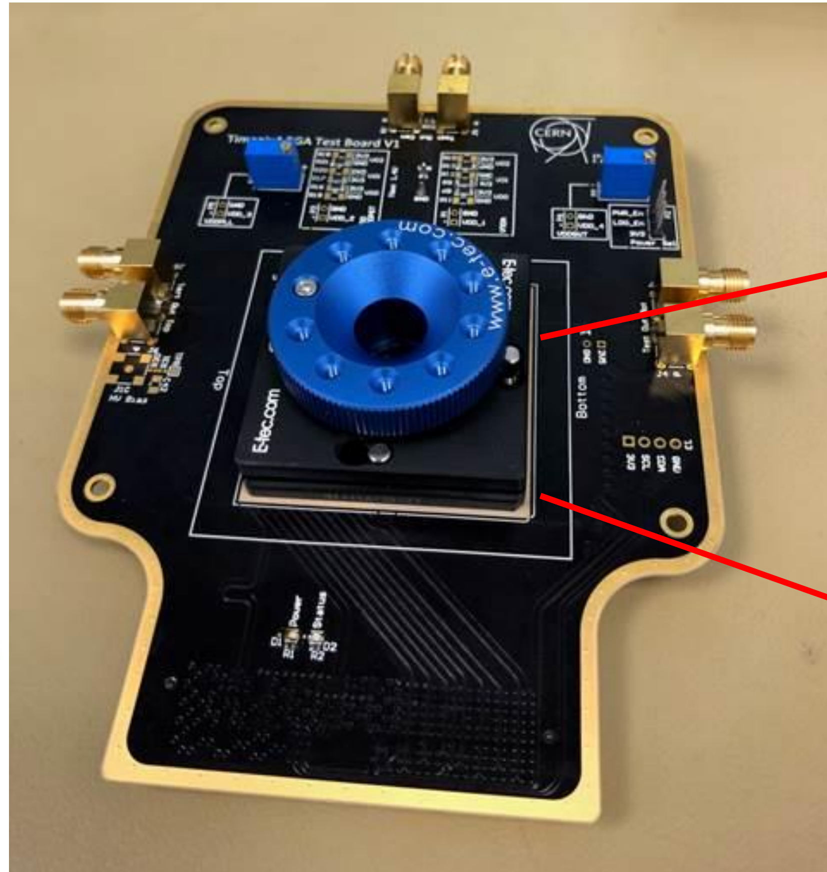
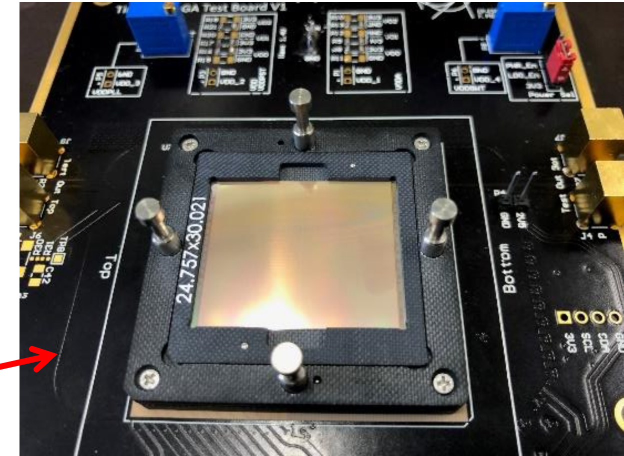
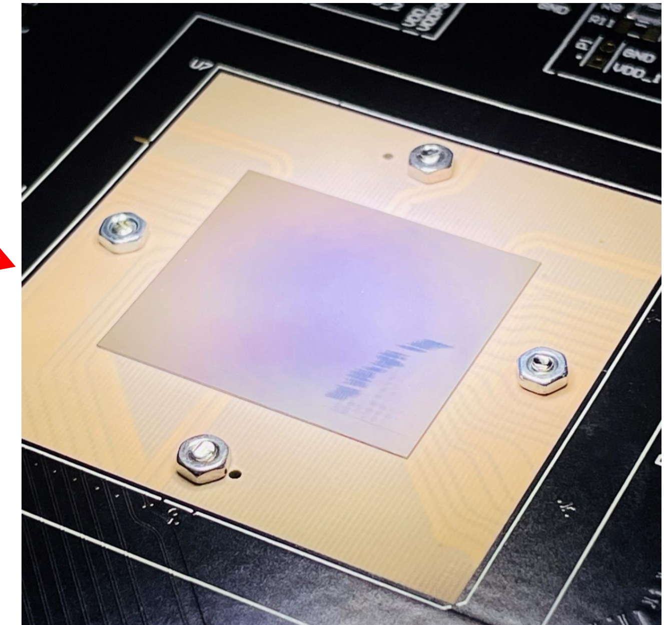




Pogo-pin based socket PCB that allows testing TSV-processed chips

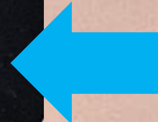


Chip in socket



Direct bonding compatible, with Anisotropic Conductive Paste (ACP) or BGA

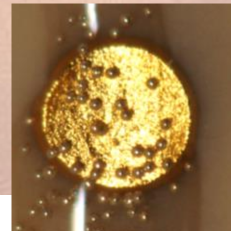
4. Module Design to Test TSV



Front side pixel matrix with bumps

Glue under the chip

Chip bonded with ACP (glue + conducting particles)



PCB pad

4. Module Design to Test TSV

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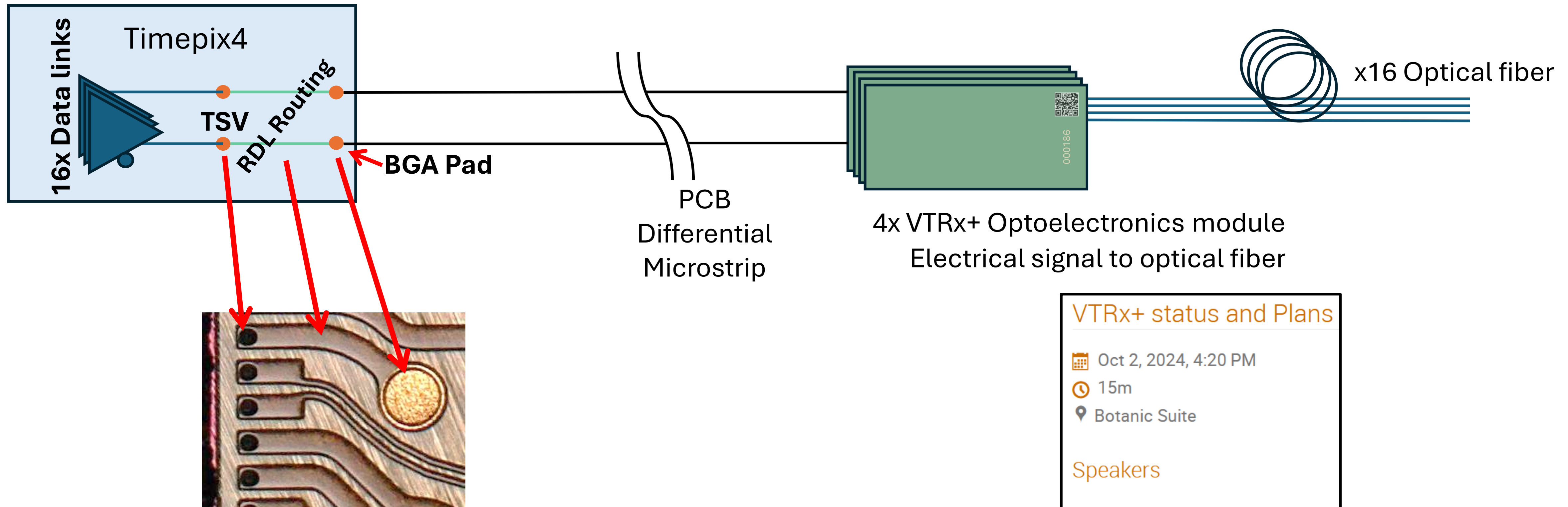
4. Module Design to Test TSV

The Idea:
Proof of principle for particle detector modules



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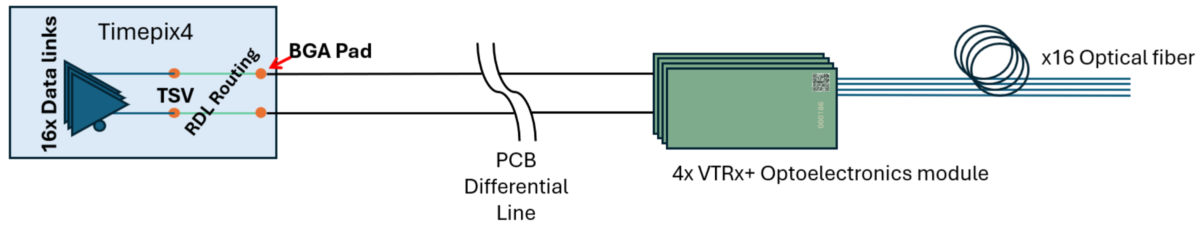
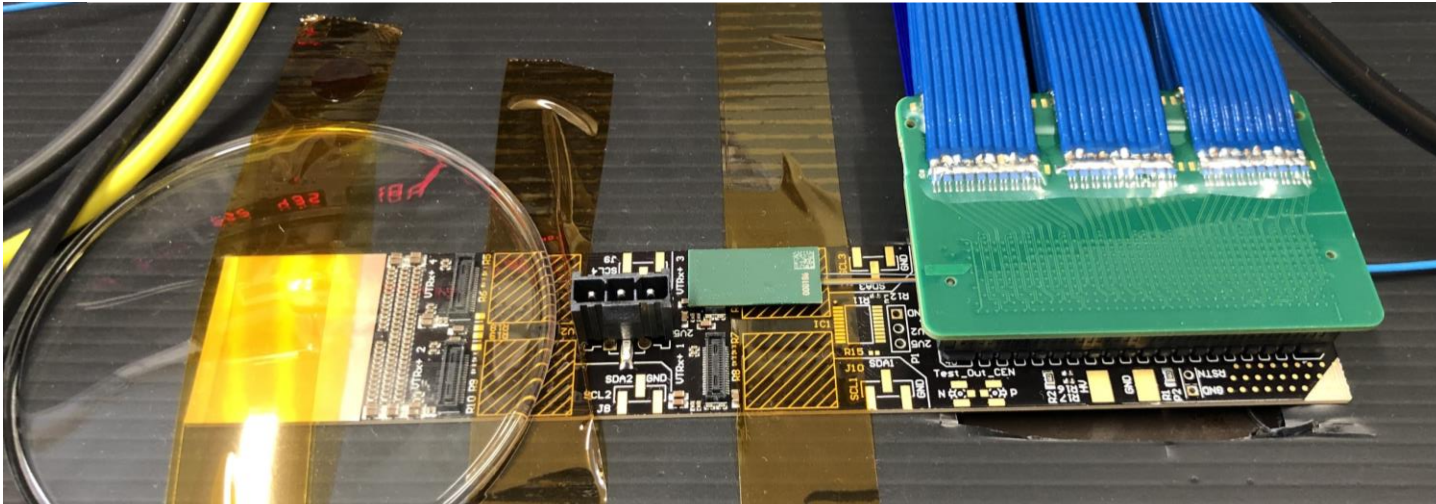
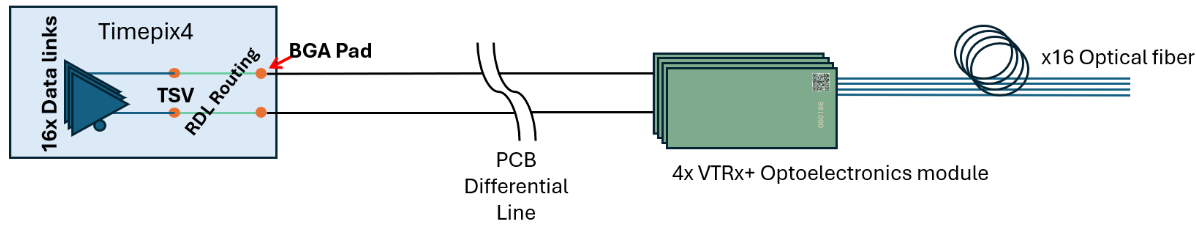
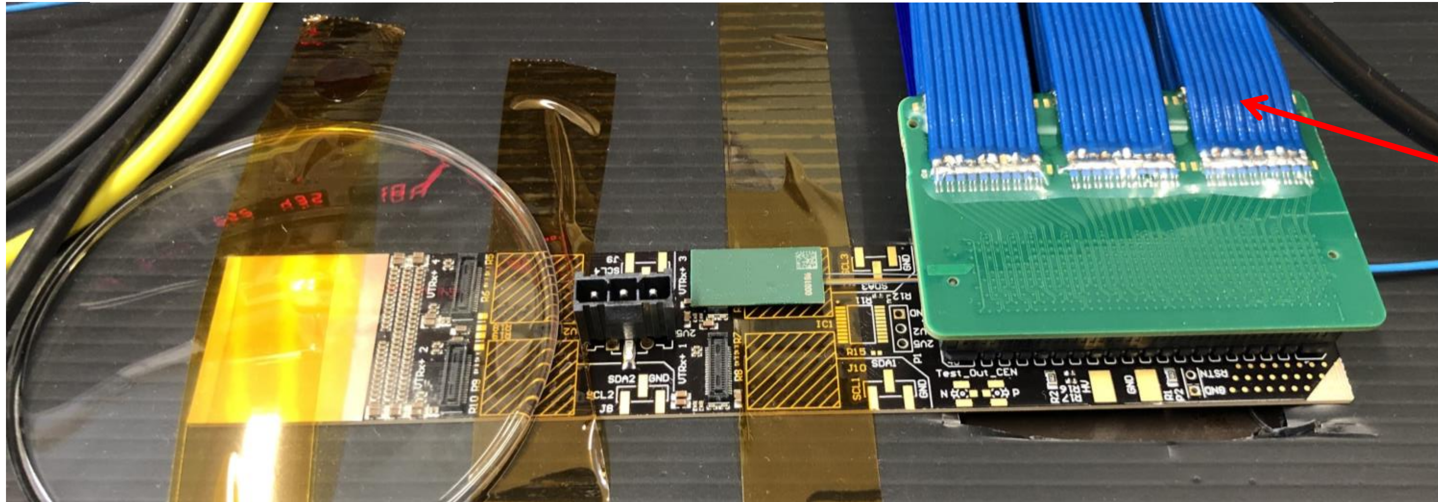




Carrier board 2-Side Buttable
Demonstrator PCB of Timepix4 and VTRx+

4. Module Design to Test TSV

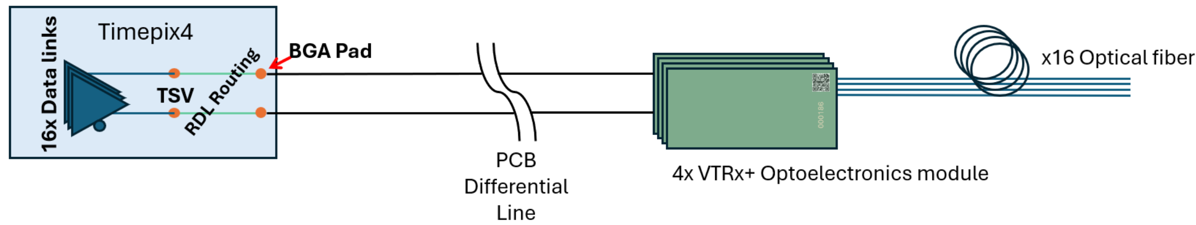


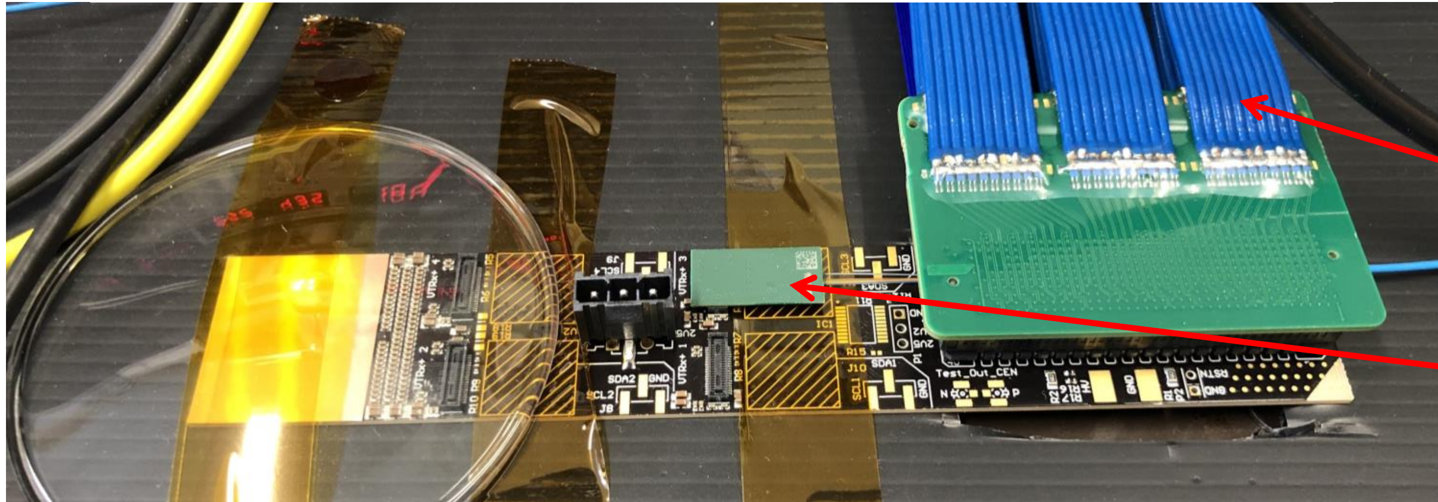


Carrier board 2-Side Buttable Demonstrator PCB of Timepix4 and VTRx+

FMC with slow control and clocks

4. Module Design to Test TSV





Carrier board 2-Side Buttable

Demonstrator PCB of Timepix4 and VTRx+

FMC with slow control and clocks

VTRx+ Quad-Channel Optoelectronics module

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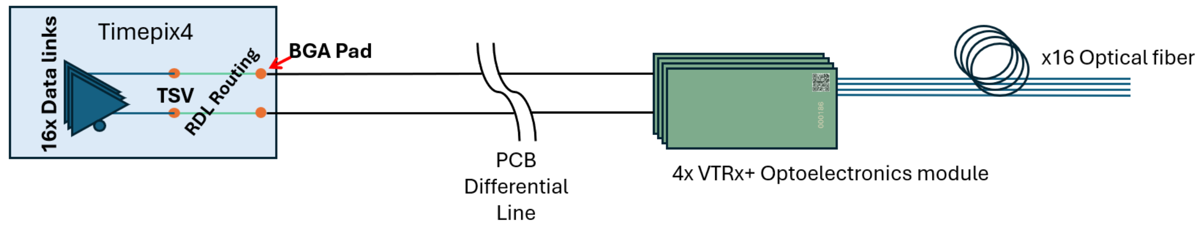
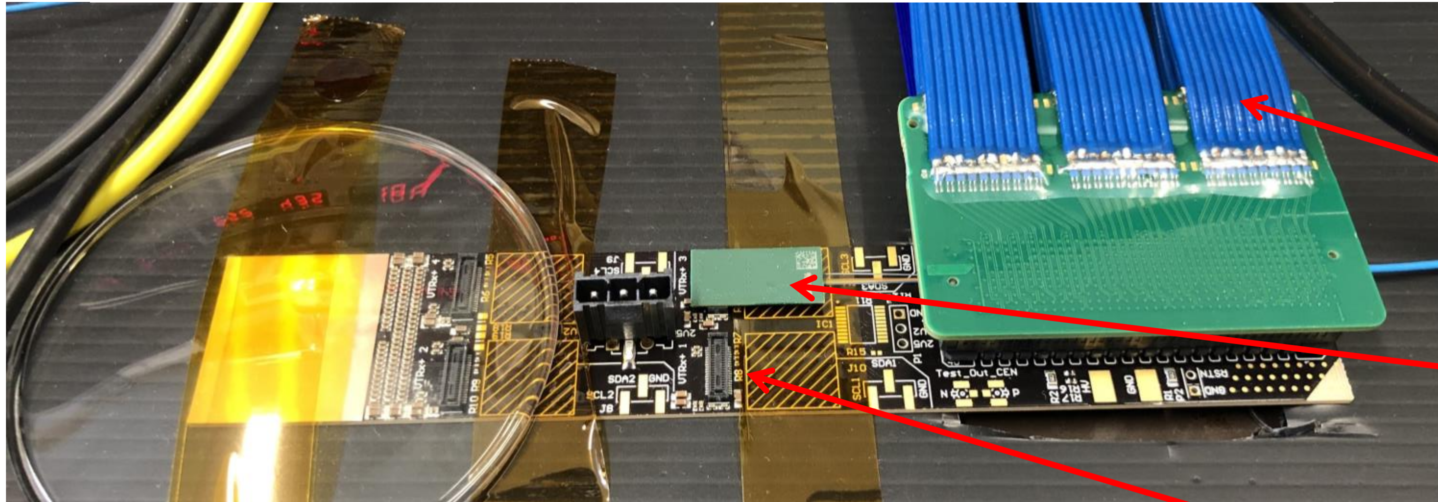




Carrier board 2-Side Buttable

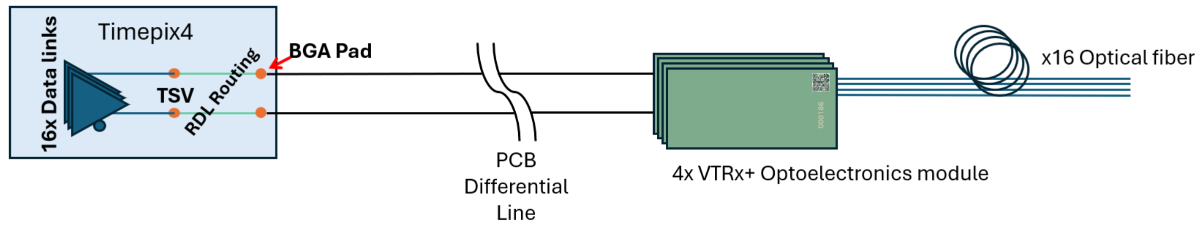
Demonstrator PCB of Timepix4 and VTRx+

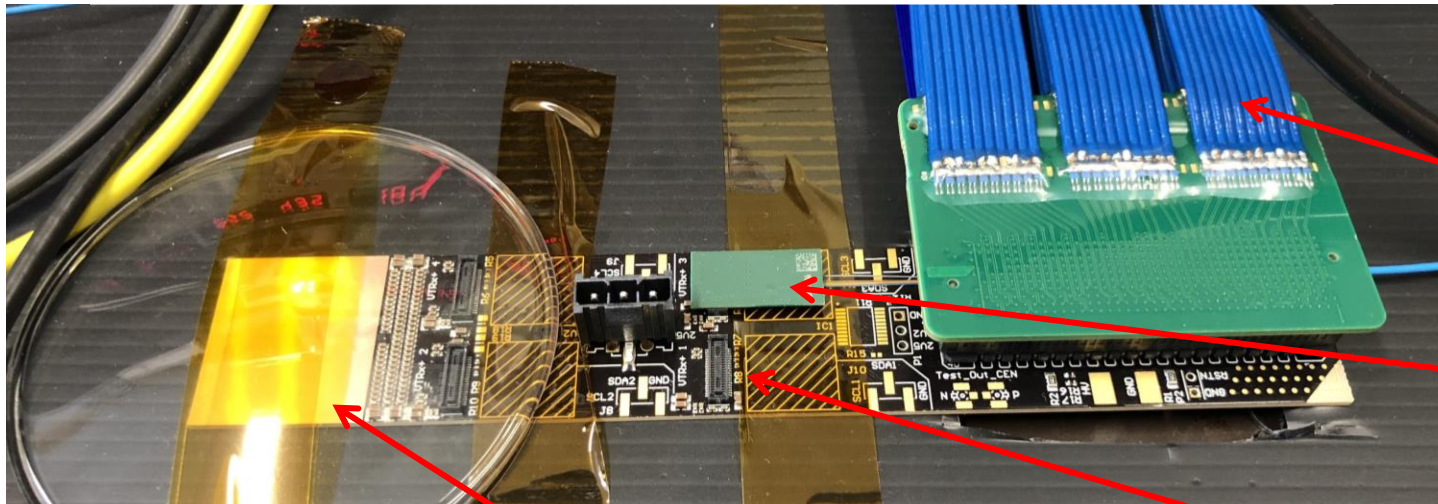
FMC with slow control and clocks

VTRx+ Quad-Channel Optoelectronics module

VTRx+ Connector (4 available for 16 channels)

4. Module Design to Test TSV





Carrier board 2-Side Buttable

Demonstrator PCB of Timepix4 and VTRx+

FMC with slow control and clocks

VTRx+ Quad-Channel Optoelectronics module

VTRx+ Connector (4 available for 16 channels)

Timepix4 V1 TSV, bonded with ACP glue

4. Module Design to Test TSV

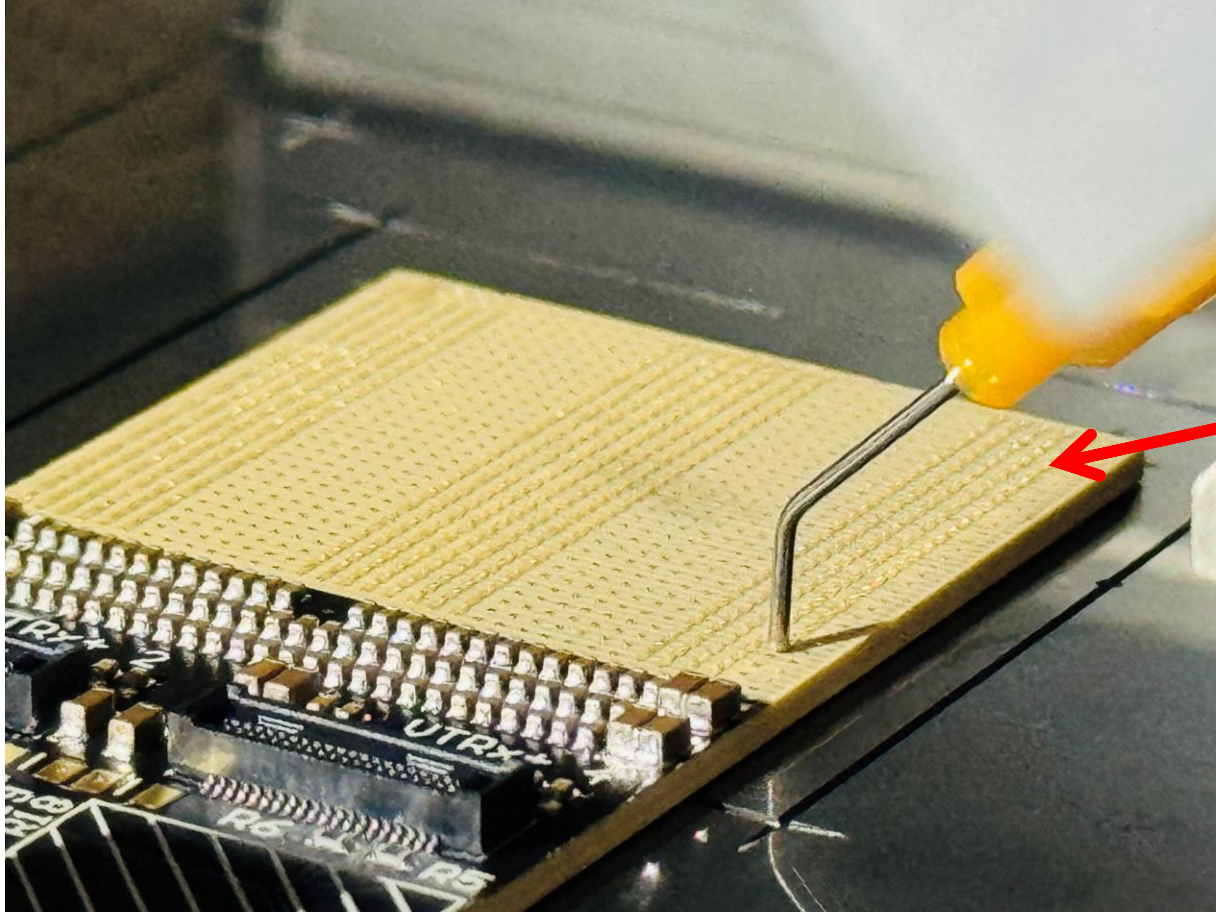
Pixel detector hybridization with anisotropic conductive adhesives

Oct 1, 2024, 4:40 PM
1h 20m

Poster | Packaging and Inter...

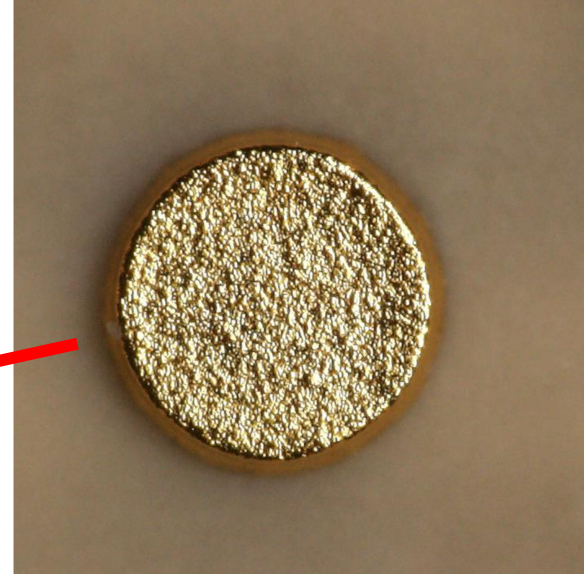
Speaker

Dr Ahmet Lale

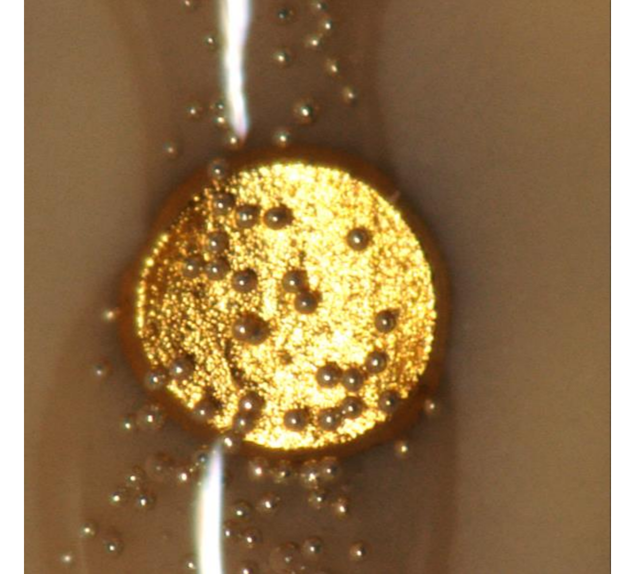


Assembly done at UniGe (University of Geneva)

PCB BGA pad before glue



After glue (30um particles)



Thermo-compression

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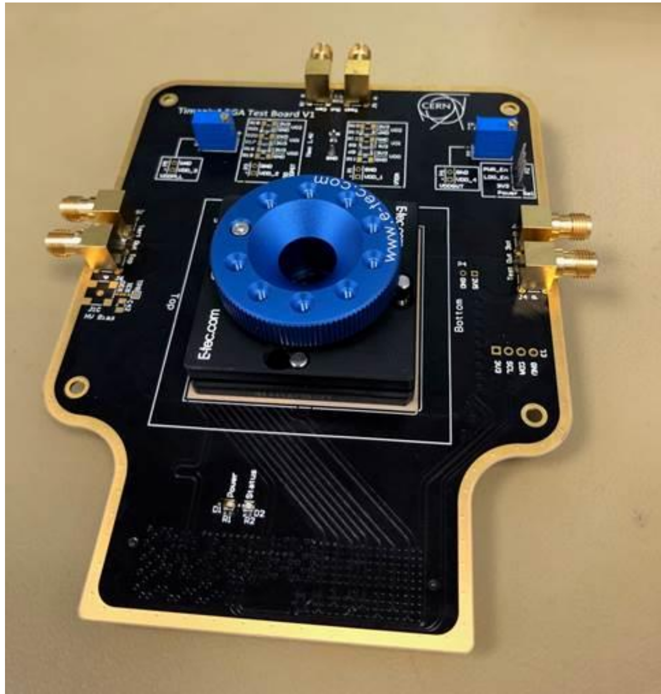
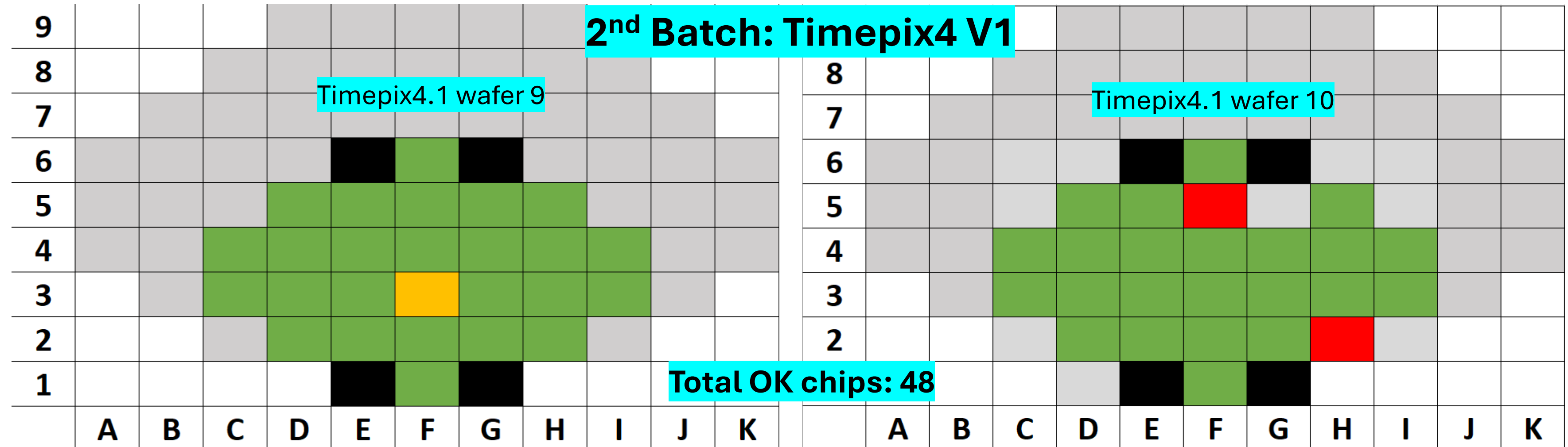


The socket PCB was used to electrically validate chips (power, slow control, etc)

Results:

- 1st batch (2 wafers): Timepix4 **V0**, low yield *
- 2nd batch (2 wafers): Timepix4 **V1**, **<u>excellent yield of 94%</u>**
- 3rd batch (3 wafers): Timepix4 **V3,** expected soon

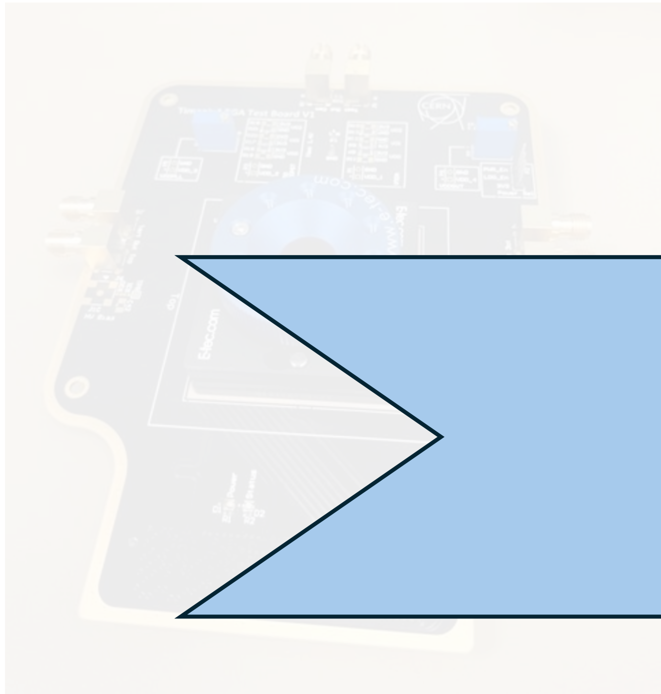
*Processing this batch took very long, due to COVID times

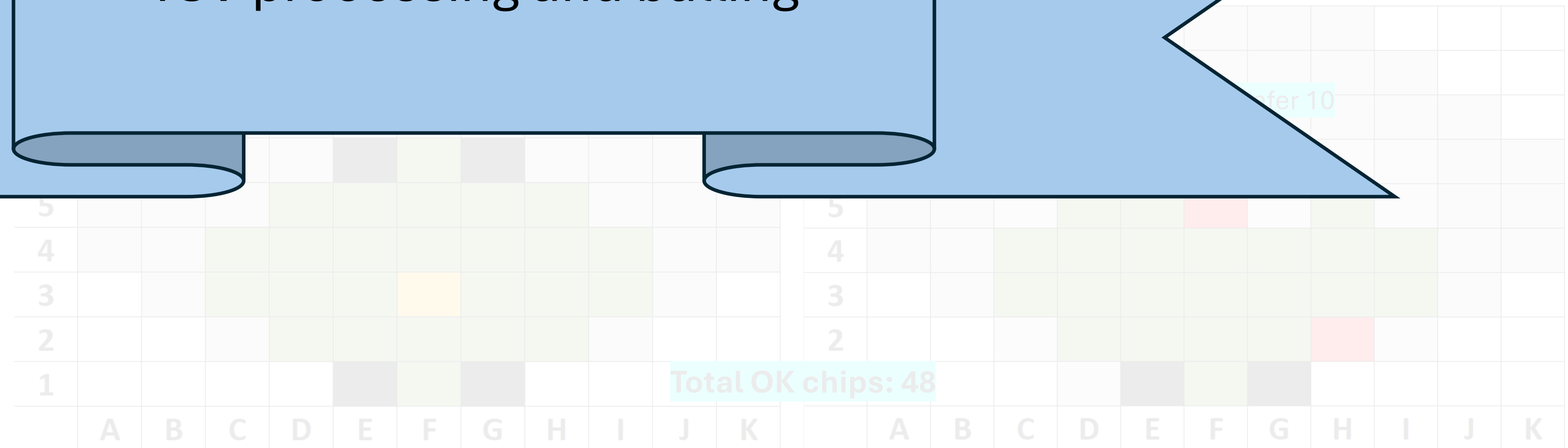


Red: faulty chip
Yellow: partially faulty chip, not TSV related

Black: chip with incomplete edge due to coring margin
Grey: missing chip (coring or inspection)

5. First Results and Future Work





Socket PCB used to test TSV-processed chips

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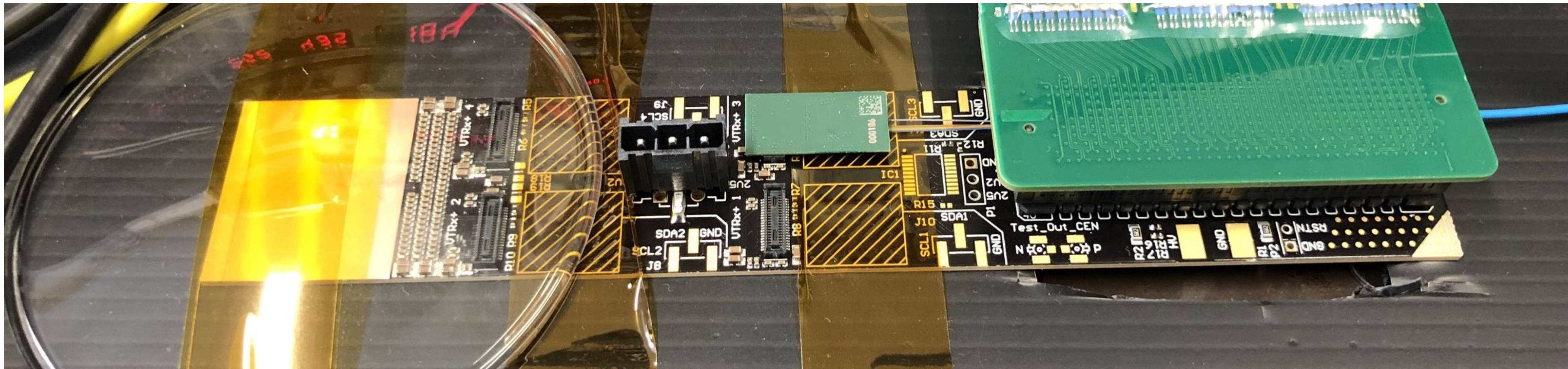
Chips successfully work after TSV processing and balling

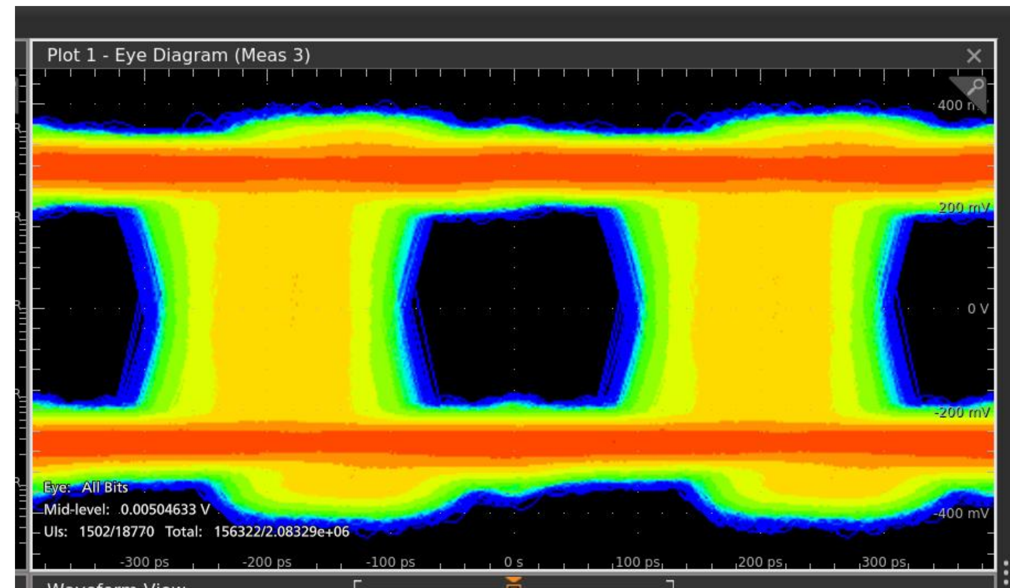
5. First Results and Future Work



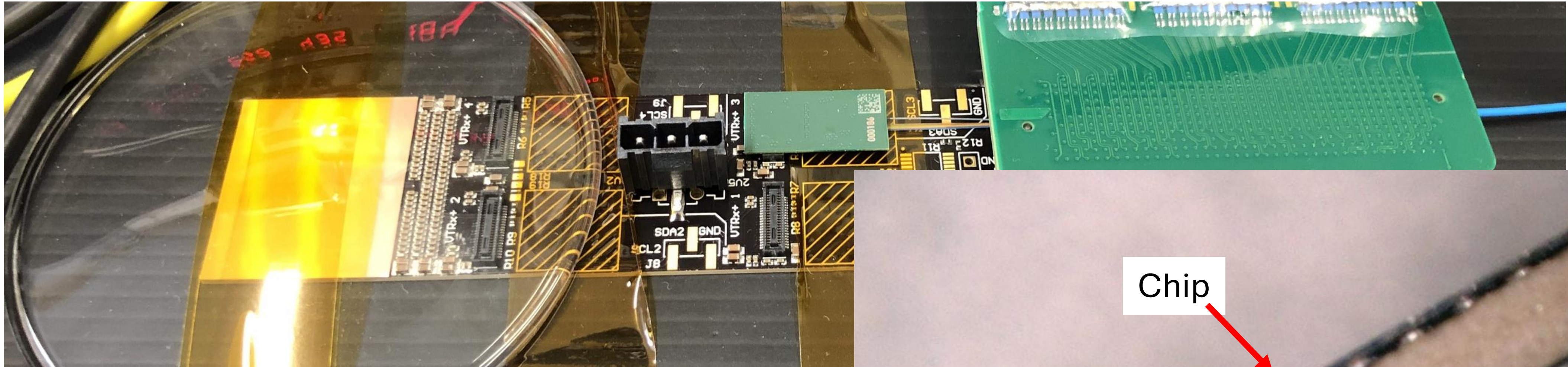
Opto-demonstrator module

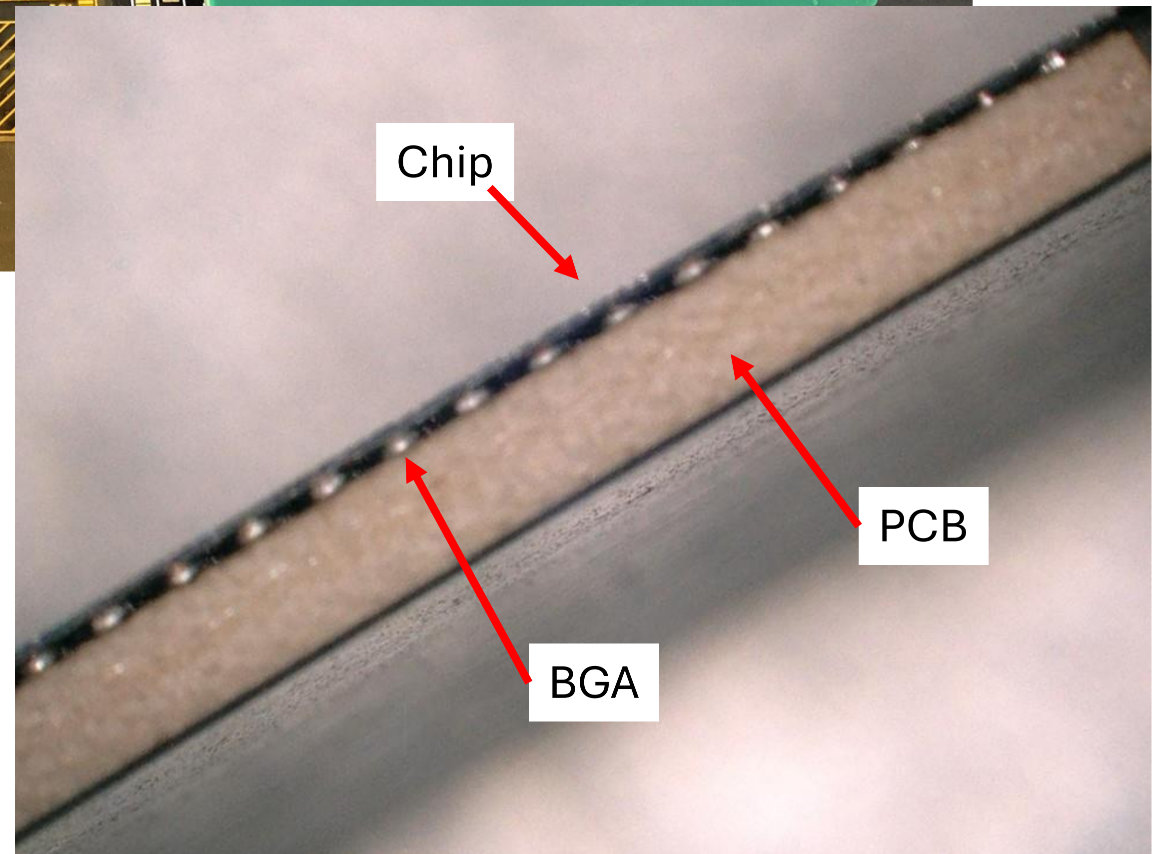
Timepix4.1 TSV, bonded with ACP glue

- Eye diagram through **optical fiber** at 2.56Gbps.
- This version of the chip has **problems with jitter**.
- Waiting for TSV processing of Timepix4 V3

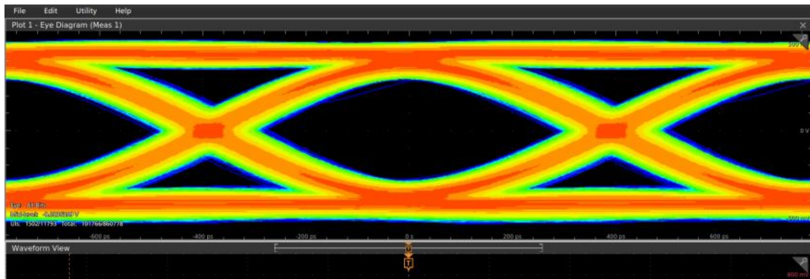


5. First Results and Future Work





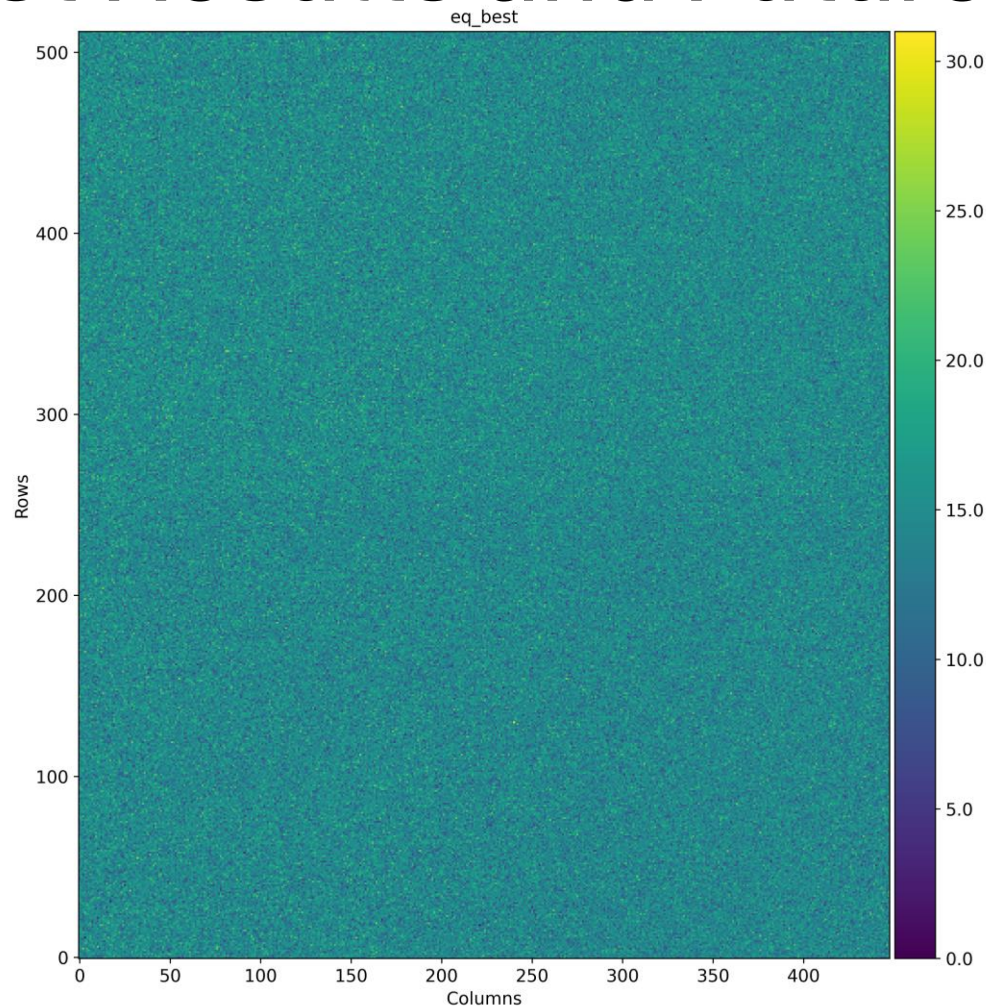
Same PCB but Timepix4.1 TSV soldered with BGA balls (for the first time) instead of ACP glue
SAC305 alloy, 300um solder balls

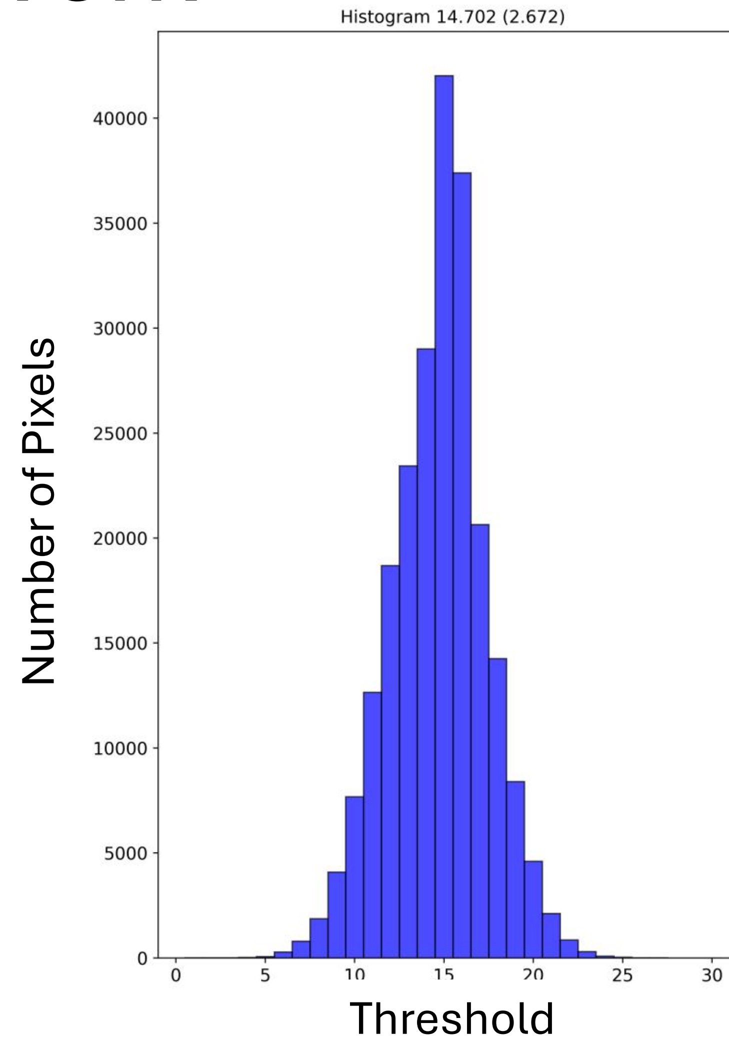


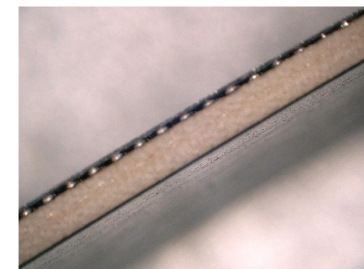
Eye @1.25Gbps
Through optical fiber

Assembly done at CERN

5. First Results and Future Work





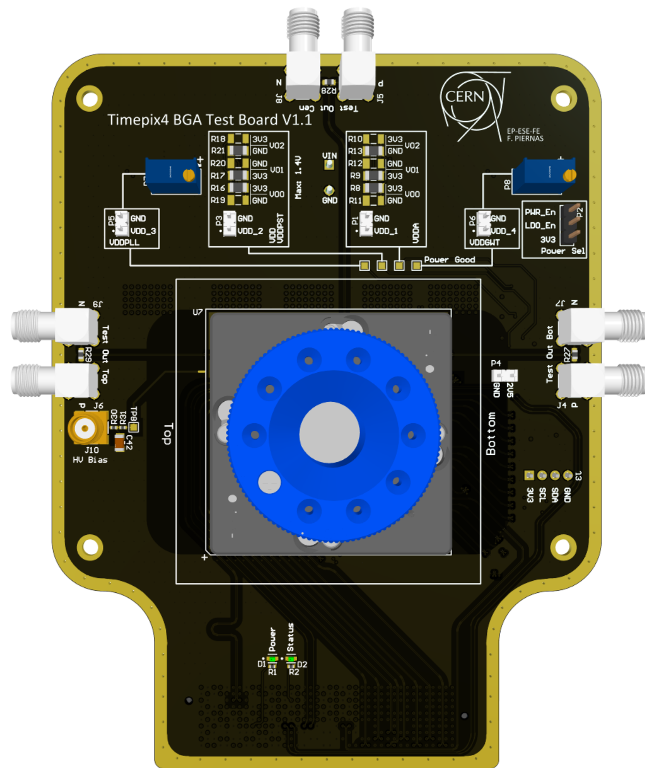


Threshold equalization with the previous PCB (Timepix4 V1 TSV soldered with BGA)

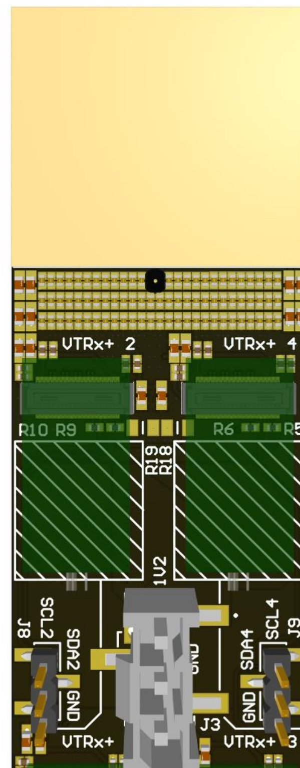
Slow control, global biasing DACs and pixel matrix working, after TSV processing, balling and soldering

5. First Results and Future Work

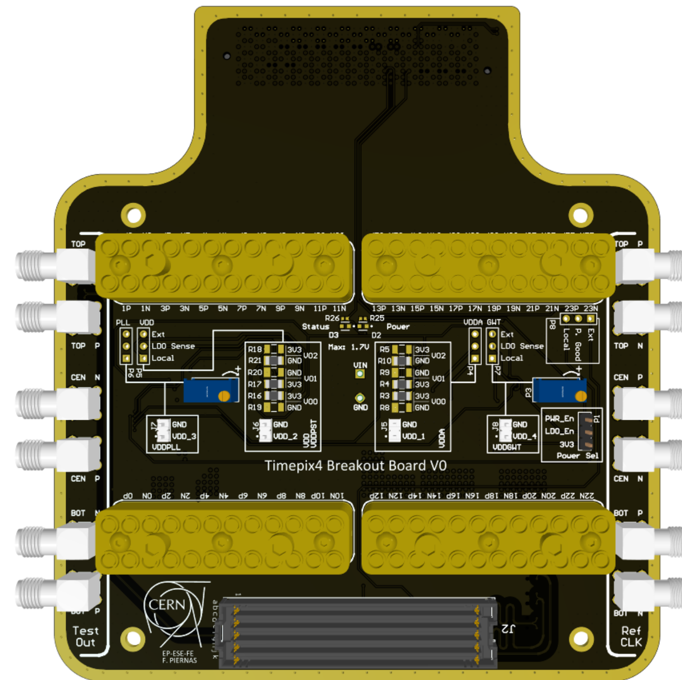
Family of PCBs for testing TSV-processed Timepix4



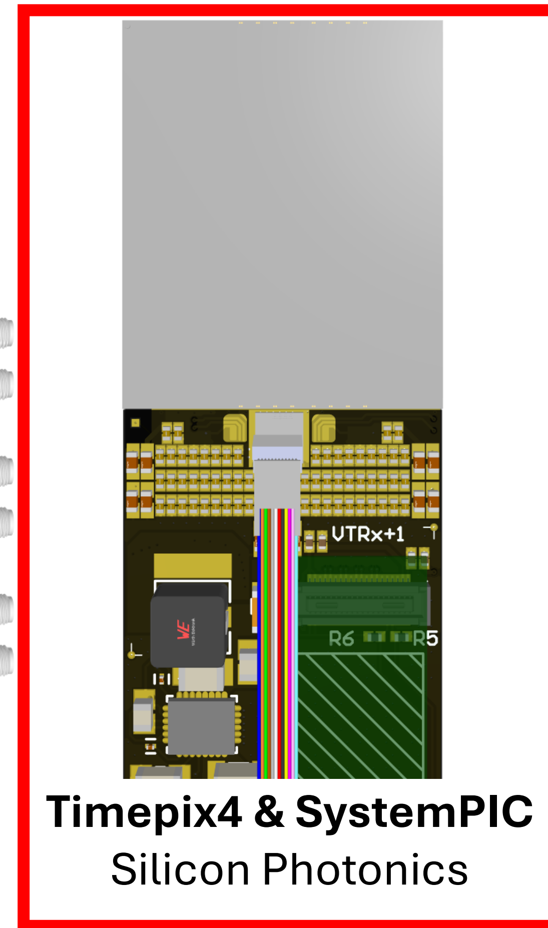
Socket PCB
Electrical Tests



Timepix4 & VTRx+
Optoelectronics Demonstrator



Breakout PCB
Extracting data links and clocks through SMA cables



Timepix4 & SystemPIC
Silicon Photonics

More in progress…

5. First Results and Future Work

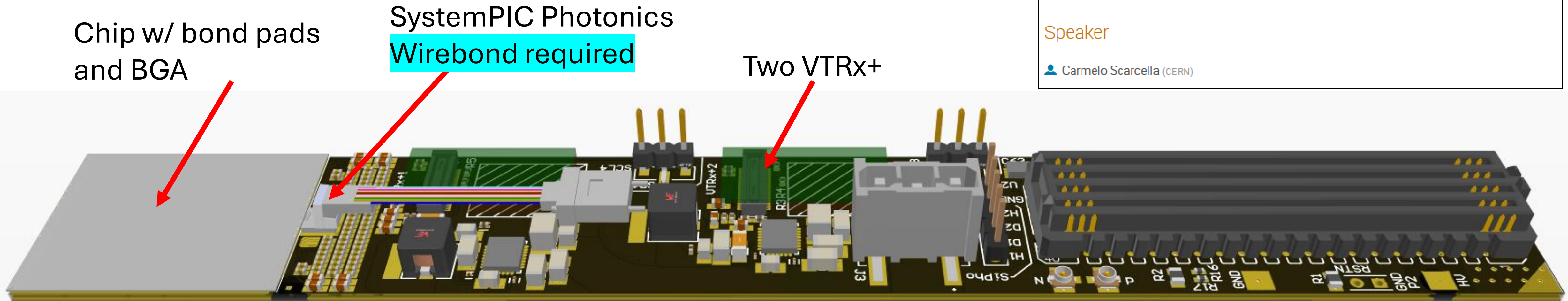
Silicon Photonics Circuits for the optical readout of CERN detectors

Oct 3, 2024, 2:20 PM
20m
Grosvenor Suite Theatre
Oral
Optoelectronics and...

Speaker

Carmelo Scarcella (CERN)

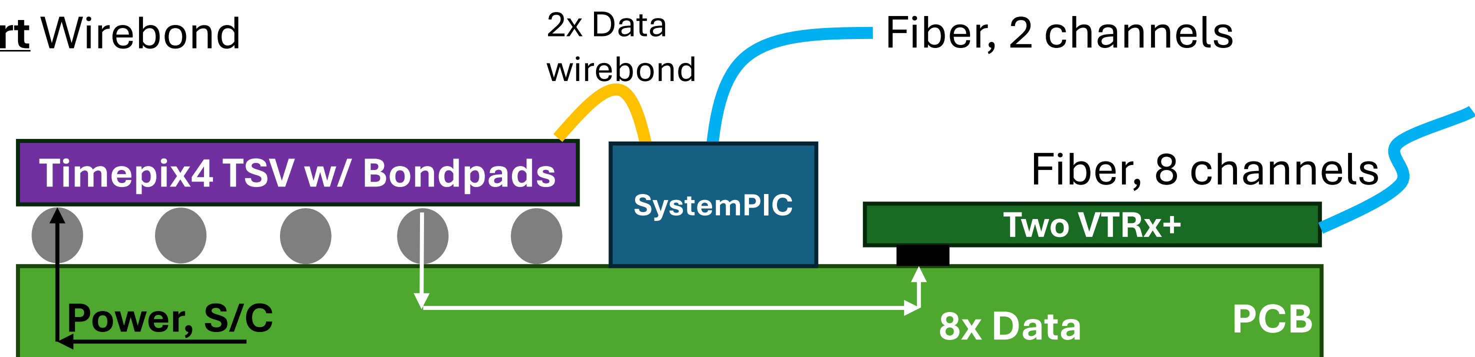
Demonstrator PCB of Timepix4 and SystemPIC 2-Side Buttable



One PCB to test, at the same time:

- Power and S/C through TSV
- Silicon Photonics with data through **short** Wirebond
- Optoelectronics with data through TSV

In production



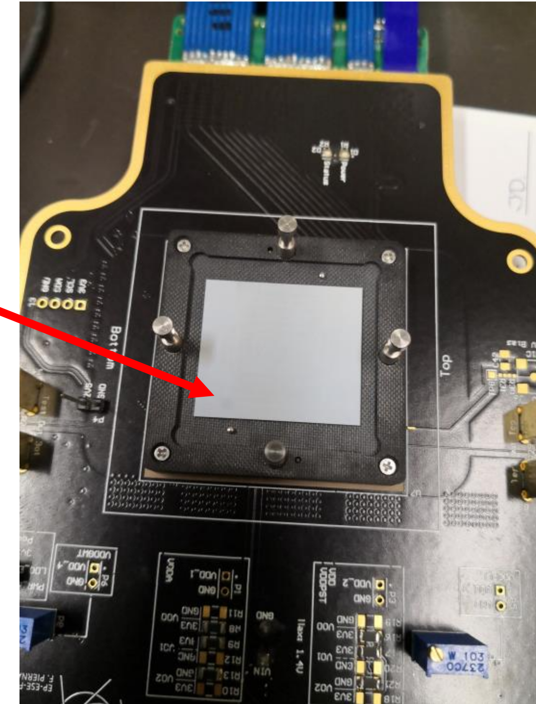
How will this assembly perform?

Last-minute Surprise!

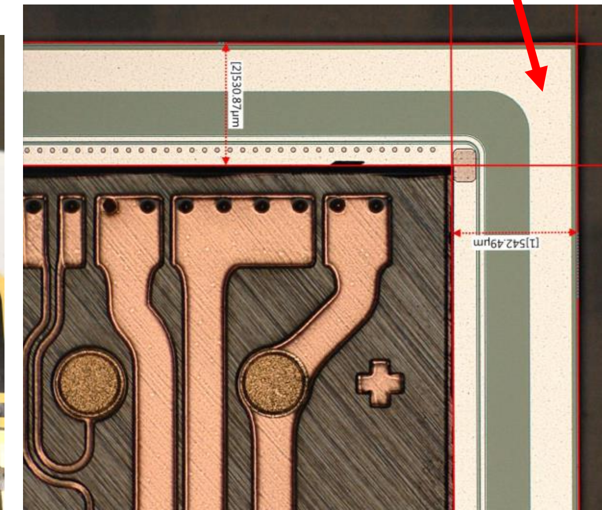
First Timepix4.1 TSV with Silicon Sensor

Chip back side

Sensor



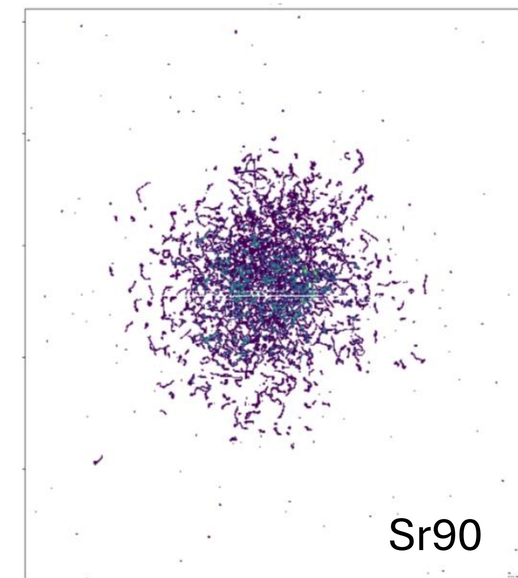
Sensor



Testing by J. Alozy

Sensor bonding at Advafab

First result with radioactive source!



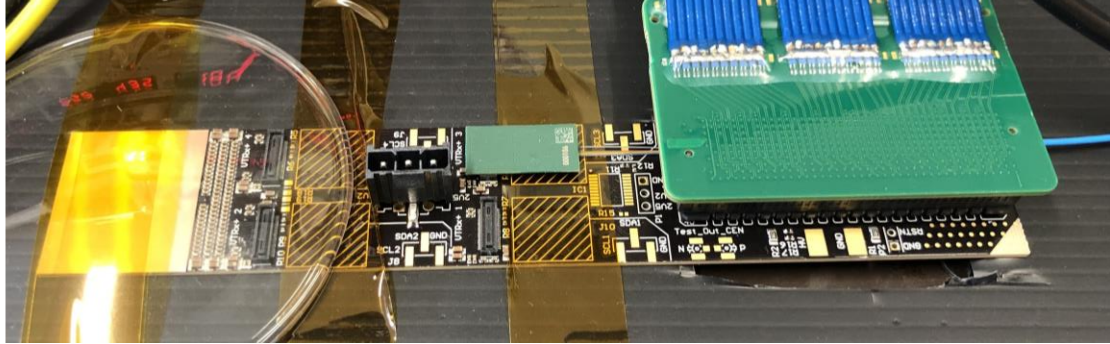
Conclusions and outlook

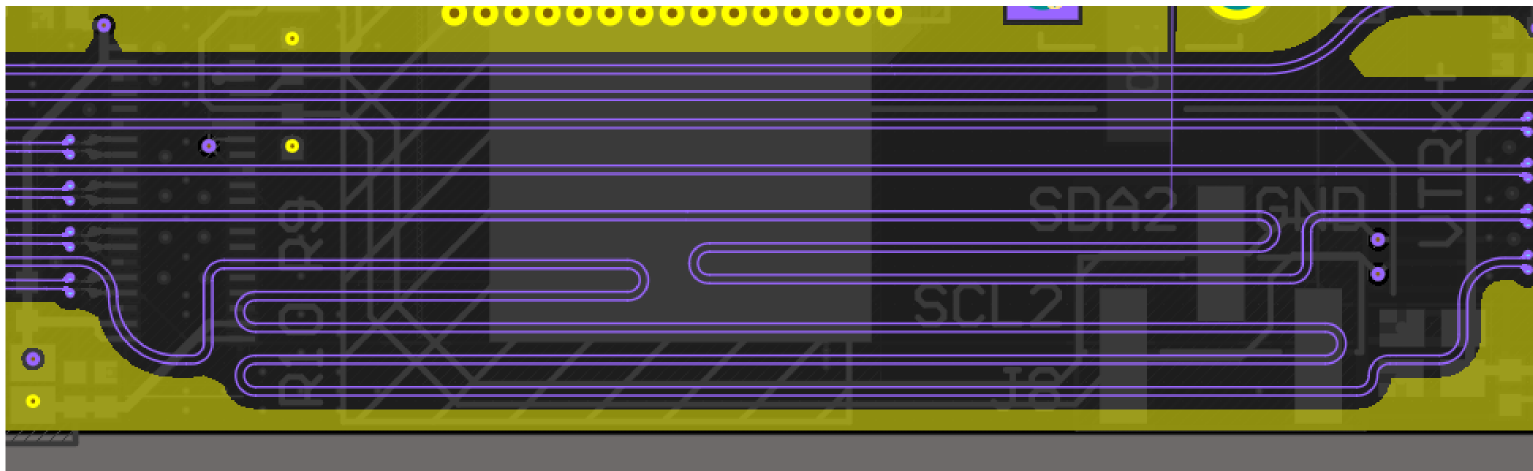
- TSV are a **suitable alternative** to wirebond.
- TSV successfully fabricated on Timepix4 chips.
- Tests show that **chips work** when connected to test modules.
- TSV processing is **tricky**, done at wafer level and some wafers are **used** for tuning of the process.
- Demonstrator **modules** for extracting data through optical fiber.
- Waiting for Timepix4 V3 with TSV for **5Gbps** readout.
- Exploring other vendors for TSV processing (Europe and worldwide).

Thank you for your attention

Extra Slides

PCB Design considerations

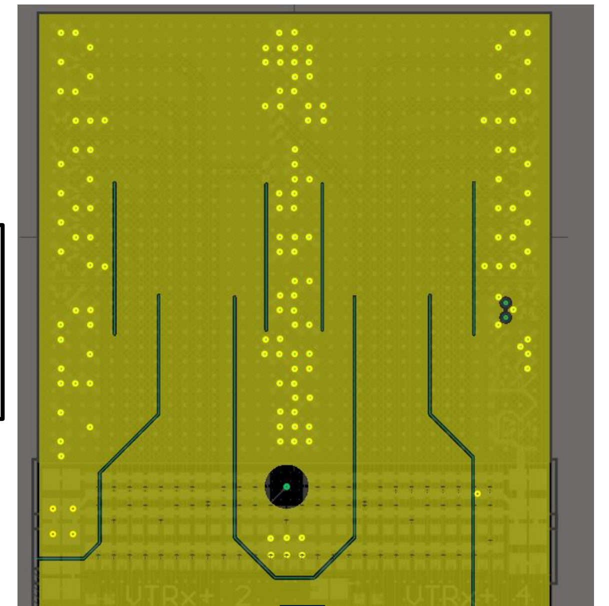


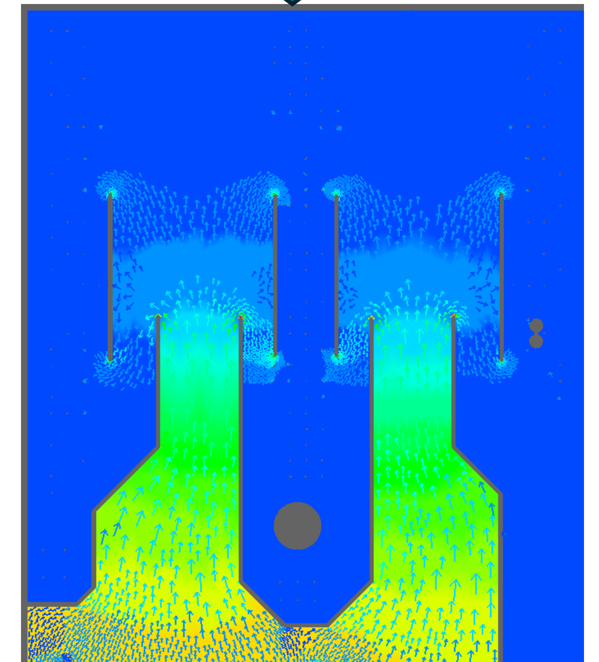


Extension of data lines up to 15cm to test signal integrity (how far the VTRx+ can be placed).

- Too close to the readout ASIC: high radiation
- Too far: signal degradation

Copper cutouts to distribute current and voltage drop





Conductivity test of TSV

- Wafer with defective TSV.
- Feedback by IZM: Bad processing of this wafer.

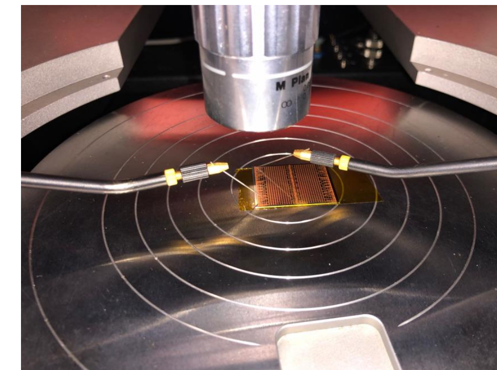
Row of TSVs

<1	<1	<1	<1	1	<1	<1	1	W3H2 (Ω)
97	9	256	75	9	36	66	19	W4D2 (Ω)
56	138	5	53	36	32	79	29	W4G2 (Ω)

Chip nº

Conduction test between pads of the same internal power plane, using micromanipulator probes.

Some faulty chips have higher resistance in BGA than in wirebond pads: TSV conduction issue.

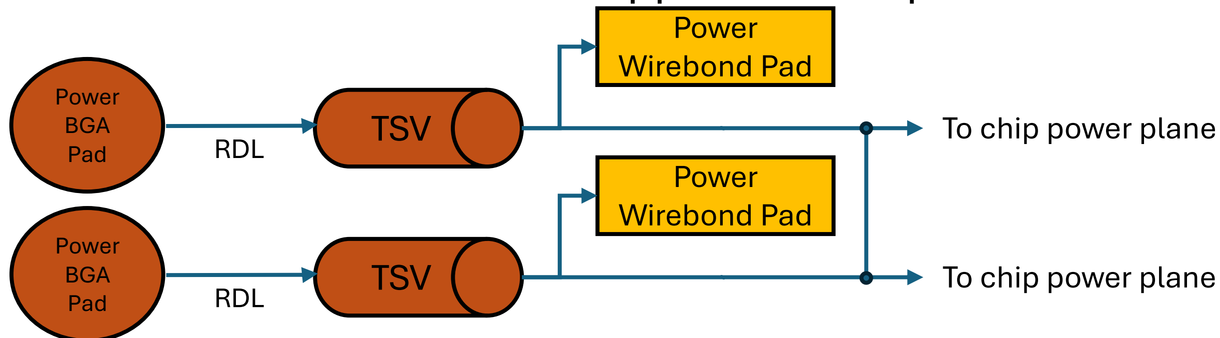


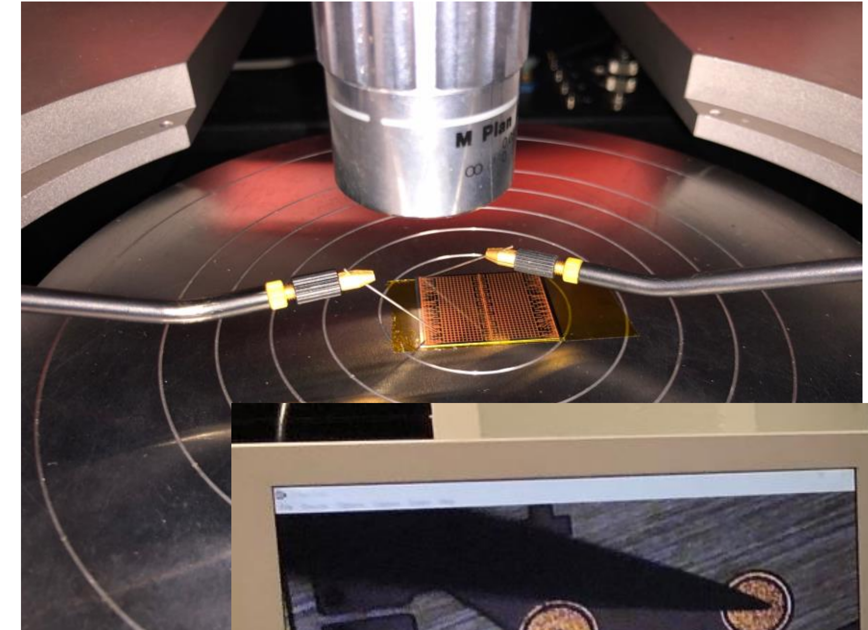
Bondpad Resistance vs BGA Resistance

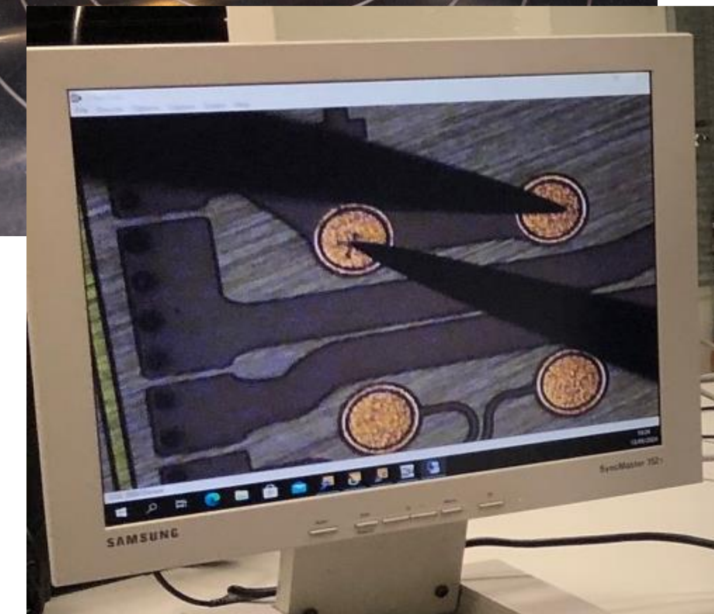
Wafer 4 (faulty TSV) Resistance on VDDA											
F1		D2		E2		F2		G2		H2	
Bond Pads	BGA	Bond Pads	BGA	Bond Pads	BGA	Bond Pads	BGA	Bond Pads	BGA	Bond Pads	BGA
2	2	2	19	1.8	19	1.3	51	1.9	29	1.5	52
2	7	1.9	66	2.9	70	1.3	47	1.4	79	1.4	2
1.7	24	2	36	2.9	66	1.4	1	1.8	32	1.6	35
2	19	1.3	9	1.3	20	1.4	60	1.5	49	1.6	95
2	29	1.9	75	1.4	83	1.4	3	1.5	53	1.3	20
2	9	2.2	256	1.3	54	1.7	1	1.5	5	1.5	19
2	16	2	9	1.4	16	2.2	15	1.5	136	1.4	30
2	48	2	97	1.4	239	1.7	53	1.3	55	1.5	2

Measurements done by S. Al-Tawil

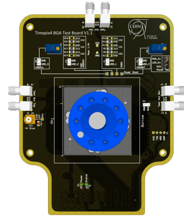
Observations: resistance on bond pads is overall lower than BGA on this wafer. Measurement sensitive to force applied on the pads.



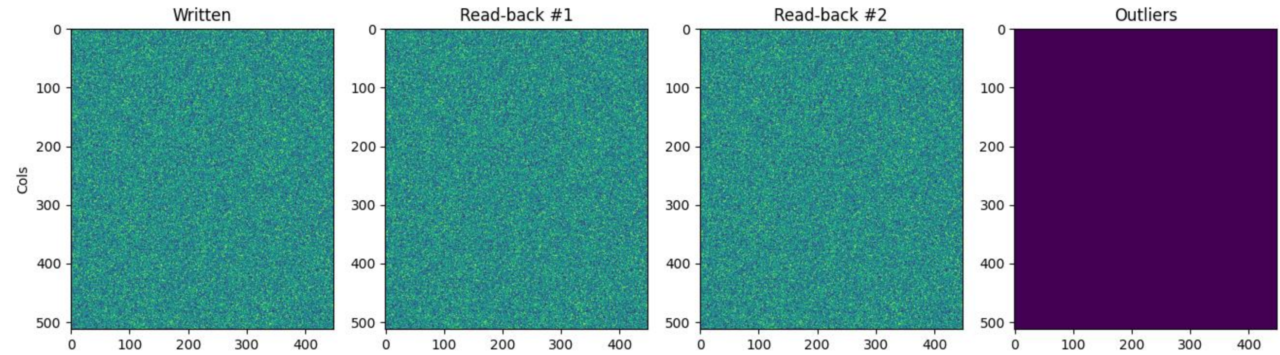




Soldering and Testing a Timepix4 V1

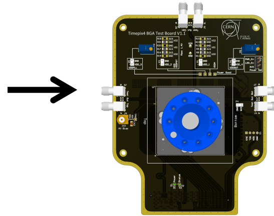


- TSV processed only

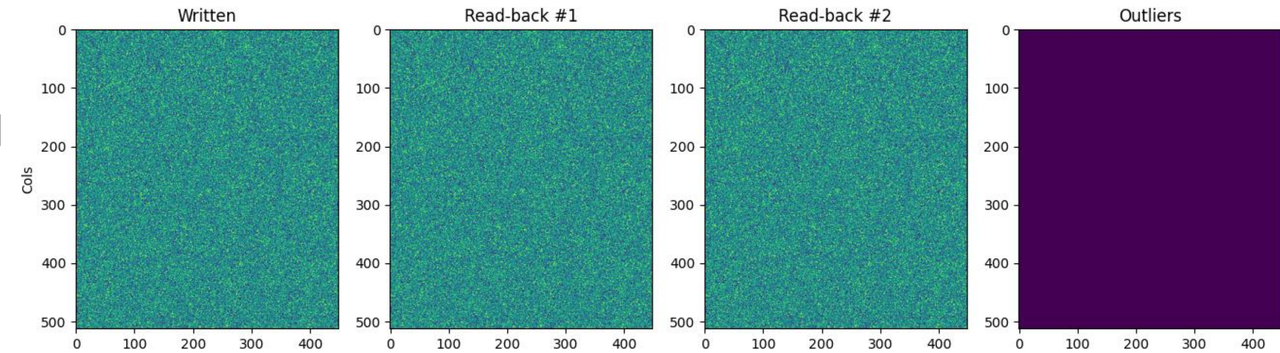


Bad pixels: 0

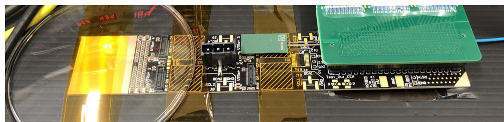
PCB used to test



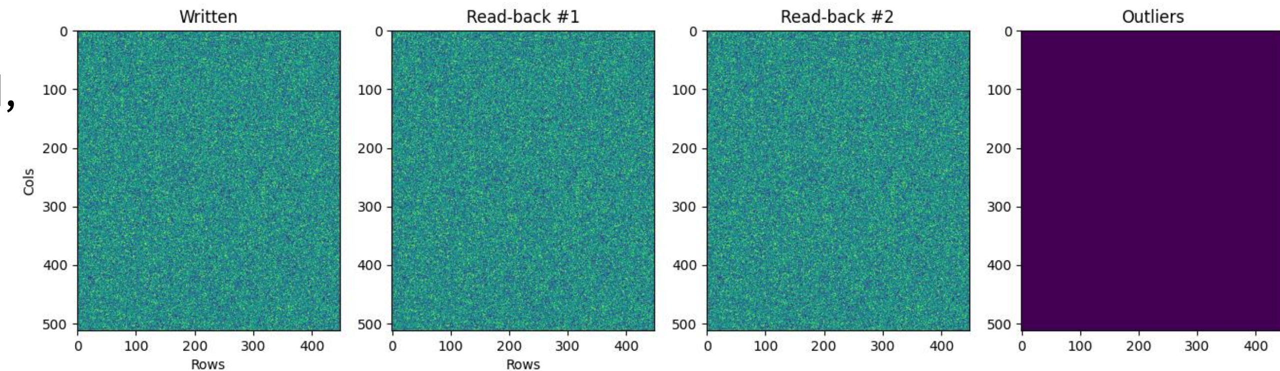
- TSV processed and balled



Bad pixels: 0



- TSV processed, balled and soldered



Bad pixels: 0

Test successful: writing and reading back random data to a register in all pixels.

Chip W10I3

Deep Reactive Ion Etching (DRIE) in Silicon

- Deep Reactive Ion Etching (DRIE)
  - Bosch Process
  - Switched Process

a) Resist or Hardmask

b) Isotropic Etch (SF6)

c) Deposition (C4F8)

d) Anisotropic Etch (SF6)

e) Isotropic Etch (SF6)

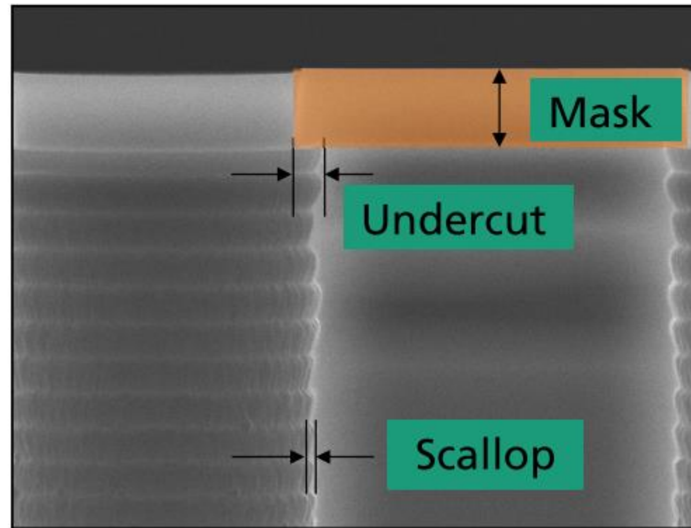


Image: SPTS

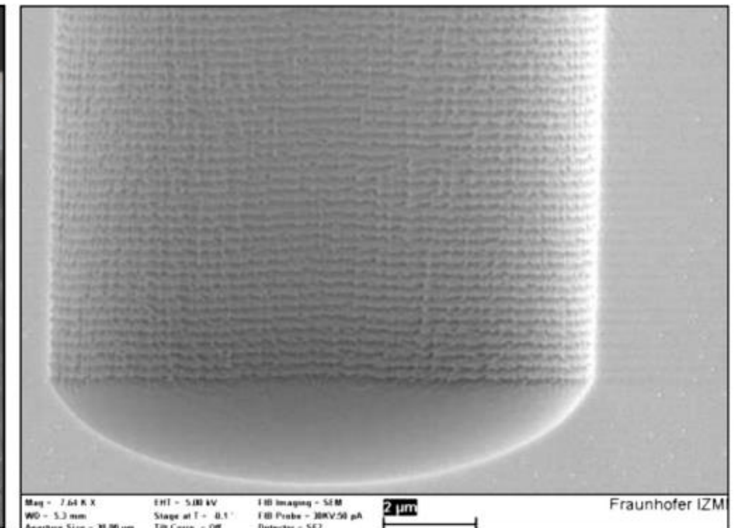
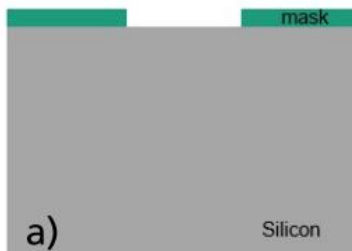
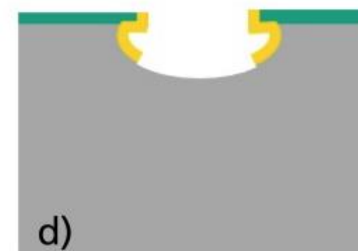
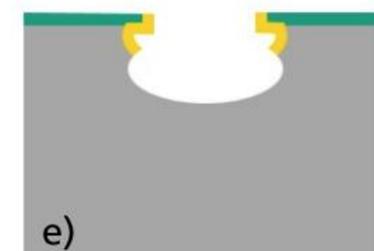


Image: IZM







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CERN EP-ESE Electronics Seminars, April 12th, 2022

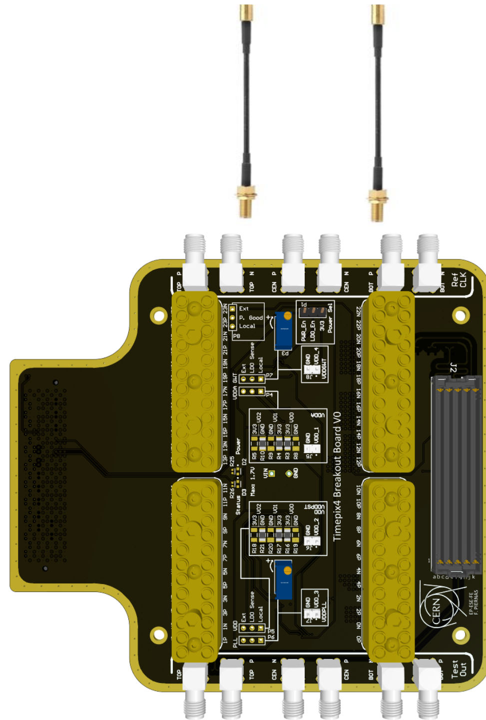
Seminar by T. Fritzsch et al.
IZM Fraunhofer

Breakout PCB

Reference clock generator (optional)

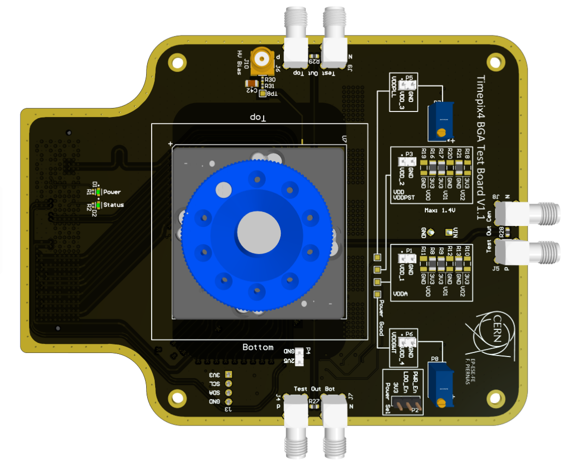
Readout System

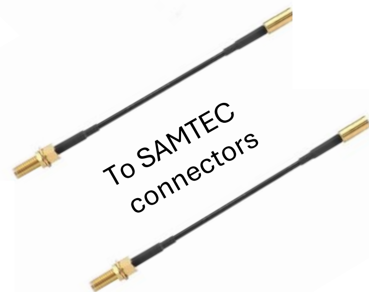
Optional FMC



Optional FMC

Socket board



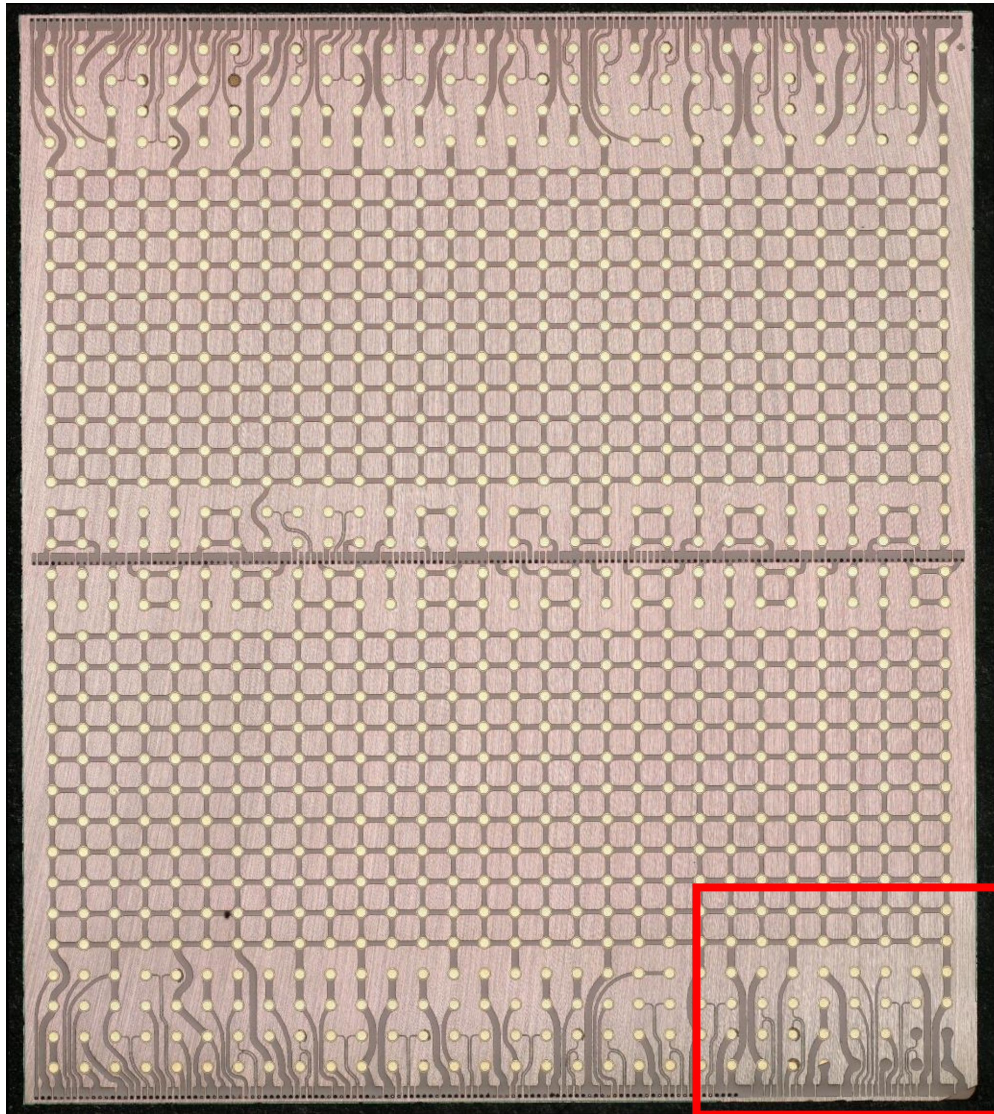


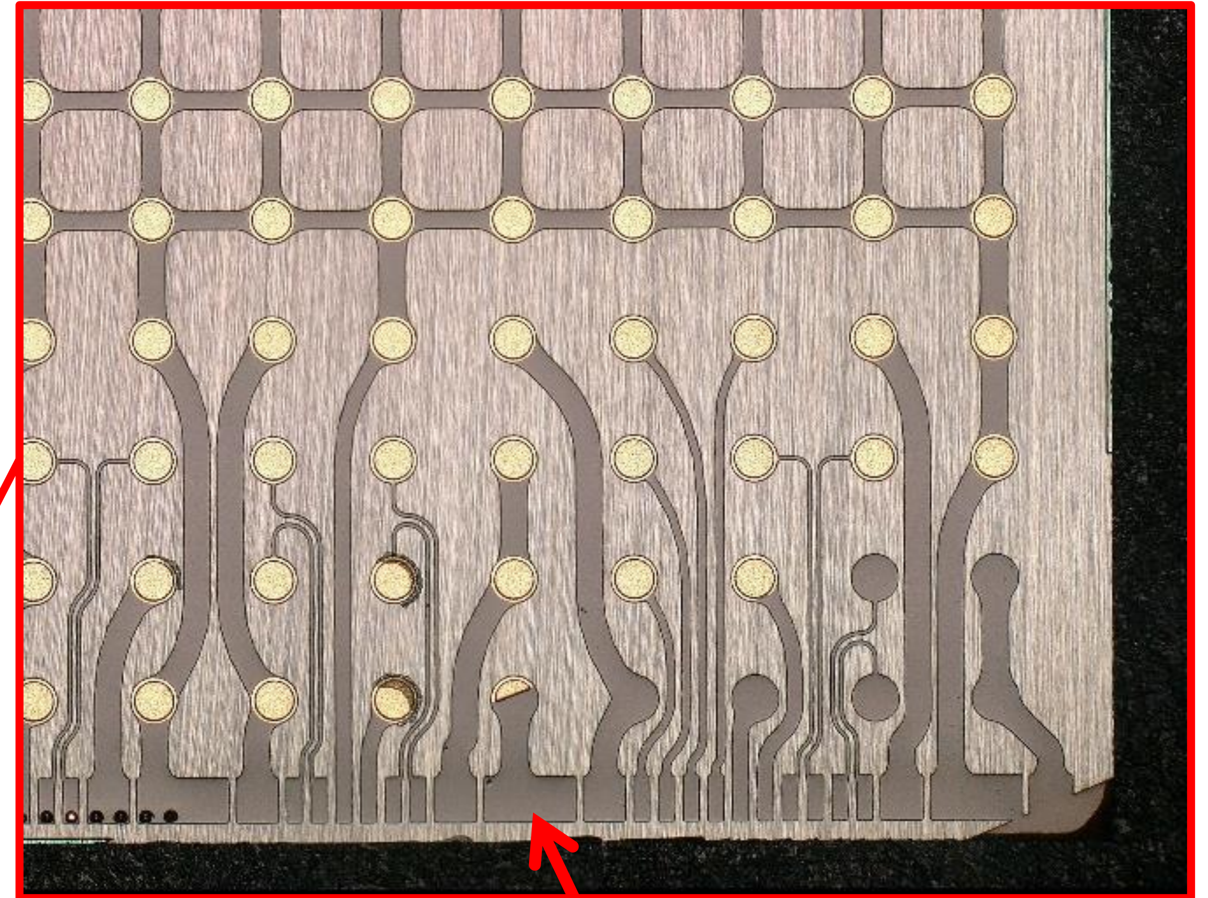
To SAMTEC connectors

Data signal eye

Test out signals measurement (optional)

Chip with incomplete edge





Missing pads and TSV, due to limitations at IZM