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3D Integration of Pixel Readout Chips using Through-Silicon-Vias

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Particle tracking and imaging detectors are becoming increasingly complex, driven by demands for densely integrated functionality and maximal sensitive area. These challenging requirements can be met using 3D interconnect techniques widely used in industry. In this paper, we present the results of an evaluation of the 3D through-silicon-via (TSV) technology, using the Timepix4 integrated circuit as a test-vehicle. We will present the concepts for 3D integration and test results from TSV-processed chips bonded to custom-designed circuit boards conceived as proofs-of-principle for future detector modules.

Summary (500 words)

The evolving demands on solid-state particle-tracking and imaging detectors incorporating pixelated readout integrated circuits (ICs) require new approaches for power and signal connections. Future systems will provide complex functionality such as timing the hits of particles to the order of tens of picoseconds, as well as precise position and energy measurements. The corresponding needs to deliver clean power to the IC circuitry and support high data bandwidths are challenging with traditional interconnect technologies such as wire-bonding. Additionally, space reserved for the interconnects often limits the sensitive area. These concerns have motivated our study into alternative interconnect technologies.

Through-Silicon-Vias, (TSVs), are vias fabricated in an IC by performing deep reactive ion etching (DRIE). After side wall passivation and metal filling by an electroplated Cu-layer, TSVs connect the IC circuitry on its active front-side to the back-side. A back-side redistribution layer (RDL) provides the interconnection to an array of I/O pads. This technique is used in industry for the 3D integration of ICs, but is not yet common for detector instrumentation. An effort to study the suitability of TSVs for dense interconnects, with good power/signal integrity, is on-going within the framework of a CERN R&D programme and the Timepix collaboration. We have used Timepix4 [1] as our test-vehicle.

Timepix4 is a large-area pixel read-out IC, with external connections designed to connect to the carrier PCB using wire-bonds, with the option to create and use TSVs instead. Each I/O and power connection of the chip has a landing pad in the backend-of-line stack which can be accessed by a TSV fabricated from the back-side. Here, a RDL connects to a ball-grid-array (BGA). The 3D nature of the TSVs combined with the RDL allows accessing signals and power nets from anywhere on the bottom surface of the die. Using wire-bonding, only the peripheries of the die are accessible. With TSVs, wire-bond pads are not needed and can be diced-off, making the chip four-side buttable with minimal dead-area.

Several batches of Timepix4 have undergone TSV processing, performed by Fraunhofer IZM. The 300mm wafers were cored to 200mm, followed by thinning down to 120um. The TSVs created have a diameter of 55um.

For testing, a family of printed-circuit boards was designed: a BGA-test socket board to electrically test and identify good chips; a break-out board to extract the high-speed data signals from Timepix4; a thermal cycling board to study the quality of the BGA array; and a module-demonstrator for testing the integration between Timepix4 and VTRx+ [2] opto-electronics modules. Tests have demonstrated data transmission from TSV-processed Timepix4 at 5 Gbit/s with good power integrity. Co-integration of the Timepix4 and opto-electronics is a proof-of-principle for future particle-tracker modules.

An alternative technique for connecting chips to boards is Anisotropic Conductive Paste (ACP). It consists of tiny metal spheres mixed with glue. A flip-chip bonding machine has been used for trials of permanently bonding Timepix4 samples to carrier boards, using this method. A comparison between soldering by BGA and with ACP will be presented.

[1] https://cds.cern.ch/record/2825271?ln=en
[2] https://cds.cern.ch/record/2312396?ln=en

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