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Pixel detector hybridization with anisotropic conductive adhesives

Developing a cost-effective single-die pixel-detector hybridization method using Anisotropic Conductive Films (ACF) or Anisotropic Conductive Paste (ACP) aims to replace fine-pitch bump bonding with conductive micro-particle embedding in adhesive film or paste. This technology enables integration of hybrid or monolithic detectors in modules, replacing wire bonding or solder-bumping. Within the scope of this project, also an Electroless Nickel Immersion Gold (ENIG) plating process has been developed for single-die chips to achieve the required pixel pad topology. This contribution introduces the ENIG, ACF and ACP processes, alongside test results from test structures, functional chips and hybrid pixel assemblies with flip-chip bonding.

Summary (500 words)

In the development of hybrid pixel detectors, a reliable and cost-effective interconnect technology is paramount. This technology must be tailored to the specific pitch and die sizes of the applications at hand. Particularly crucial during the ASIC and sensor development phases, these interconnection technologies must also accommodate the assembly of single dies, commonly available from Multi-Project-Wafers.

Within the CERN EP-R&D program and the AIDAinnova collaboration, innovative and scalable hybridization concepts are pursued for pixel-detector applications in future colliders. The recent focus has been on developing a reliable single-die interconnection process based on Anisotropic Conductive Adhesives (ACA). Two different approaches are studied: Anisotropic Conductive Paste (ACP) and Anisotropic Conductive Film (ACF). These ACA technologies replace solder bumps with conductive micro-particles embedded in an adhesive layer, applied either as film or paste. The electro-mechanical connection between the sensor and ASIC is achieved through thermo-compression of the ACA using a flip-chip device bonder. The ACA technology demonstrates versatility by also facilitating ASIC-PCB/FPC integration, offering a viable alternative to wire bonding or large-pitch solder bumping techniques.

A critical aspect of the ACA approach is the necessity for a specific pixel-pad topology, enabling connection via micro-particles and creating cavities for excess adhesive flow. This pixel-pad topology is achieved through an in-house Electroless Nickel Gold (ENIG) process, which is concurrently under development within the project.

The ENIG and ACA processes are rigorously qualified with various ASICs, sensors, and dedicated interconnect test structures, featuring pad diameters ranging from 10 µm to 140 µm and pitches between 20µm and 1.3mm. Thanks to recent process optimizations, an excellent ENIG plating yield has been achieved, with nearly 99% of pads correctly plated. For flip-chip assemblies using ACF and ACP, the rate of correctly connected pads is close to 98% for chips with large pad dimensions and pitches (80µm pads with a 200µm pitch). Current efforts focus on chips with pad dimensions around 10µm with a 25µm pitch, aiming to achieve similar connection rates for these smaller dimensions. Several projects participate with readout ASICs and sensors in the qualification of the assembly process, including Timepix3 with 12-14µm exposed pad diameter, 55µm pitch on a 2cm² bonding surface, ESRF SPHIRD with 15µm exposed pad diameter, 50µm pitch on a 5 mm² surface, ALTIROC2/3 with 90 µm exposed pad diameter, 1.3 mm pitch on a 4 cm² surface, and CLICpix2 with 12µm exposed pad diameter, 25 µm pitch on a 2.6 mm² surface. The assemblies produced undergo comprehensive electrical characterization, including tests with radioactive-source exposures and high-momentum particle beams. Additionally, thermal cycling is conducted to study the robustness and potential aging of the assemblies. Initial results show good resistance of the interconnections to temperatures ranging from -40℃ to 120℃.

In summary, this contribution serves to introduce the developed interconnect and plating processes, highlighting several types of hybrid assemblies produced and tested using the aforementioned methods. Notably, recent optimizations in plating and interconnect processes have led to improved plating uniformity and interconnect yield, enhancing the overall reliability and performance of hybrid pixel detectors.

Primary author: Dr LALE, Ahmet

Co-authors: VOLKER, Alexander (KIT - Karlsruhe Institute of Technology (DE)); MAGALHAES SUAREZ, Debora; DANNHEIM, Dominik (CERN); CALDERINI, Giovanni (LPNHE-Paris, Centre National de la Recherche Scientifique (FR)); BANGARU, Haripriya; KRISTIANSEN, Helge (Conpart AS); SCHMIDT, Janis Viktor (KIT - Karlsruhe Institute of Technology (DE)); BRAACH, Justus (CERN, Hamburg University (DE)); Mrs RUAT, Marie (ESRF); VICENTE BARRETO PINTO, Mateus (Universite de Geneve (CH)); CENTIS VIGNALI, Matteo (FBK); Dr SVIHRA, Peter (CERN); DE OLIVEIRA, Rui (CERN); YANG, Xiao (CERN)

Presenter: Dr LALE, Ahmet

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