

Next generation fully integrated DCDC converters for HEP applications in 28nm technology

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Outline

Context and motivation

Family of fully integrated voltage regulators

- iPOL5V
- iPOL2V3
- LinPOL1V2

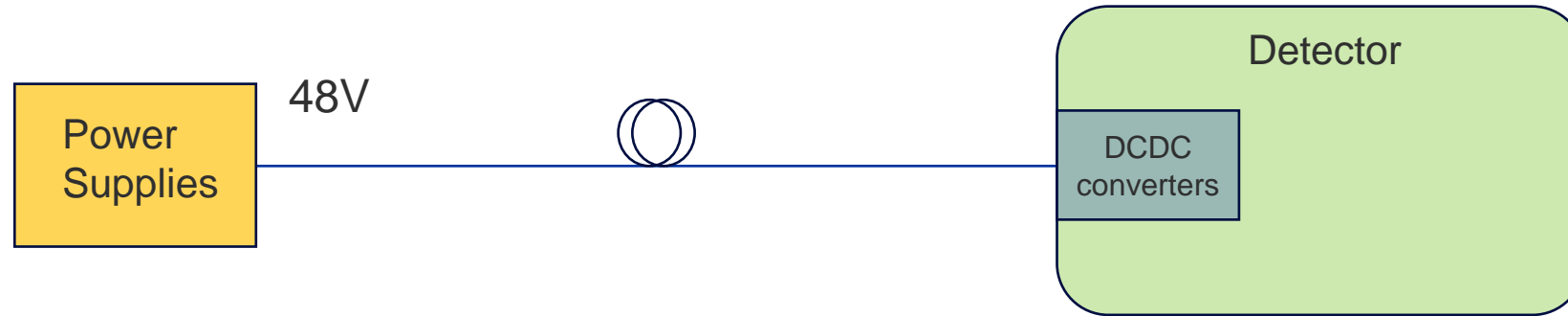
i = integrated
POL = Point of Load
value = input voltage rating
Lin = linear regulator

Experimental results

Summary, future work

Context and motivation

Power Distribution Scheme



Challenges

- Need of high current to power front end ASICs
- Total Ionizing Dose up to 1Grad
- Magnetic field up to 4T

Countermeasures

- High conversion ratios to reduce current in cables
- Deep submicron technologies
- Air core inductors

All the developments are under EP R&D WP 5.4 for future experiment upgrades and future colliders

Context and motivation

Present Power Distribution scheme

Stage 1: $V_{in} = 48V$



Stage 2: $V_{in} = 12V$



Stage 3: $V_{in} = 2.5V$

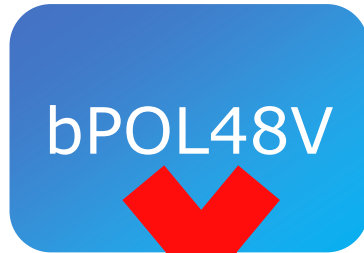


1V

Context and motivation

Present Power Distribution scheme

Stage 1: $V_{in} = 48V$



Stage 2: $V_{in} = 12V$



Stage 3: $V_{in} = 2.5V$



1V

production fab closed
enough stock LS3,LS4

Context and motivation

Present Power Distribution scheme

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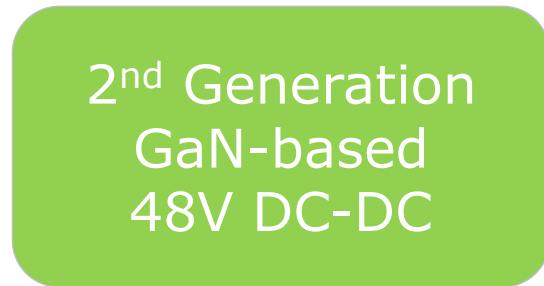


1V

production fab closed
enough stock LS3,LS4

Proposed future Power Distribution scheme

Stage 1: $V_{in,max} = 48V$



Inductor-based topology
external

5V or 2.3V

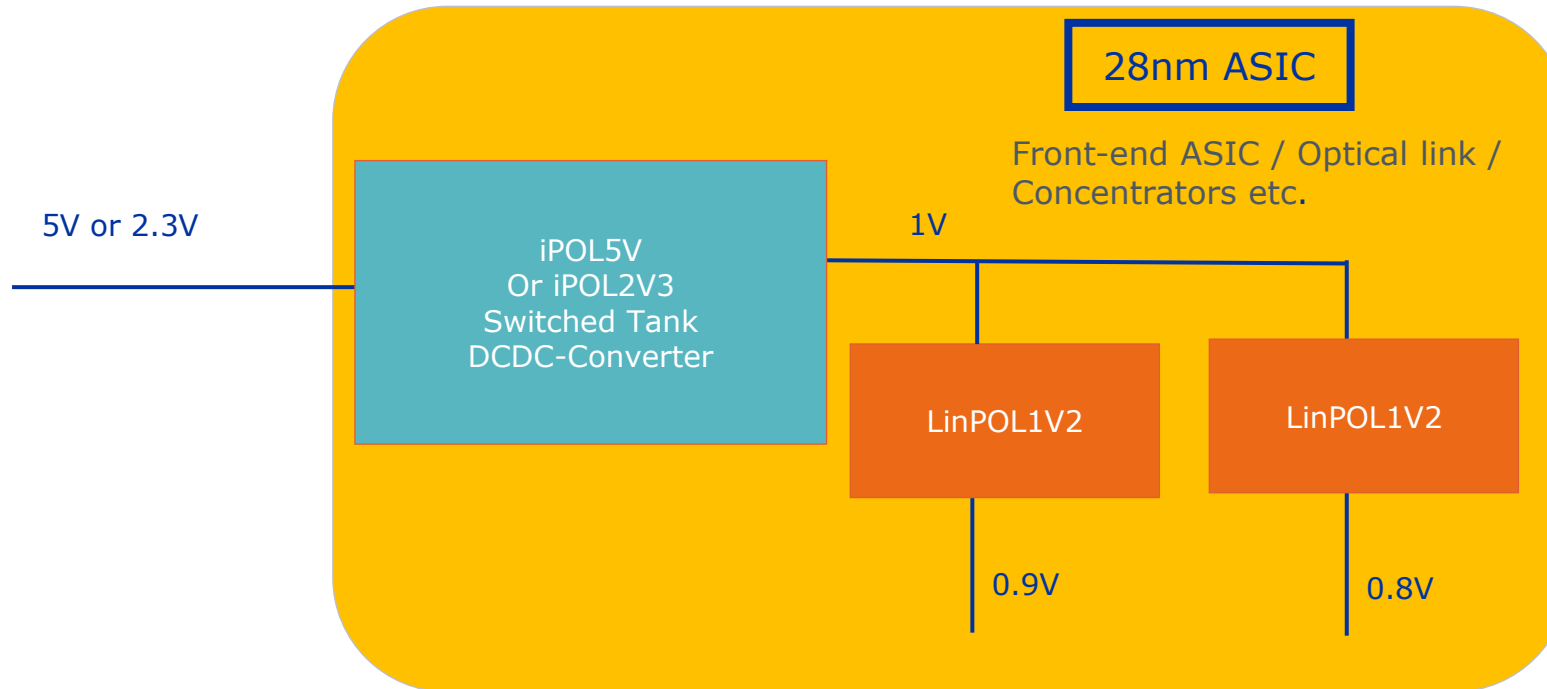


Stage 2: **On chip** $V_{in,max} = 5V$



Fully integrated converters
internal

Context and motivation



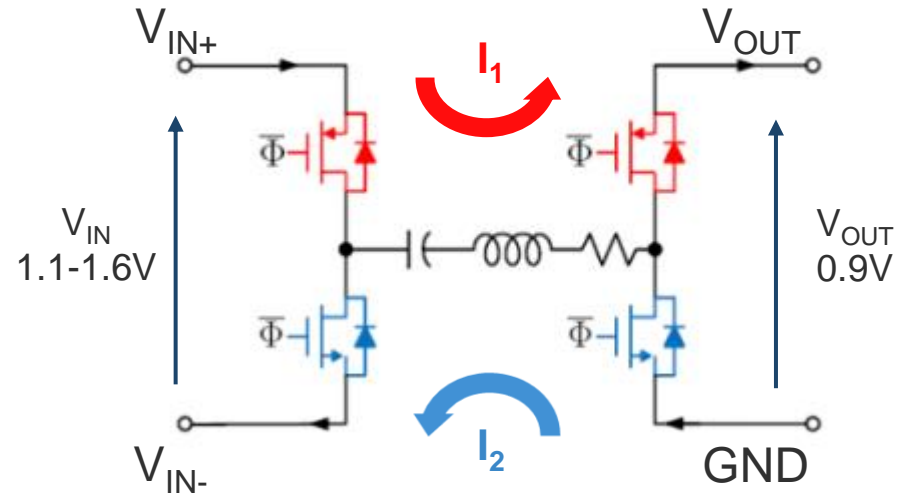
- A fully integrated DCDC will provide 0.9-1V on chip
- Different low noise voltage domains can be created using full integrated LDO
- Fabricated in 28nm CMOS technology using only core transistors
- Distributed as IP blocks to 28nm front end chip designers
- NO external components (including inductors and capacitors)

Family of fully integrated Voltage regulators

Name	Type	V_{IN}	V_{OUT}	I_{OUT} Max	Status
iPOL5V	3-stage Resonant Switched Tank DCDC converter	$4.75 \pm 0.25V$	$0.9 \pm 0.1V$	500mA	Prototyped Q4 2023
iPOL2V3	1-stage Resonant Switched Tank DCDC converter	$2.3 \pm 0.2V$	$0.9 \pm 0.1V$	250mA	
LinPOL1V2	Linear Regulator	1.2V	$0.9 \pm 0.1V$	200mA	

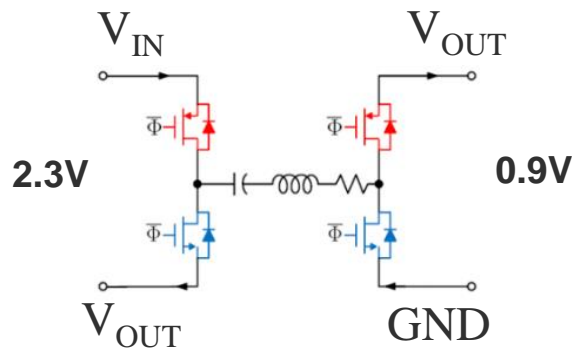
Switched Tank Converter - Basic cell

STC Basic cell



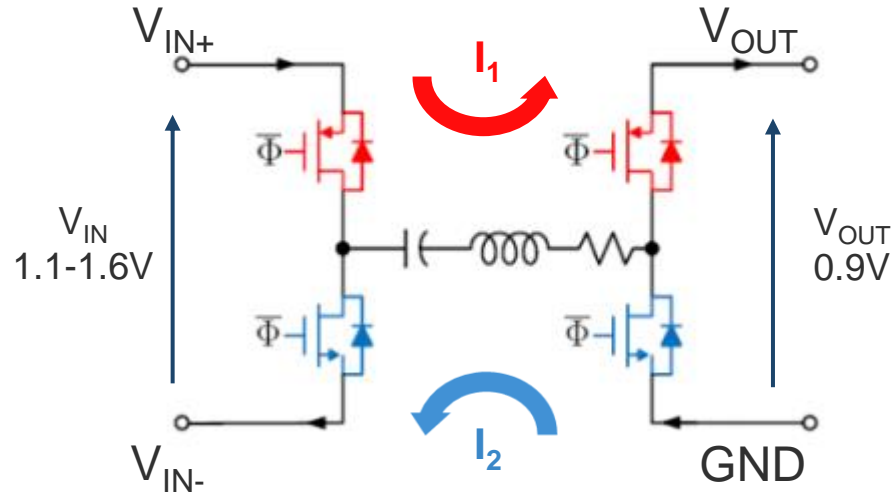
- Modified Switched Tank converter
- Φ low \rightarrow I1
- Φ high \rightarrow I2
- IN – OUT are AC coupled
No DC path from Vin to Vout
- Stack more stages possible
- 2 different configurations

iPOL2V3 - Single Stage

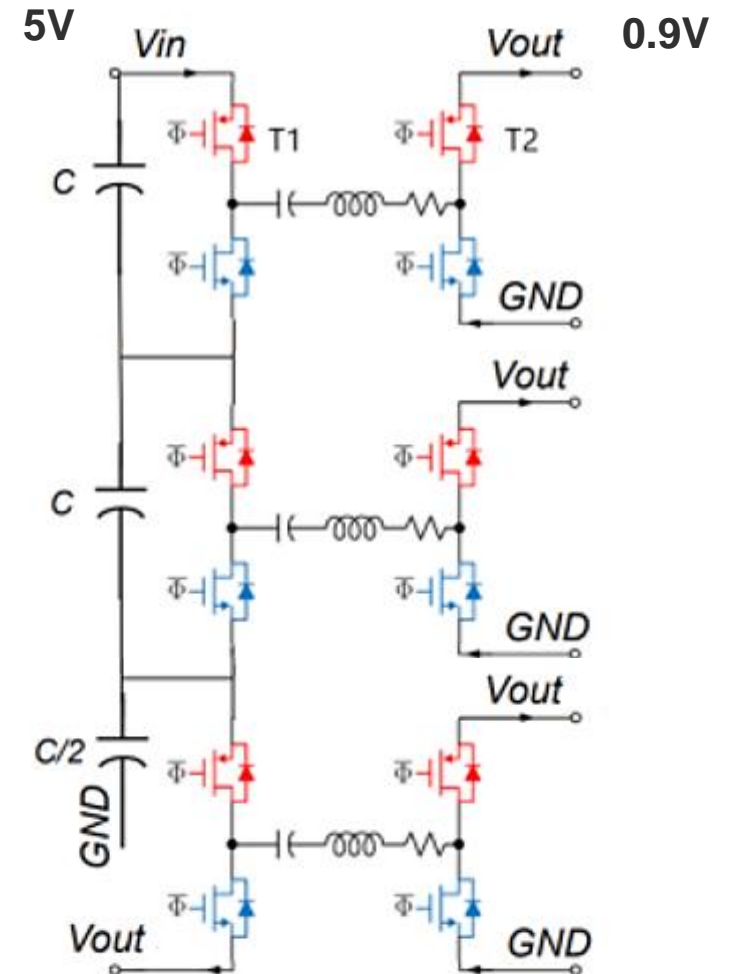


Switched Tank Converter - Basic cell

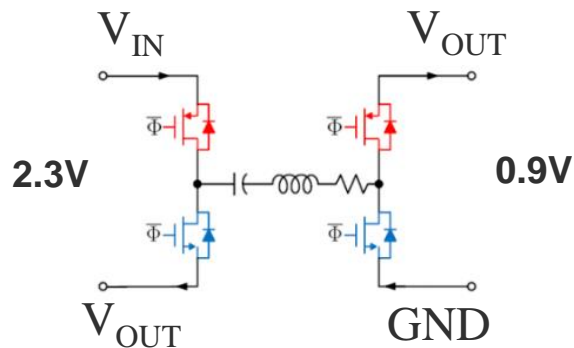
STC Basic cell



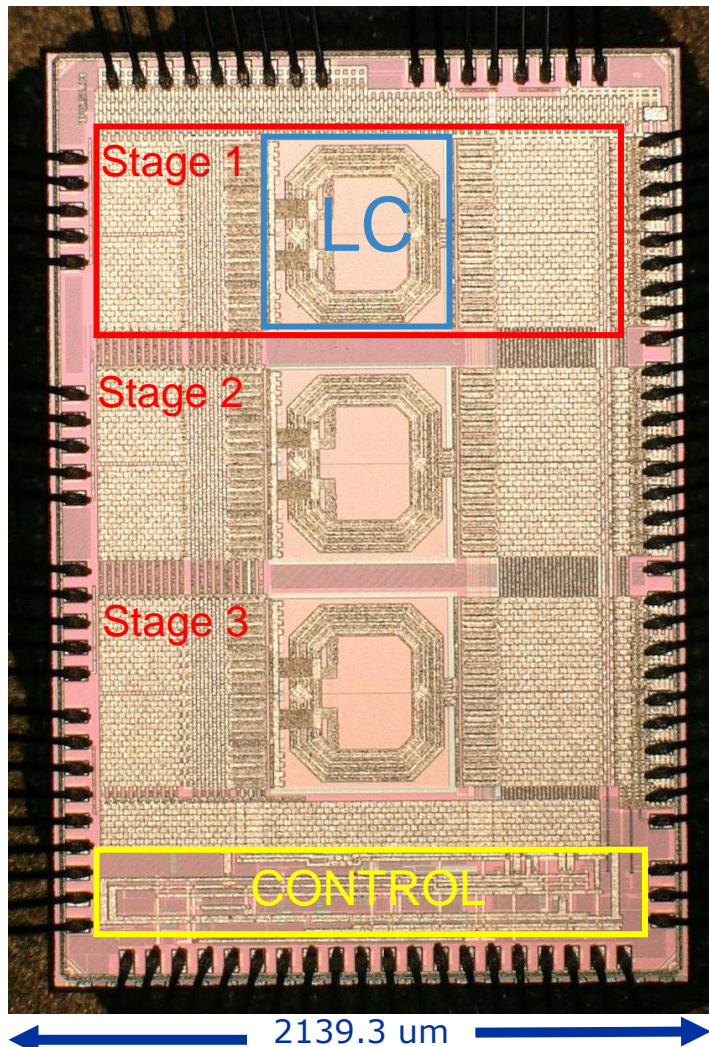
iPOL5V – Three Stages



iPOL2V3 - Single Stage



iPOL5V



Fully integrated 3 stage DCDC switched tank converter in 28nm CMOS

- Optimized for 5V to 0.9V conversion, $I_{IN} \approx \frac{1}{4} I_{OUT}$
- V_{out} can be regulated to lower values by adjusting T_{on}
- Only core devices used to reduce losses and increase rad-tolerance
- All capacitors and inductors are integrated on chip
- $f_{sw} = 150MHz$

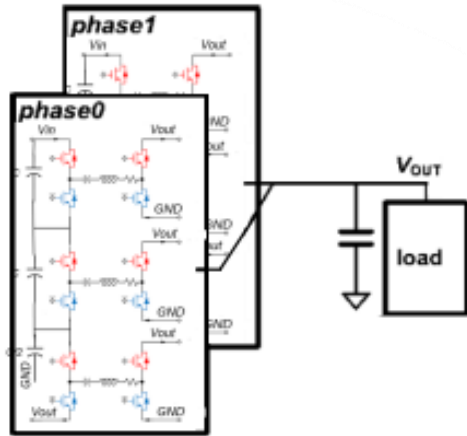
3179.34 um

- Control part is supplied by an external 0.9V power supply, Ongoing work to supply with an internal linear regulator
- Same procedure for the 150MHz oscillator

- ASICs Submitted in November 2023
- First prototypes and Test campaign from March 2024

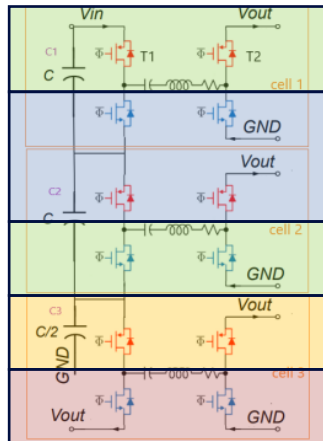
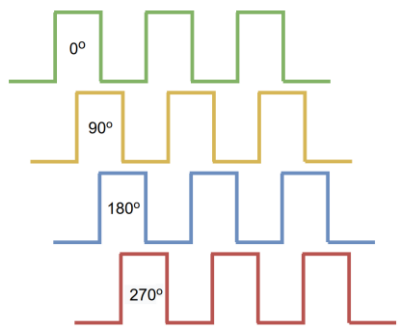
iPOL5V

Multi phase operation



- Dual phase complementary operation (180° phase shift)

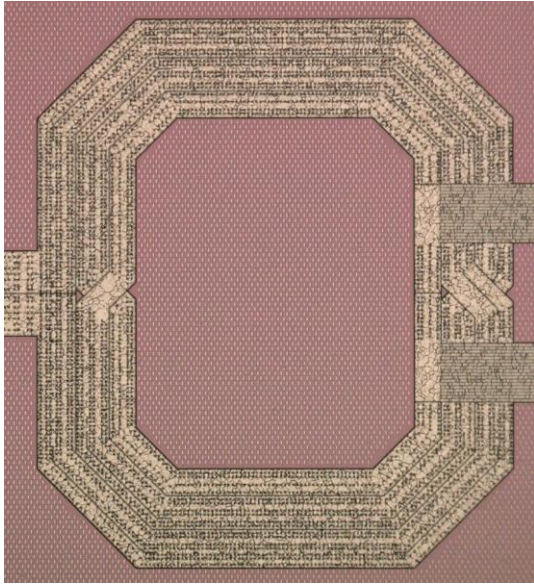
Increases the current capability and reduces the input ripple
→ reduce C_{IN} and C_{OUT}



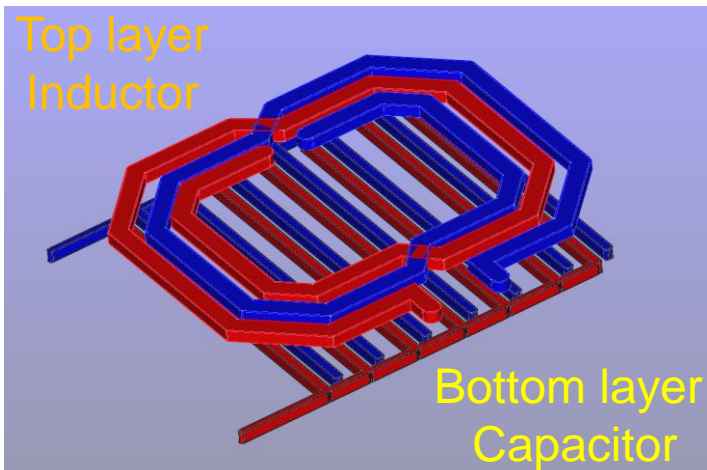
- 90° phase shift between each stage
 - 180° phase shift between pMOS - nMOS

Minimizes the output voltage ripple → reduce C_{OUT}

On chip Inductor



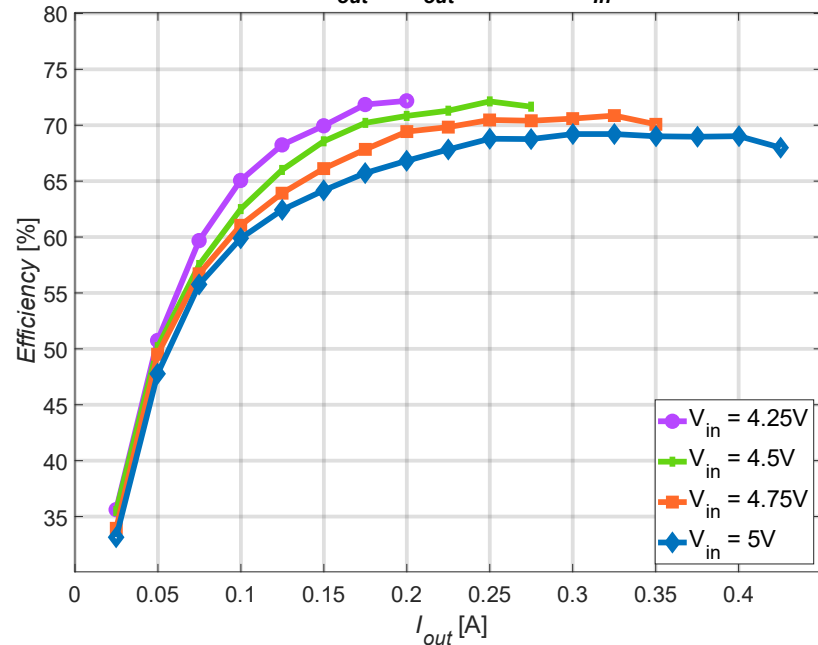
- Custom coupled air core inductor using Top metals
- Coupling between the 2 phases increases the equivalent inductance:
$$L_{eq} = L (1 + k) = 2.96 \text{ nH},$$
self-inductance of each winding is $L = 1.89 \text{ nH}$
coupling factor $k = 0.567$
- Coupled inductor reduces the area required by the tank capacitor
- Series resistance **500mOhm**
- Resonant capacitors **380pF Metal-Oxide-Metal (MOM)**



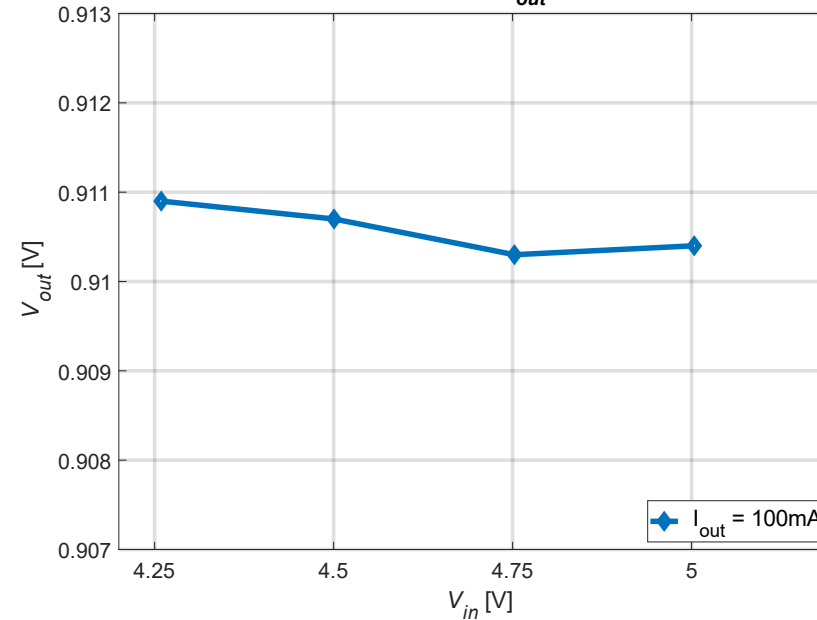
$$f_{sw} = f_{res} = \frac{1}{2\pi\sqrt{L_r C_r}} = 150 \text{ MHz}$$

iPOL5V Radiation & Test Results

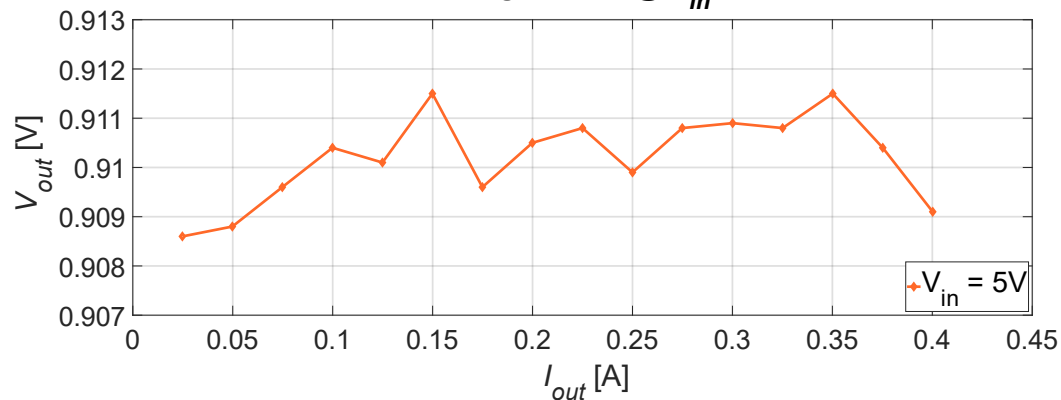
Efficiency vs I_{out} @ $V_{out} = 0.9V$, $Clk_{in} = 150MHz$



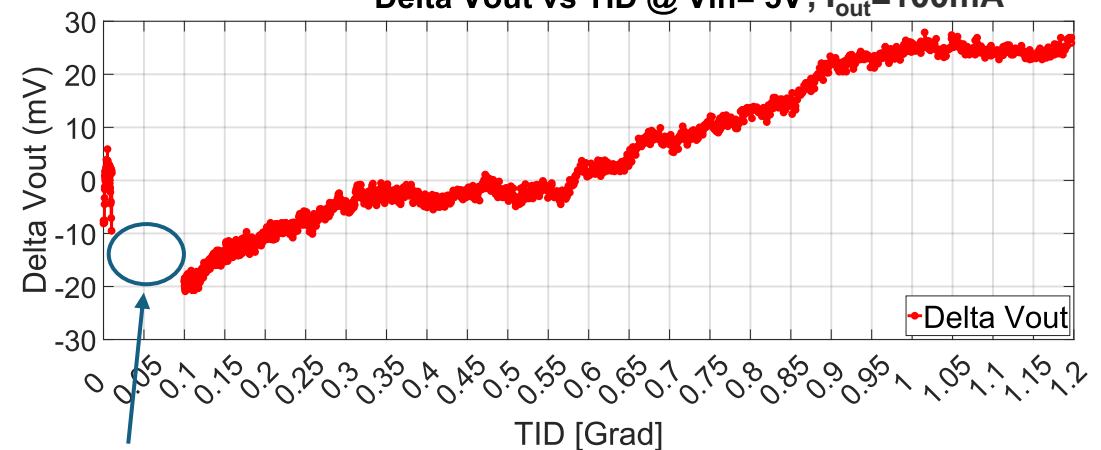
Line regulation @ $I_{out} = 100mA$



Load regulation @ $V_{in} = 5V$



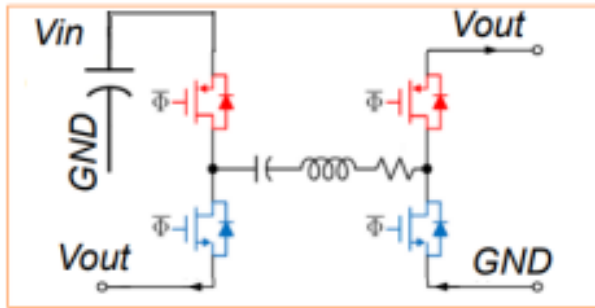
Delta Vout vs TID @ $V_{in} = 5V$, $I_{out} = 100mA$



Functional issue due to 5V Nwells-Psub leakage

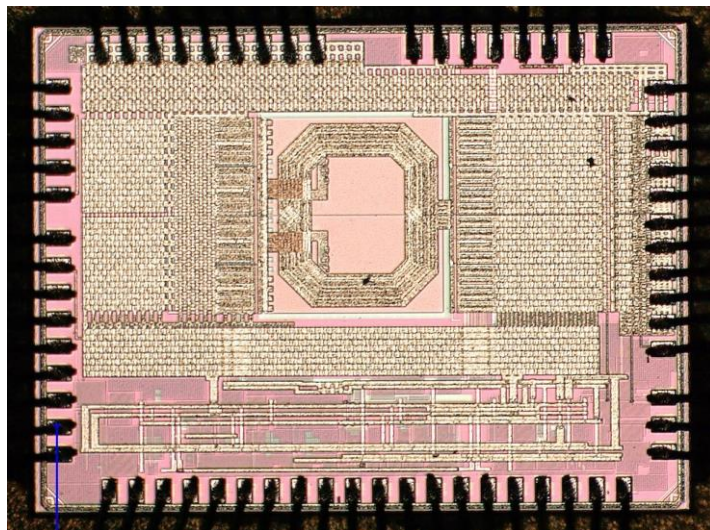
iPOL2V3

Power Part



Fully integrated single stage DCDC switched tank converter in 28nm CMOS

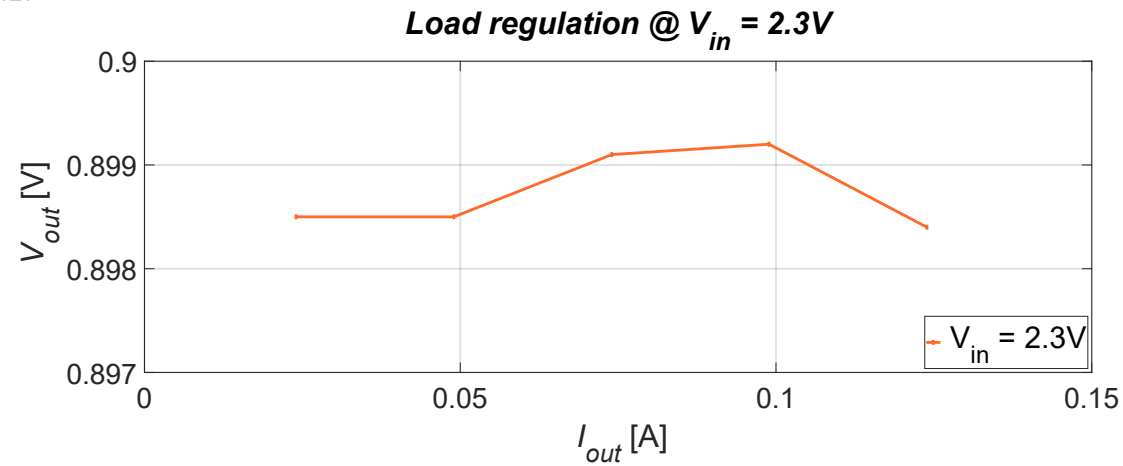
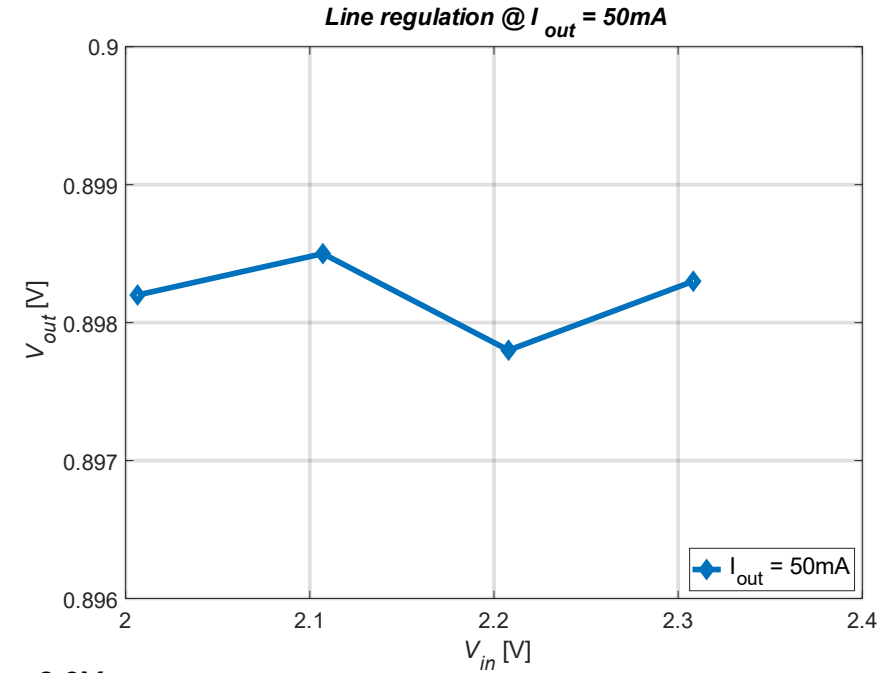
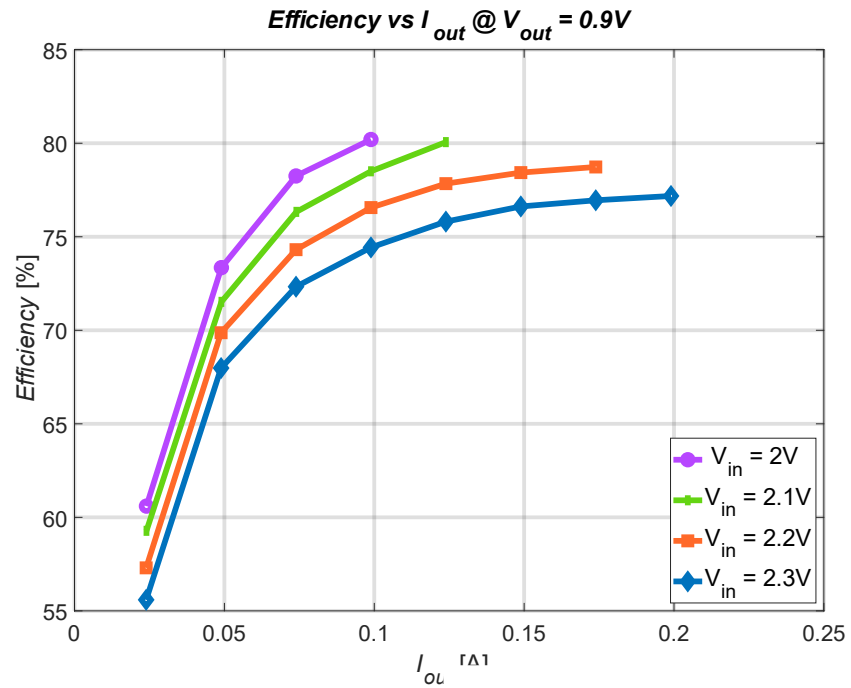
- Optimized for 2.3V to 0.9V conversion, $I_{IN} \approx \frac{1}{2} I_{OUT}$
- Only one resonant cell used
- Vout can be regulated by adjusting Ton
- Only core devices used
- Same control circuit and coupled inductor
- $f_{sw} = 150MHz$



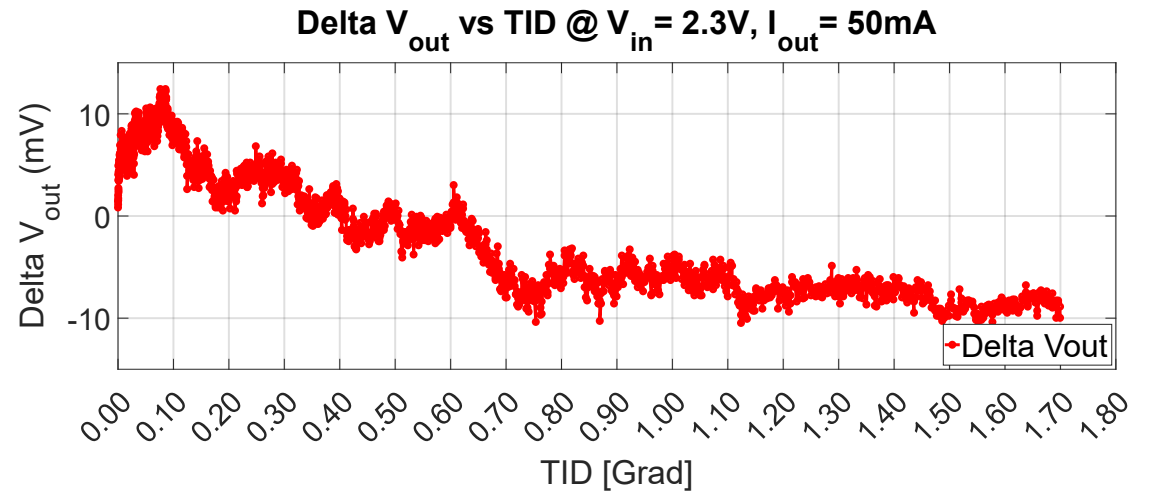
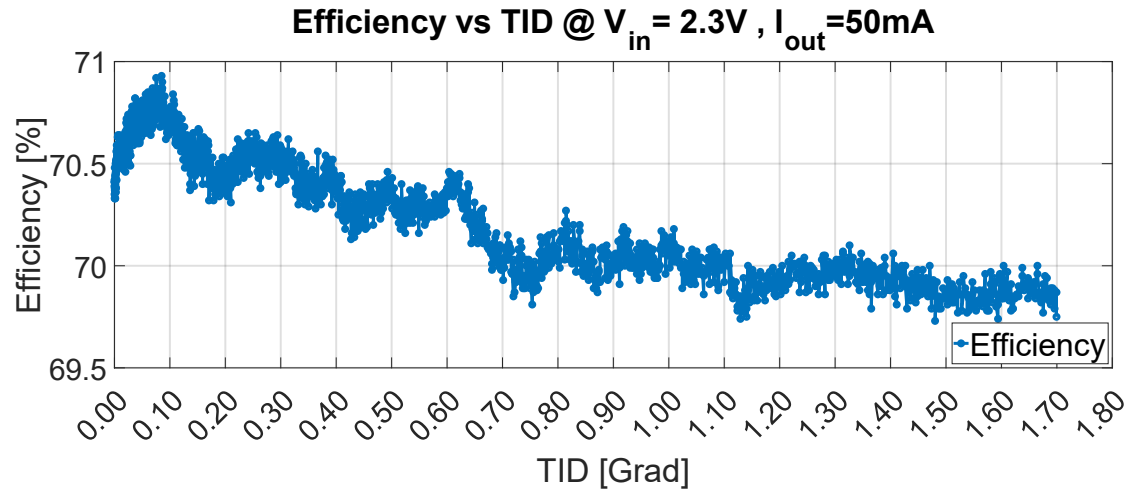
1604.7 um

2139.3 um

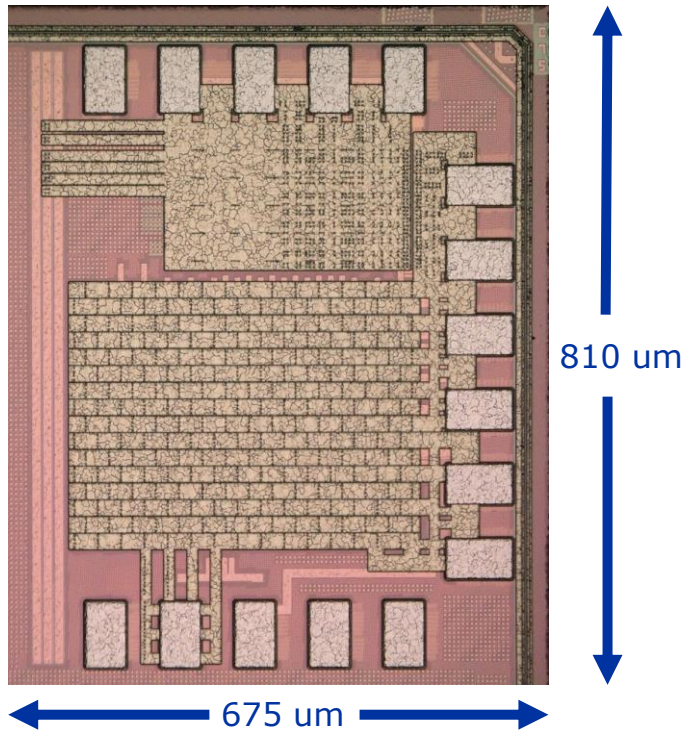
iPOL2V3 Test Results



iPOL2V3 Radiation Results

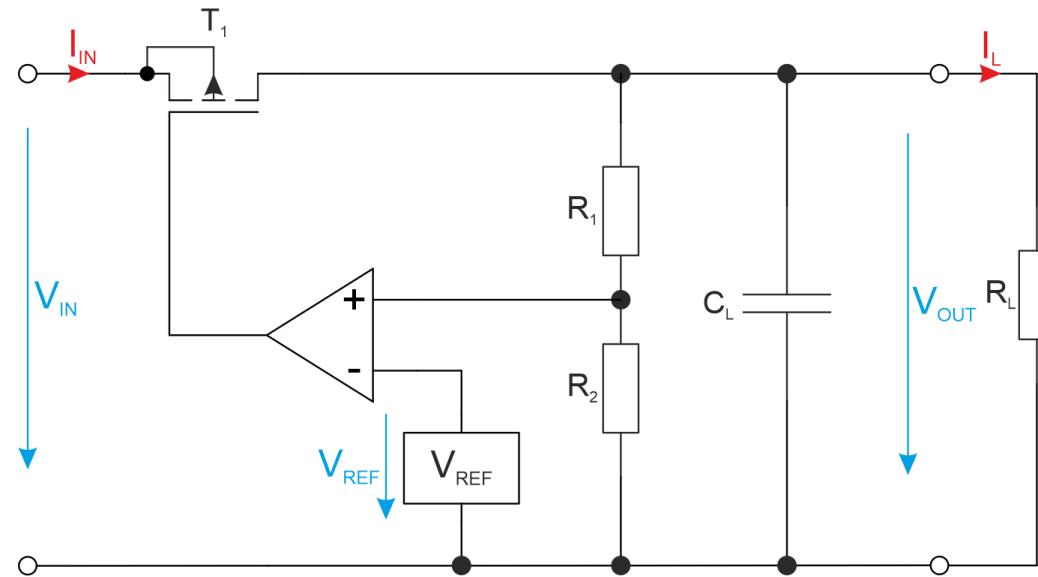


LinPOL1V2



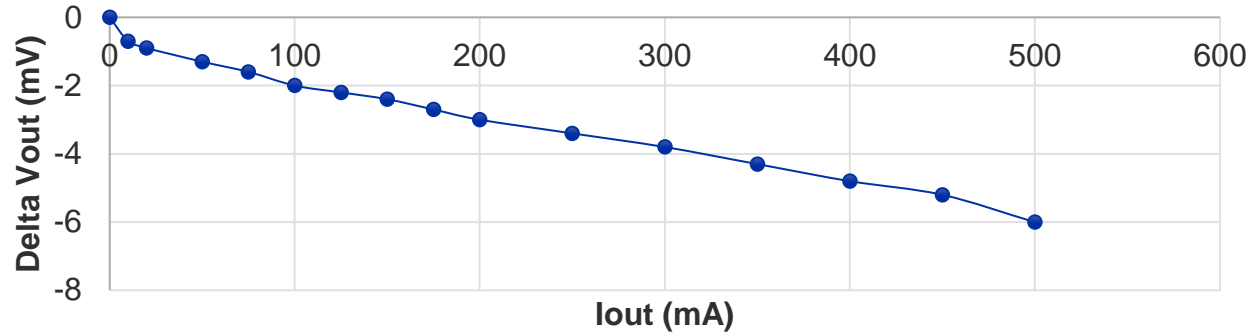
Fully integrated low drop-out linear regulator in 28nm CMOS

- Input voltage range from 0.9 to 1.2V
- Max output current 200mA
- Only core devices used

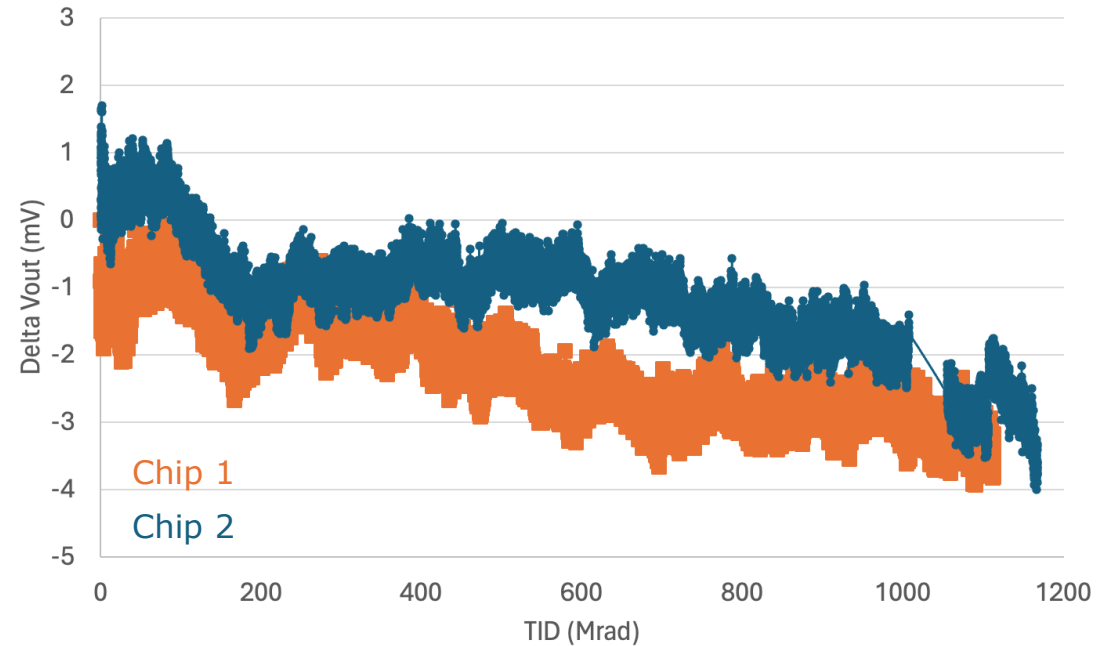


LinPOL1V2 Radiation & Test Results

Delta Vout vs Iout
@ Vin=1V, Vout=0.9V



Delta Vout vs TID
@ Vin=1V, Vout=0.9V, Iout=100mA



Summary

Conclusion

- The 3 prototyped ASICs iPOL5V, iPOL2V3 and LinPOL1V2 are fully working and operative
- iPOL2V3 and LinPOL1V2 are fully functional up to 1Grad
- iPOL5V shows TID issues between 10Mrad and 100Mrad, while functional in the 100Mrad – 1Grad range (issue understood, fixes are being implemented)

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Future work

- TID issue of iPOL5V addressed in submission November 2024
- Design of new Linear regulators to supply the control circuitry of iPOL5V and iPOL2V3 during the start-up phase
- Design of an internal oscillator
- SEE tests in 2025
- Improve efficiency and make possible sharing of the output for higher current needs
- Reliability assessment (rack with 50 iPOL5V and 50 iPOL2V3 is under construction)



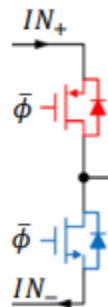
Thank you

Spare slides

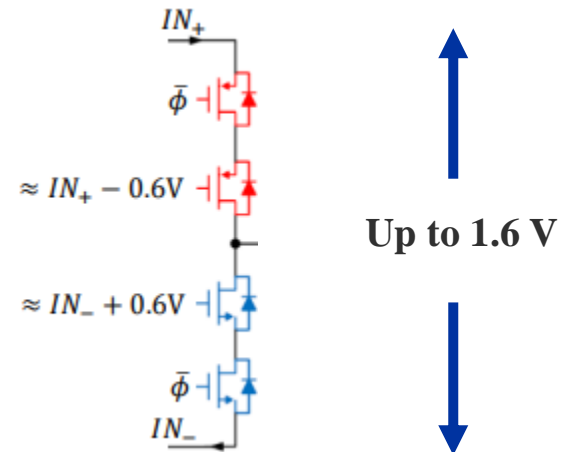
Power switch implementation

- Only core transistors are used also in the power stage (for improved efficiency and radiation tolerance).
- 2 core transistors rated 0.9V are stacked
- The one is switching while the other has a fixed bias to ensure safe operation

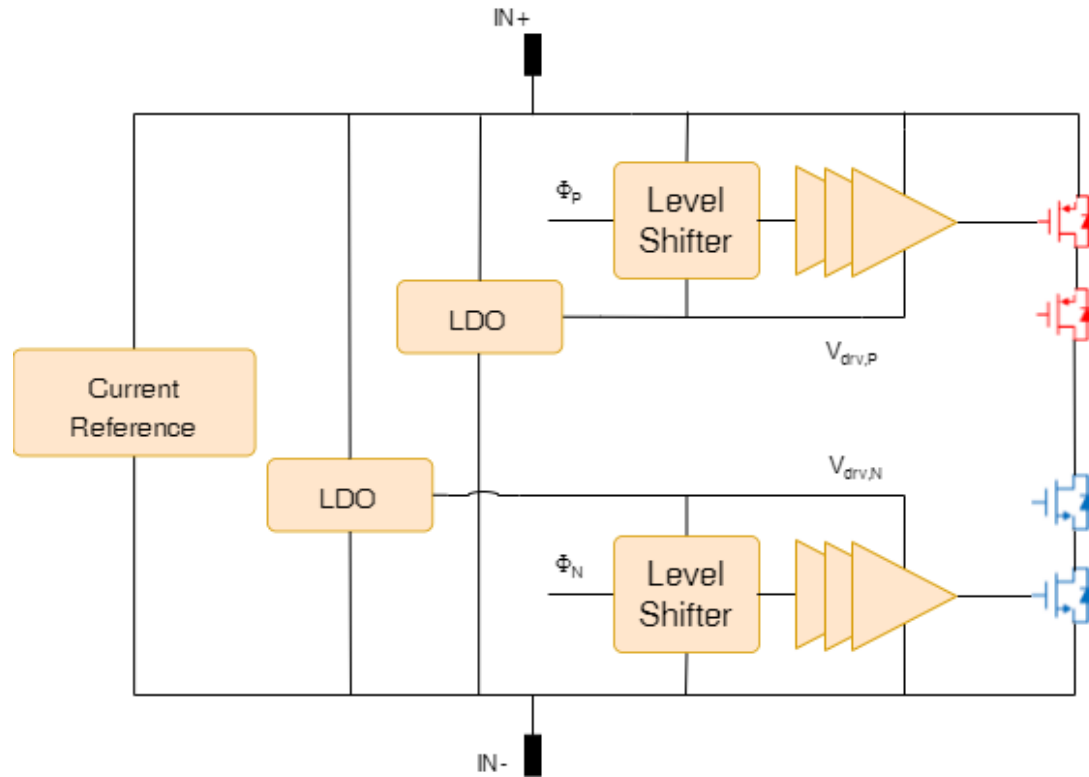
Idea



Actual implementation

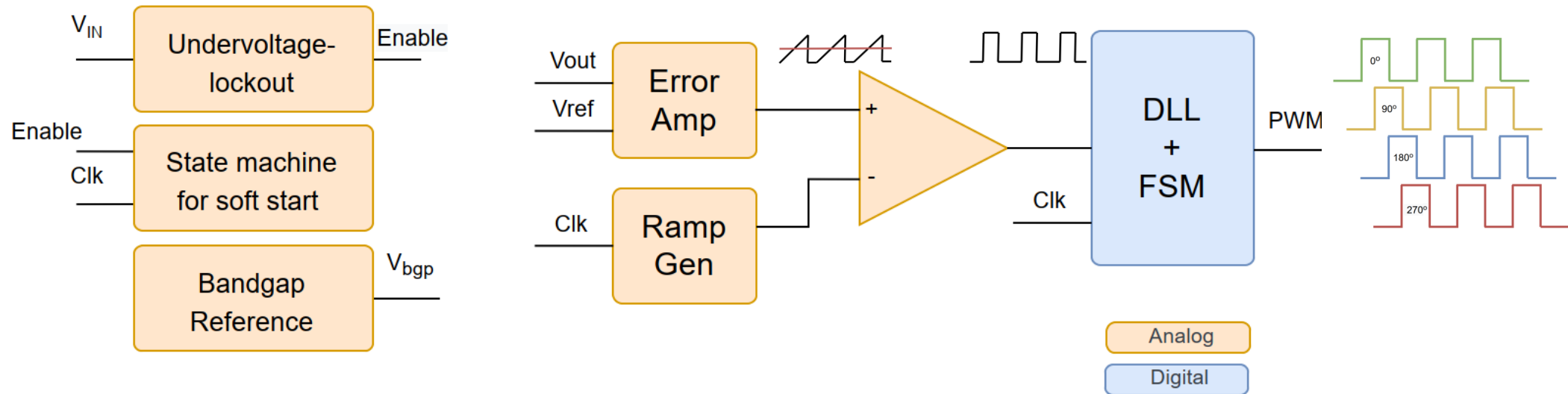


Power Stage half bridge of single stage



- LDOs generate the 0.9V domain of the gate drivers
- Level shifters
- Gate drivers

iPOL5V Control Circuit



- Error Amp, Ton generator, DLL
- 0.9V power supply
- DLL generates the 90° phase-shifted PWM signals that drive the power stage
- Use of external 150MHz clock (for this prototype, will be added in final ASIC)