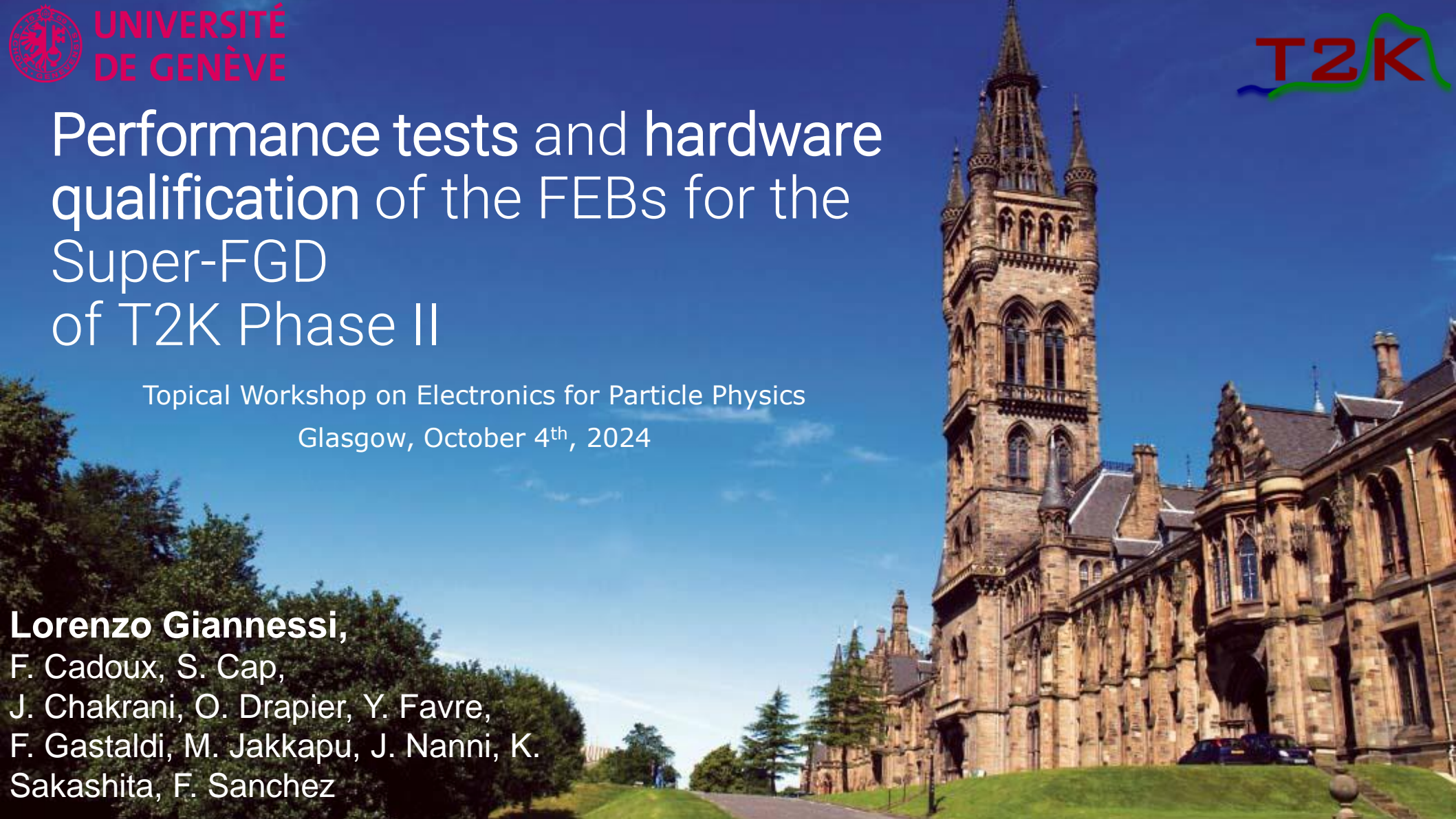


Performance tests and hardware qualification of the FEBs for the Super-FGD of T2K Phase II

Topical Workshop on Electronics for Particle Physics
Glasgow, October 4th, 2024

Lorenzo Giannessi,
F. Cadoux, S. Cap,
J. Chakrani, O. Drapier, Y. Favre,
F. Gastaldi, M. Jakkapu, J. Nanni, K.
Sakashita, F. Sanchez



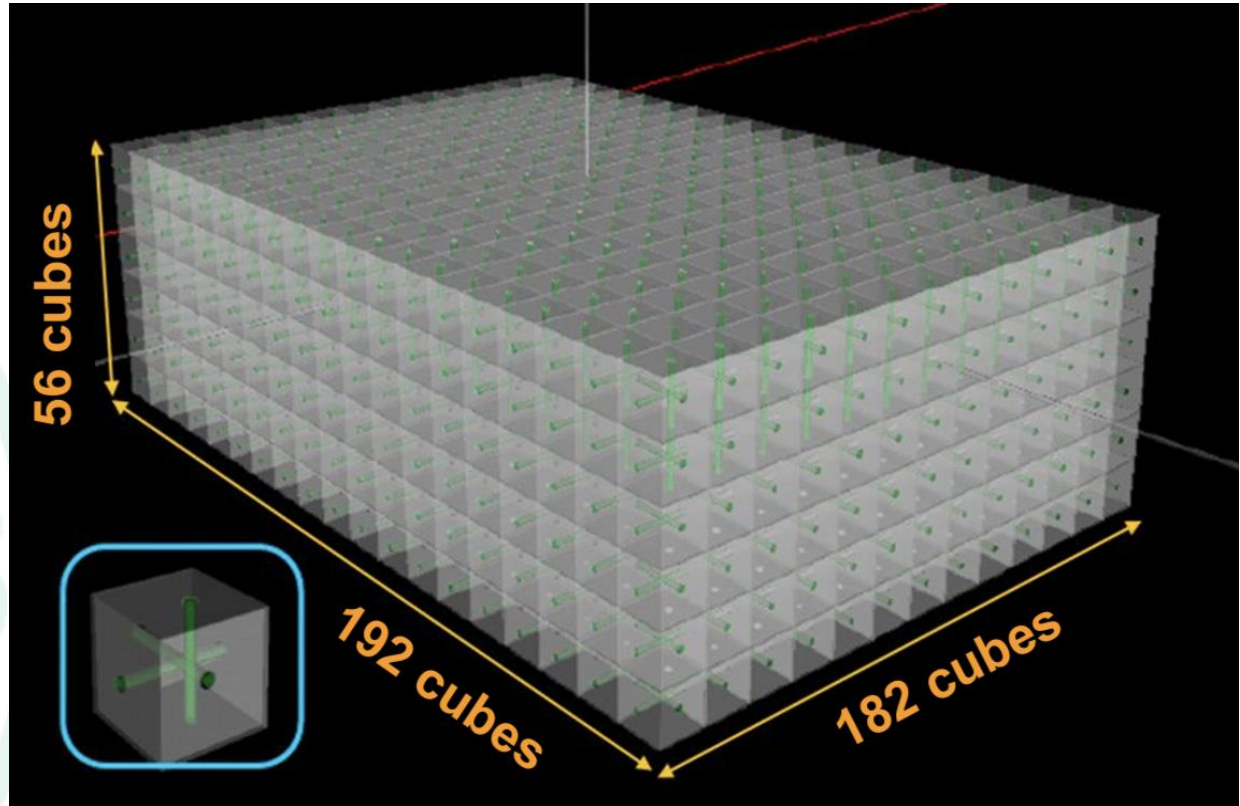
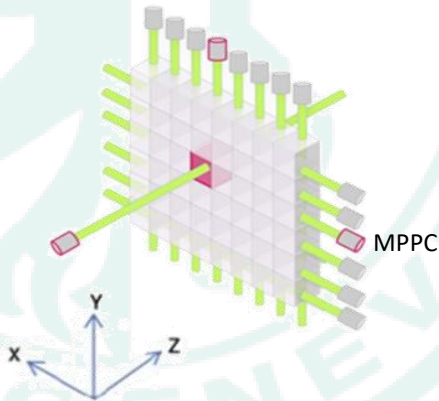
- 1. Introduction: what is the Super-FGD ?**
- 2. Electronics overview**
- 3. Requirements and FEB performance tests**
- 4. FEB mass production serial testing**
- 5. Conclusions**



1. What is the Super-FGD?

New neutrino active target for T2K Near Detector

- 2-million 1-cm³ polystyrene cubes
 - ❖ 2 tons fiducial mass
 - ❖ high granularity
 - ❖ 3D tracking
- ~60k optic fibers + SiPM
 - ⇒ 60k readout channels

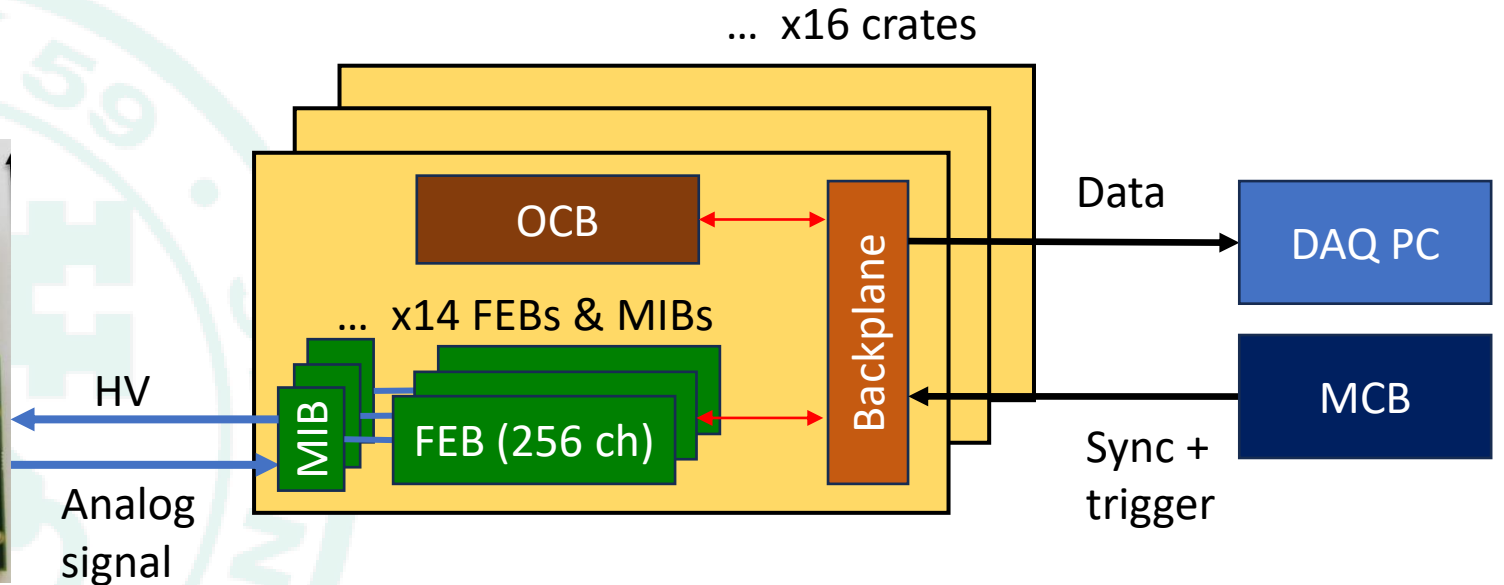
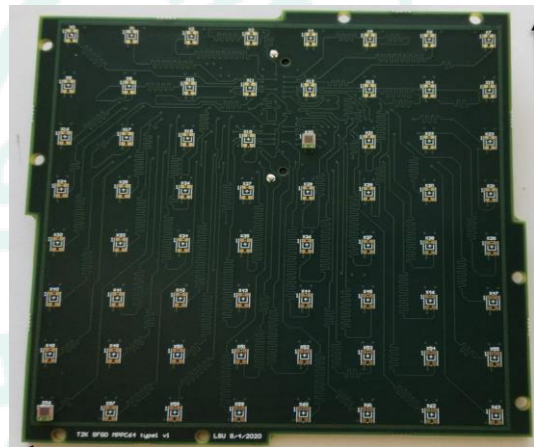


2. Electronics overview and requirements

55'888 SiPM channels \Rightarrow 16 Crates, 14 FEBs each

OCB (1 per crate) and MCB: S/C, data concentration, sync, trigger

Sensors: MPPC64 (x881)



Focus of this talk: FEB:

Amplification, shaping and digitization of 256 channels

256 channel charge + timing readout

➤ 8 CITIROC by Omega [1]:

32-ch read out chips

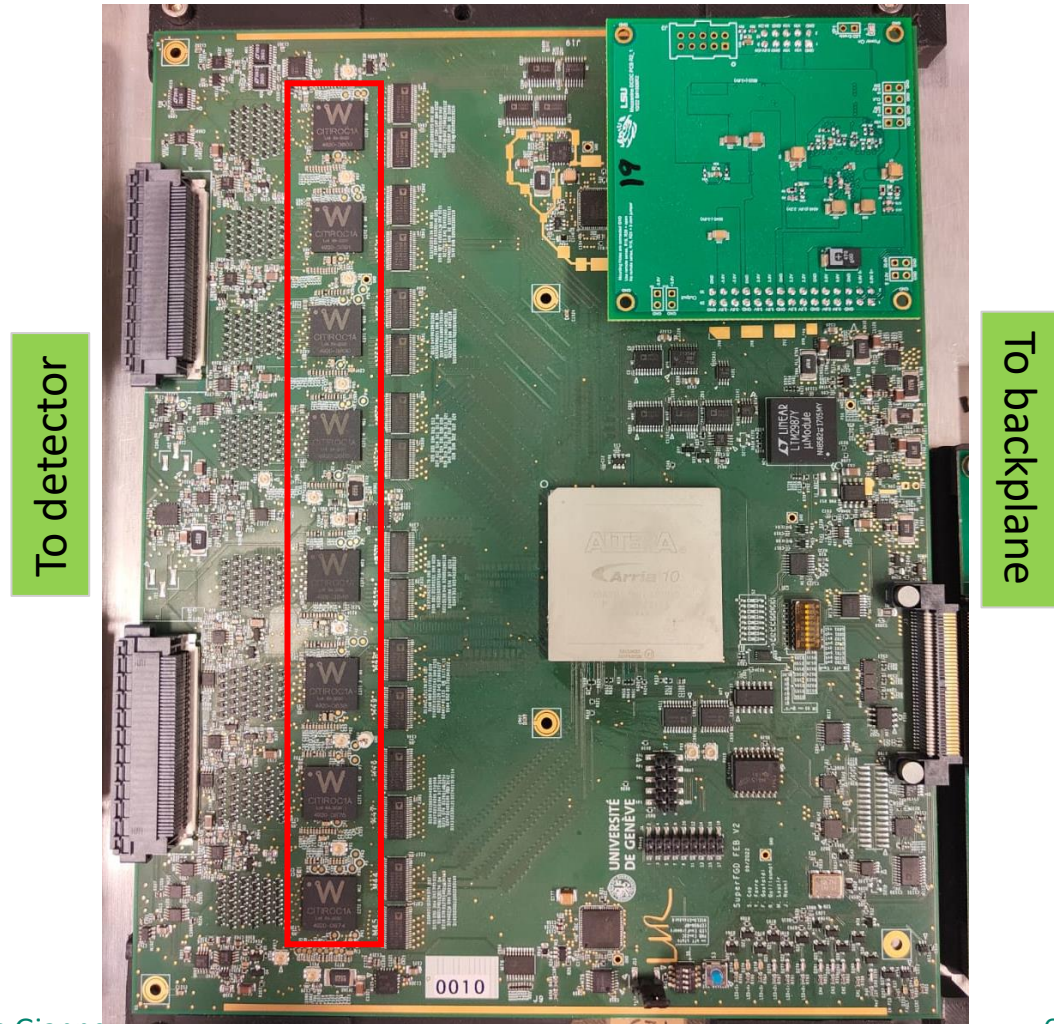
Types of read-out:

- ❖ Timing: constant threshold trigger output
- ❖ Charge: dual gain peak detector (HG, LG)

Programmable devices:

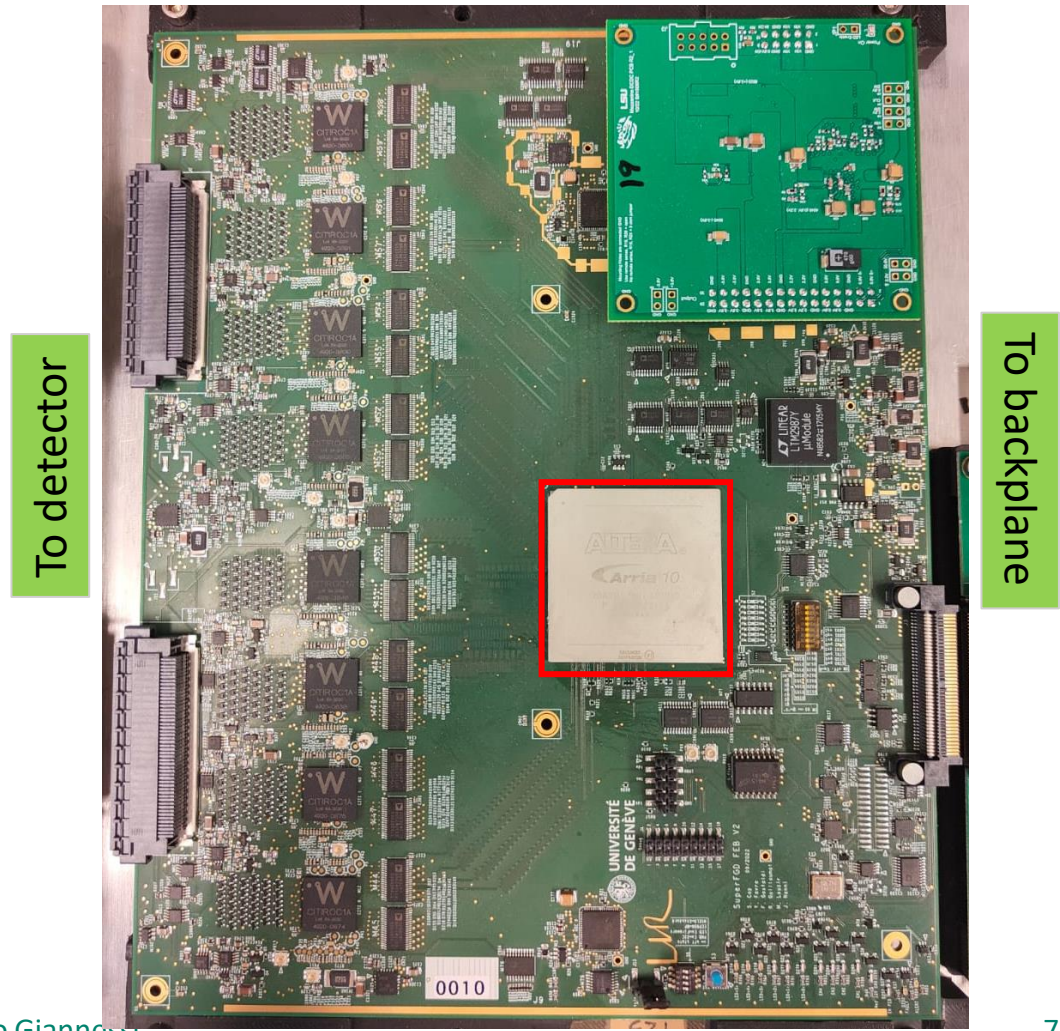
- ❖ Timing and analog thresholds: 10(+4)-bit
- ❖ Gain for charge readout: 6-bit
- ❖ Shaping time: 3-bit

[1] [CITIROC by Omega](#)



Configuration and slow control

- FPGA ARRIA 10
 - ❖ Data concentration and S/C
 - ❖ 400 MHz sampling rate for timing measurement
 - ❖ ROC configuration
 - ❖ Housekeeping
 - ❖ Remote programming

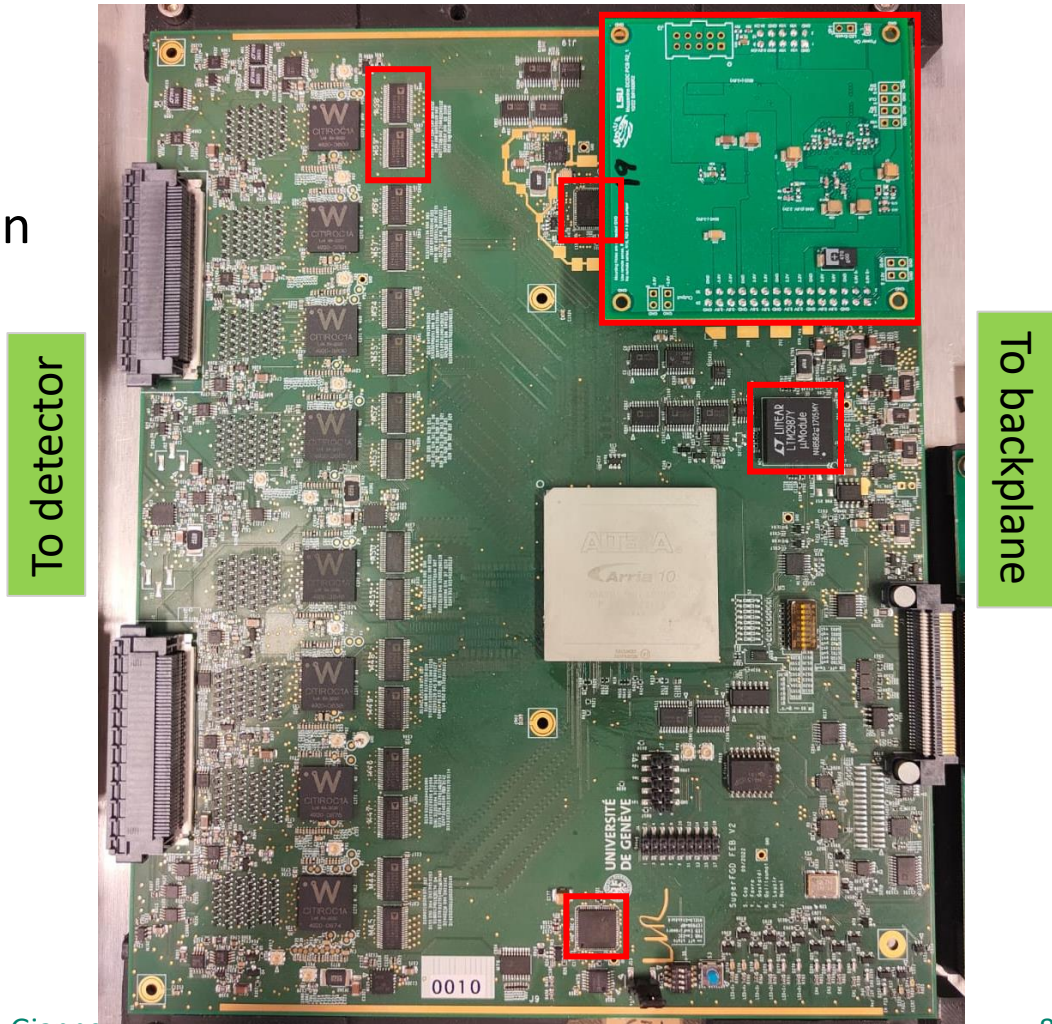


To detector

To backplane

Digitization, power, housekeeping

- Two 8-ch 12-bit ADCs for charge digitization
- Sensors for temperature, voltage and currents
- Supervisor chip
- DC-DC mezzanine board
- 16 3v3-1v8 level translators
- EEPROM for calibration data



To detector

To backplane

3. Requirements and performance tests

Validation of the FEB design against detector requirements

- Dynamic range: 1 – 1000 p.e (or 100 fC – 100 pC)
- Energy resolution < 1 p.e. in HG mode
- Electronics cross talk below 1%
- 1 ns timing resolution

Challenges:

~1 year for production + hardware testing + installation

Limited space inside UA1 magnet

~10 years expected lifetime



Dynamic range & energy resolution

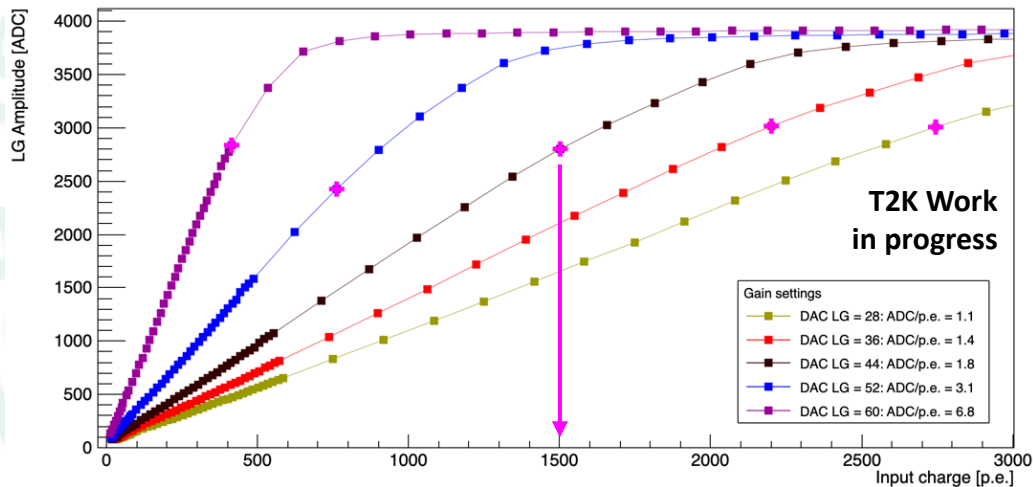
Dynamic range

Limited by **non-linearity** of the CITIROC response.

Upper limit: LG linear limit

LG linear limit > 1000 p.e

FEB low-gain signal response (ch 0)



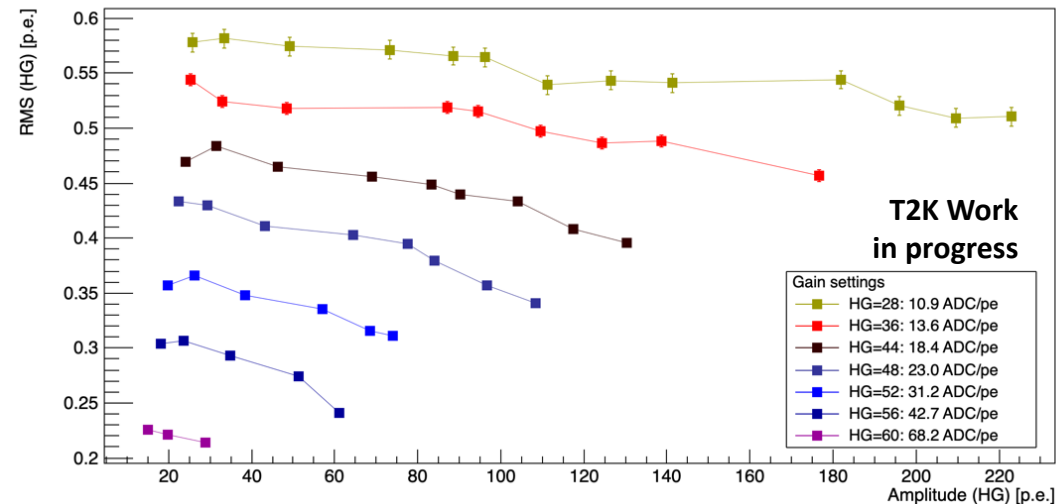
Energy resolution (HG output)

Electronic noise degrades energy resolution.

Study RMS of the signal in HG mode.

RMS < 1 p.e.

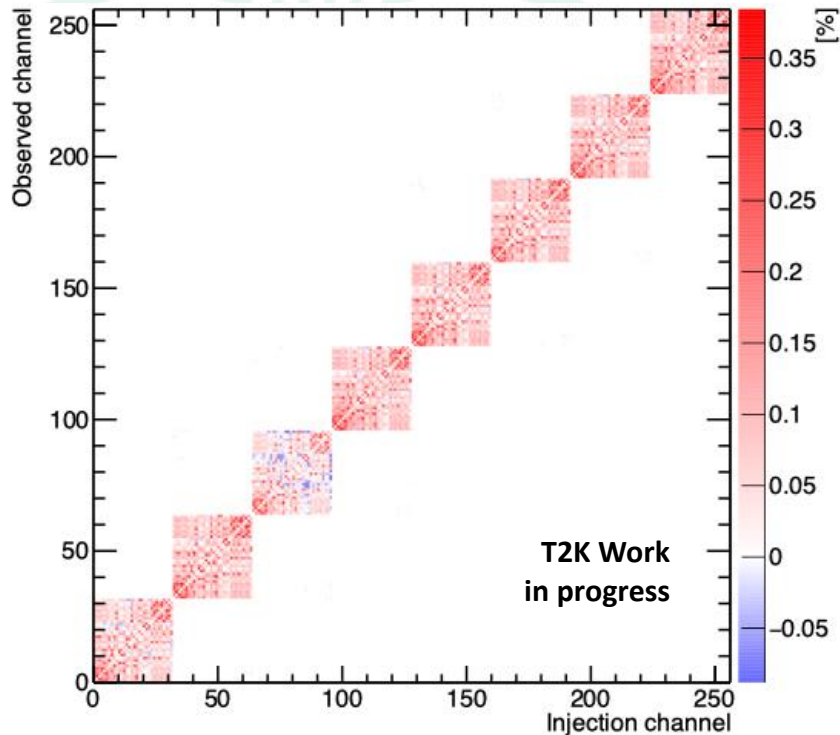
RMS vs Amplitude (FEB ch 0) in the linearity regime



Electronics cross talk:

< 0.5 %

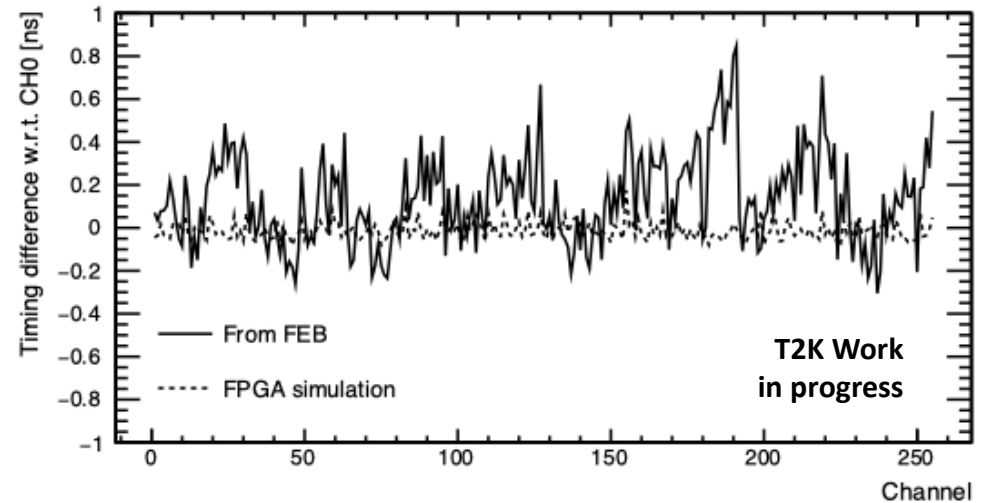
Only intra-ROC



Channel-by-channel timing delays:

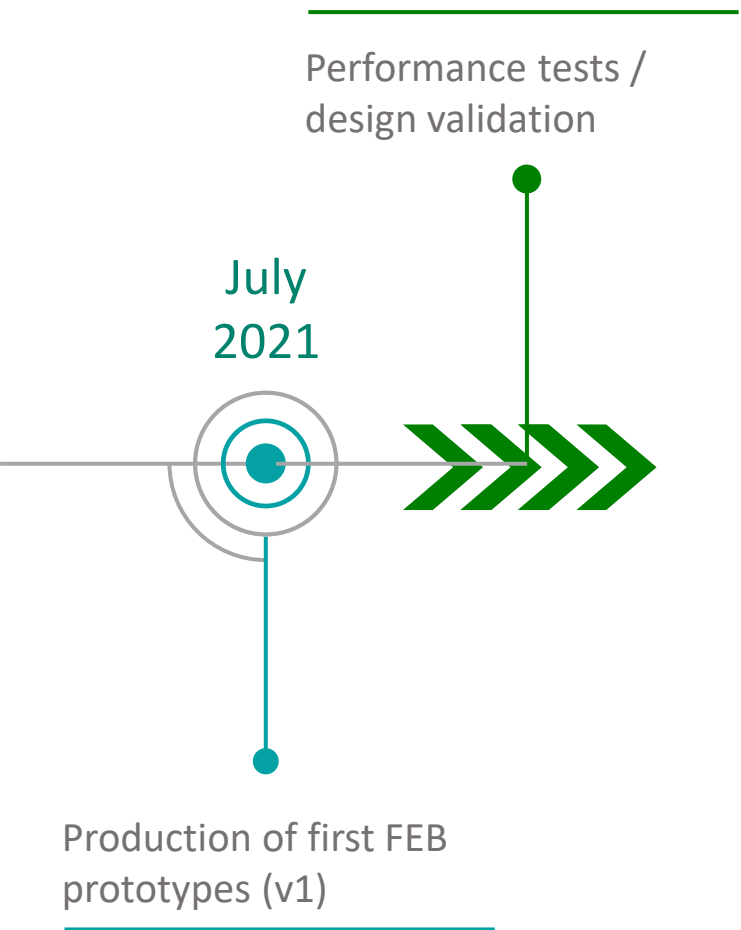
~ 1 ns

→ Need time calibration or FPGA programmable delay

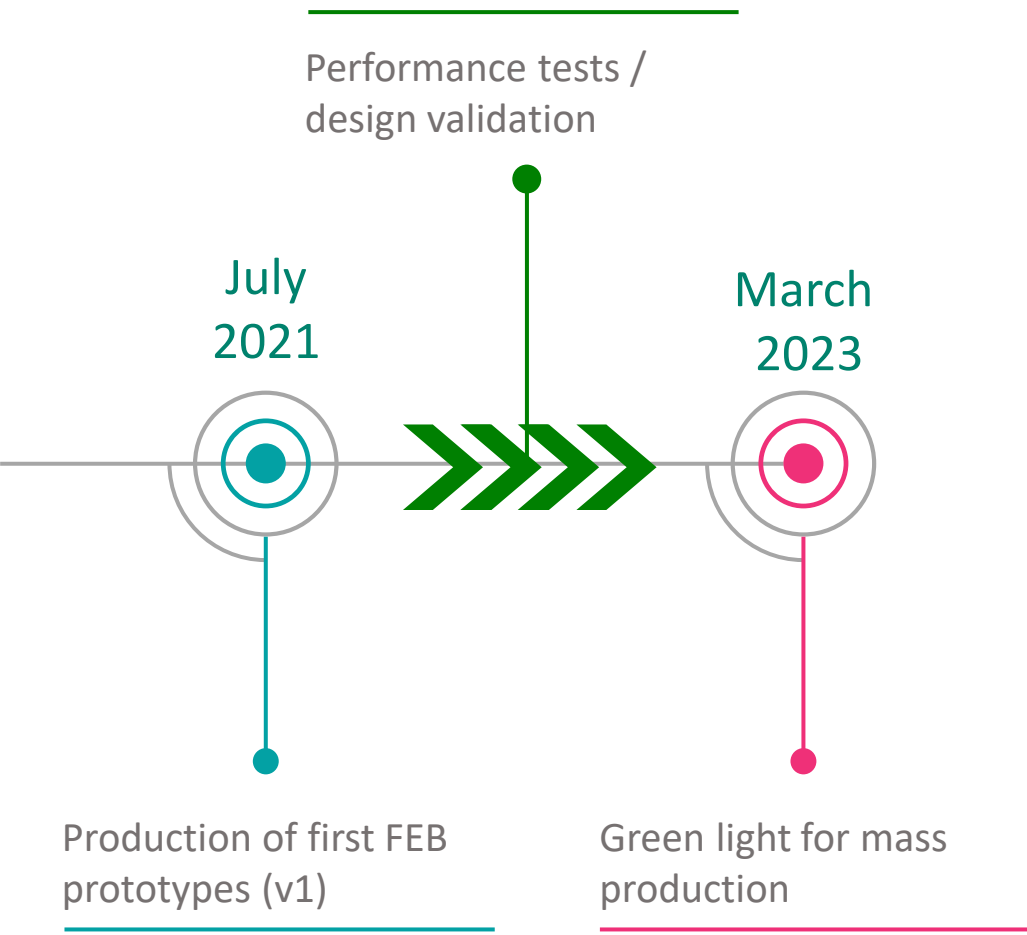


Work by J.Chakrani

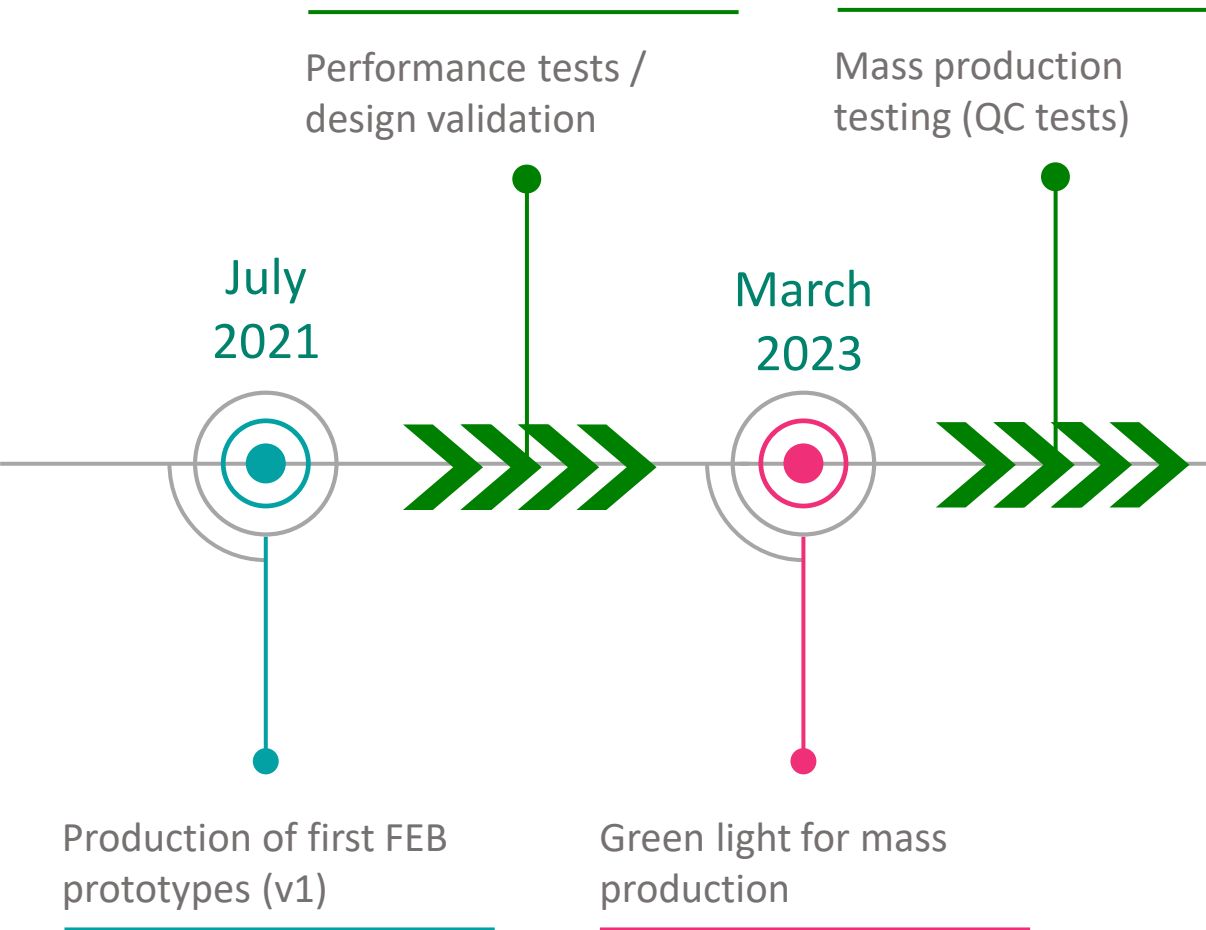
History of the Super-FGD FEBs



History of the Super-FGD FEBs



History of the Super-FGD FEBs



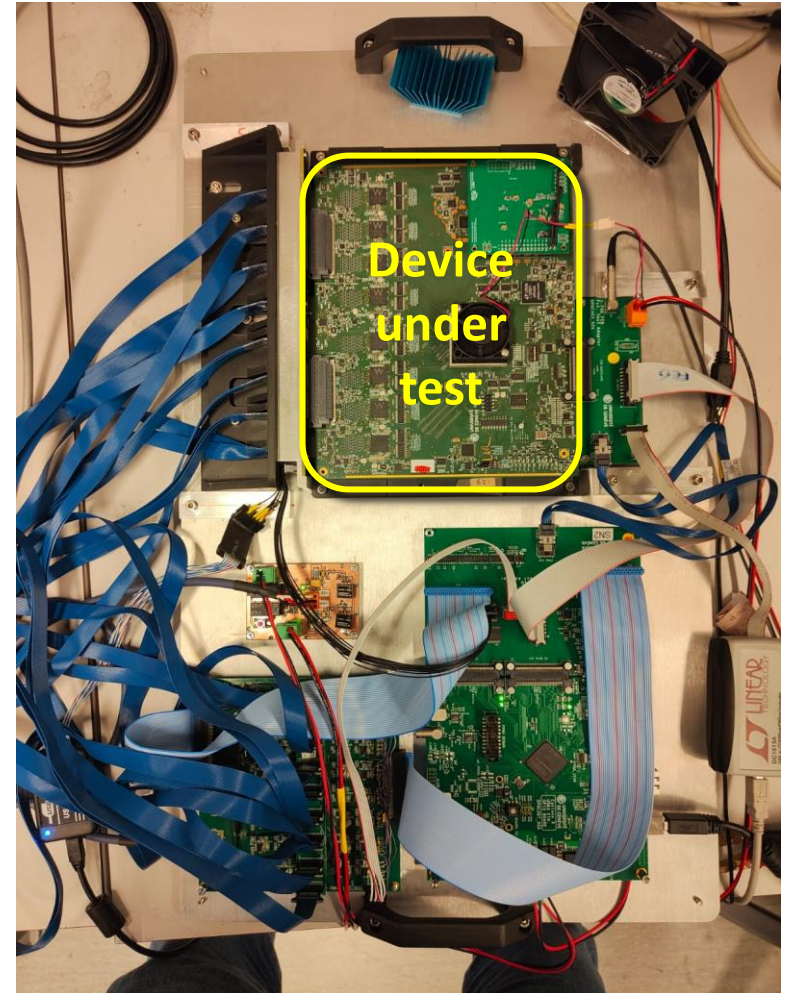
4. Mass production testing

Hardware quality check for the FEB mass production

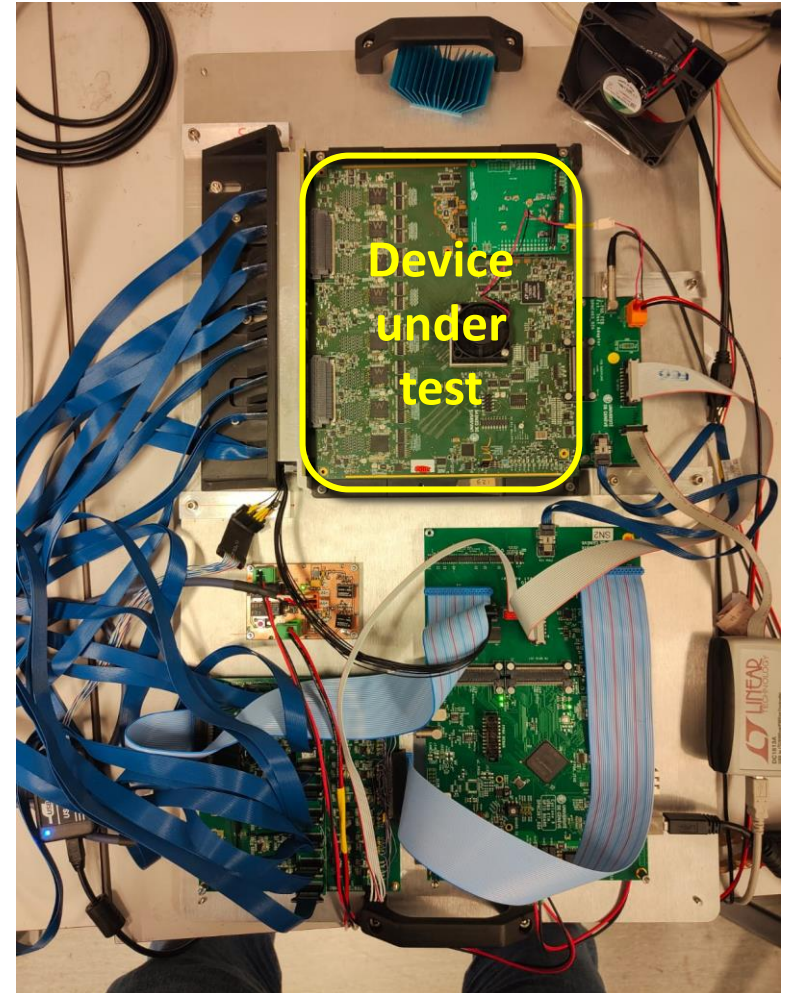
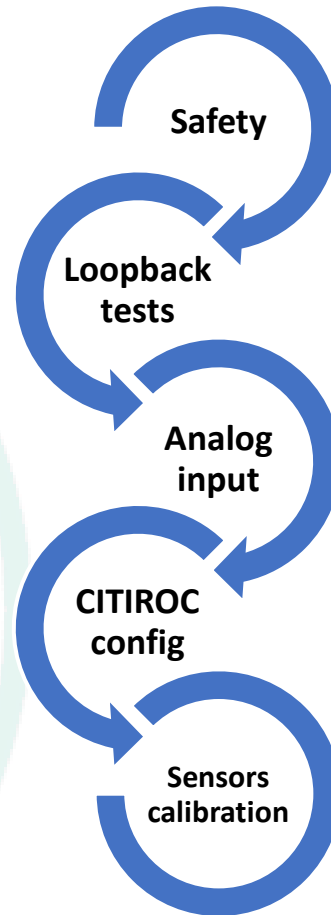
Mass production: 240 FEBs -> serial hardware testing

Challenge: need to speed up the testing (and repairing!) process.

Solution: custom QC test bench with “*symptom* → *HW issue*” diagnostic.

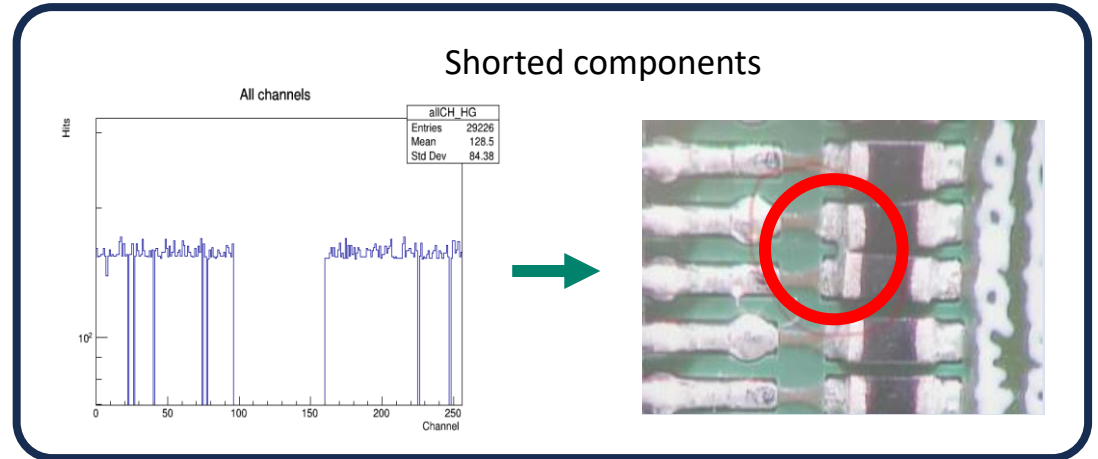
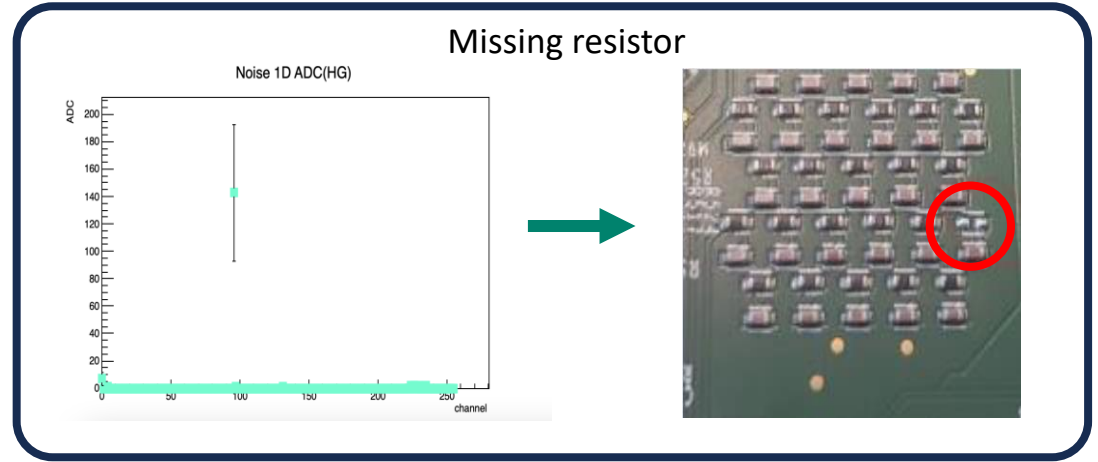


- Table-top setup, **6 minutes**
- **99%** hardware coverage:
 - ❖ Analog traces
 - ❖ Sync, clk, trigger, busy
 - ❖ CITIROC configuration, S/C
 - ❖ HV/T sensors + calibration
- Custom auxiliary board
- **Flexible:** edit software to test specific hardware problems
- **Locate** HW problems

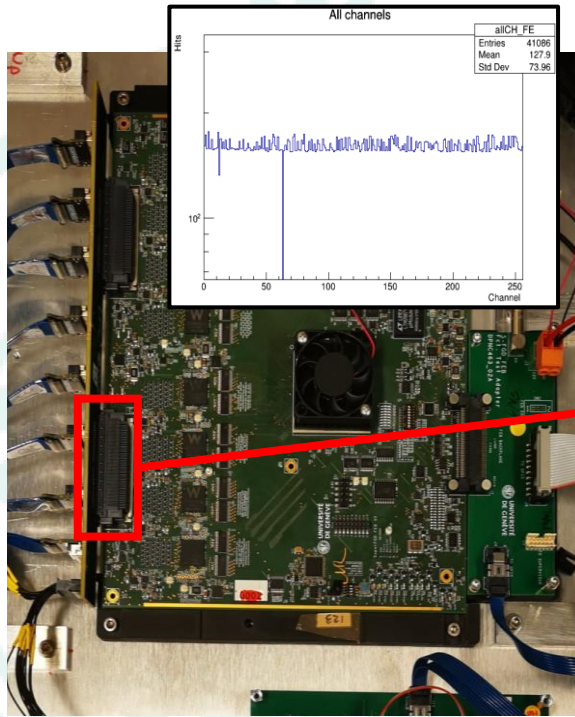


Some problems are easy to understand and fix

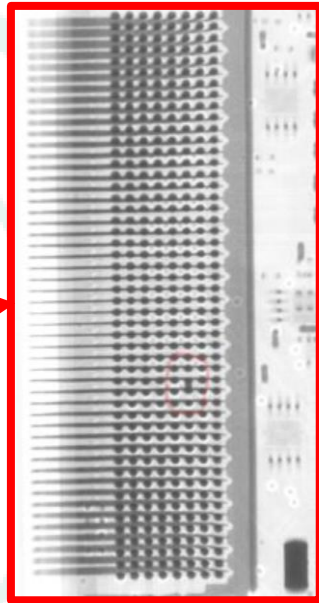
- Bad/cold soldering
- Missing/wrong passive component
- Shorts on surface components



Short circuit in connector



X-ray



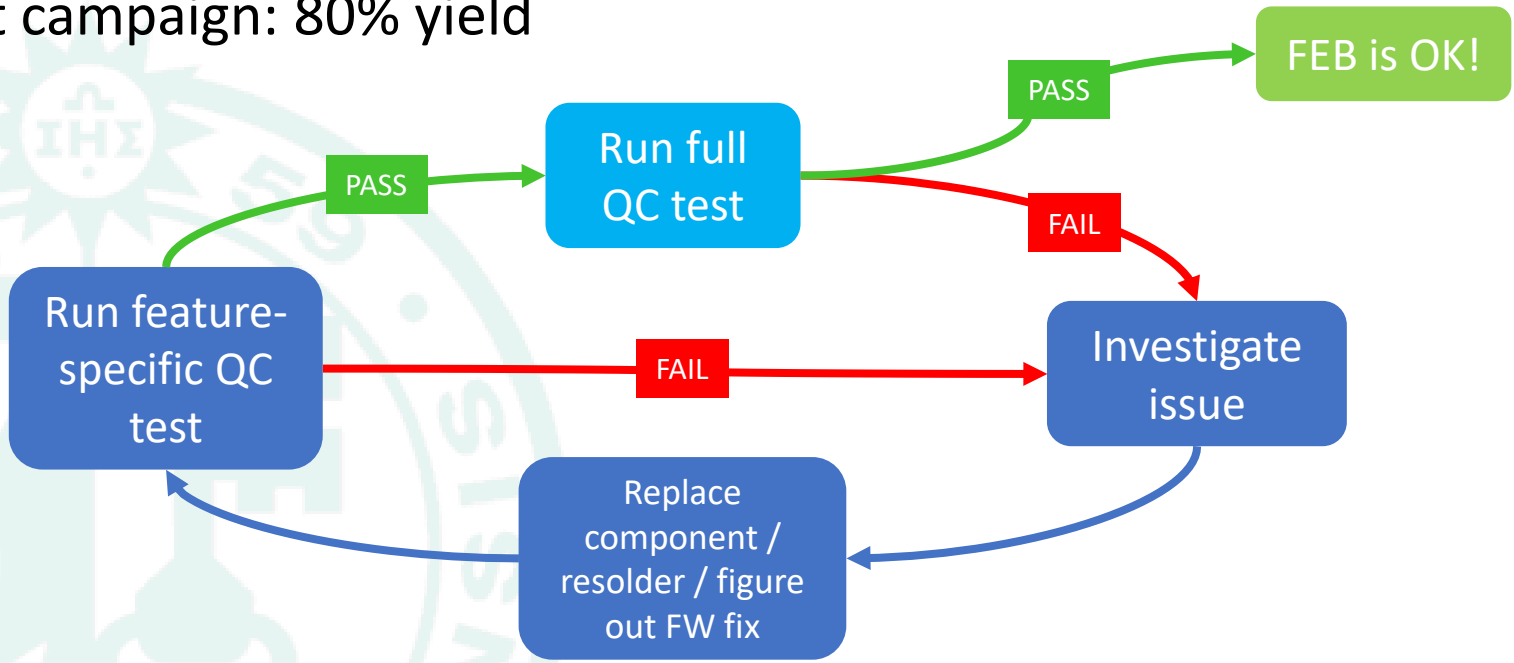
Others can be nasty...

- Shorts under connectors
- Cold-soldered BGA
- CITIROC to be replaced
- Bad PCB routing

Ship back to manufacturer:
major delay

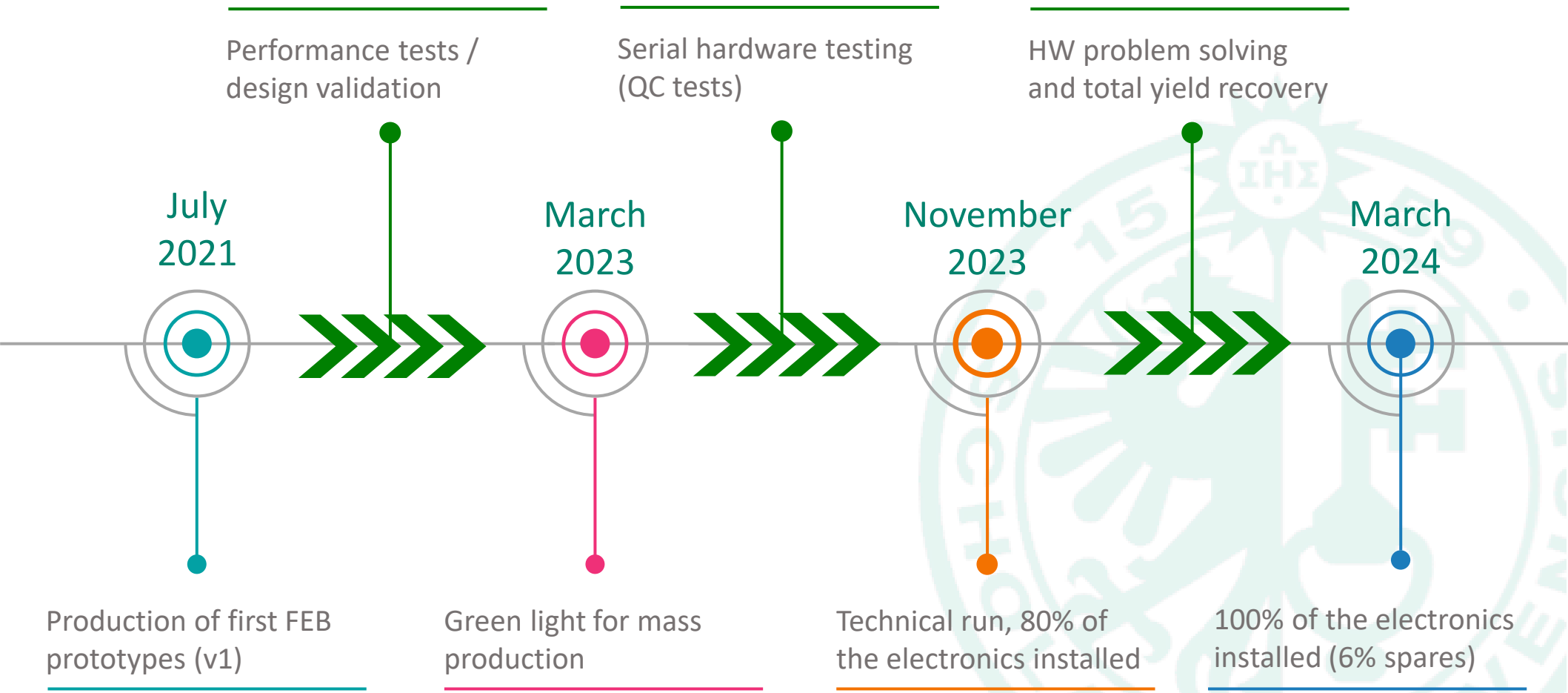
Initial plan: 222 FEBs installed + 10% spares

First QC test campaign: 80% yield

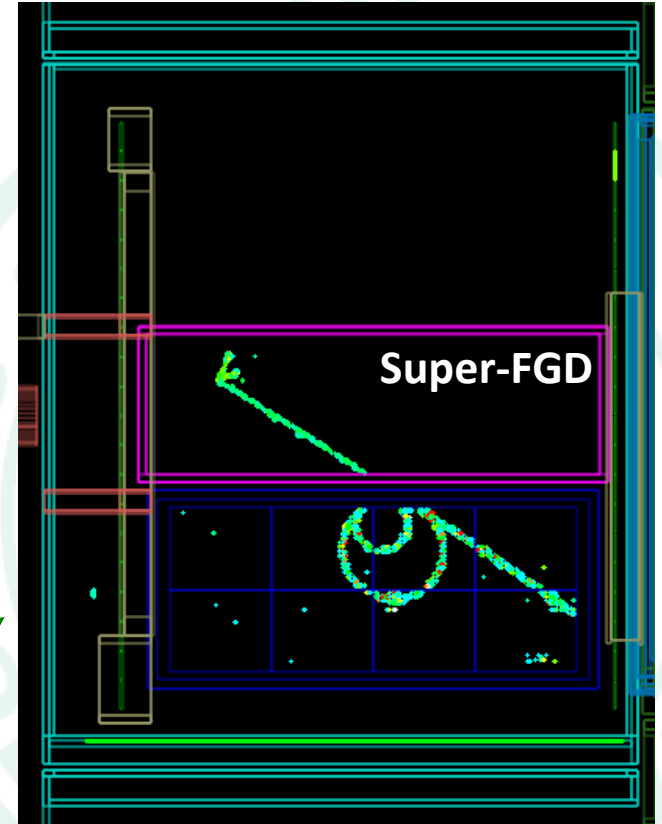
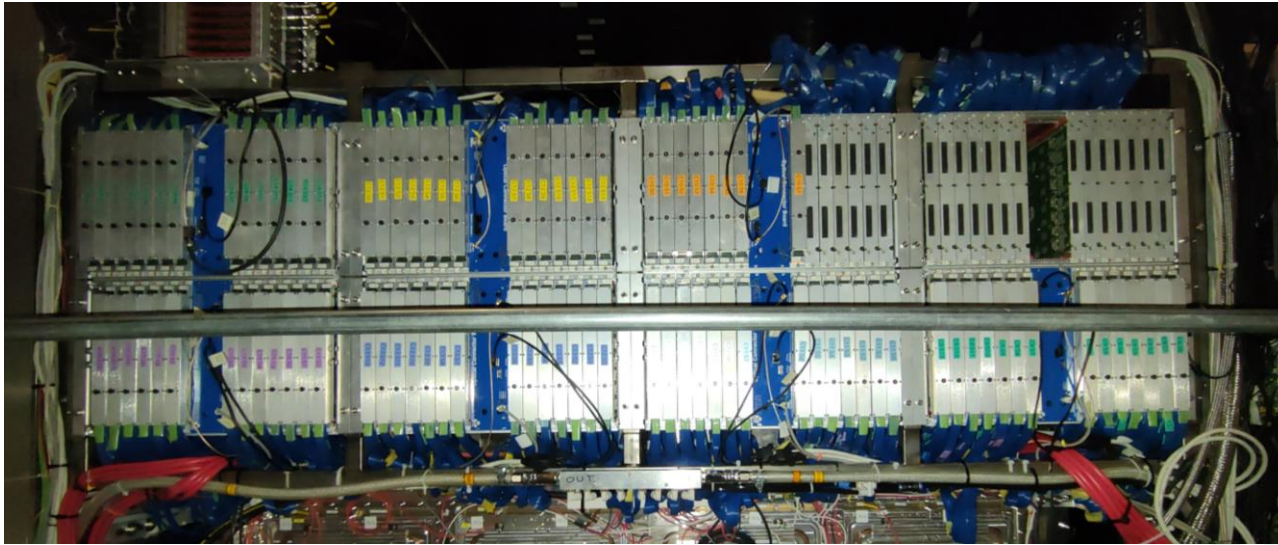


Take-home message: A custom, versatile QC setup is more work, but ends up saving time and resources.

History of the Super-FGD FEBs



- FEBs for the Super-FGD performances validated and 240 FEBs successfully tested (repaired) and installed
 - ❖ Custom, table-top QC test bench proven to be essential



First neutrino beam run of T2K phase II (June 2024)

Back up



The T2K Experiment

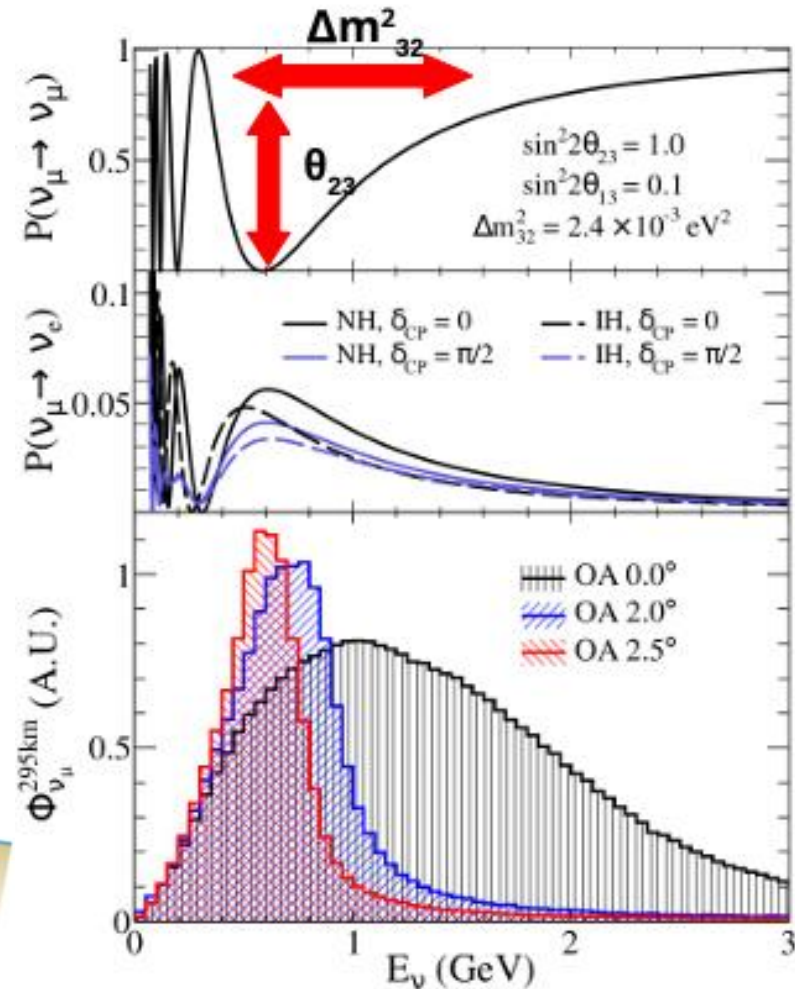
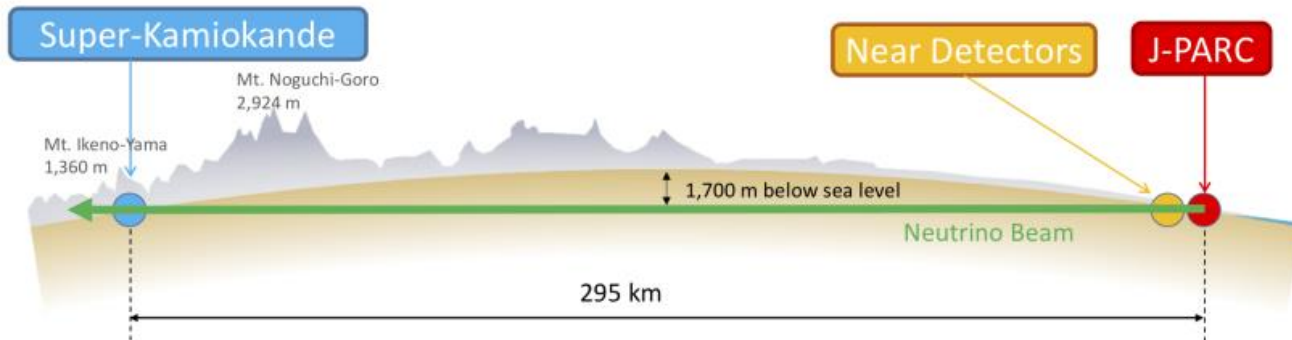
T2K is a **long baseline neutrino oscillation experiment**

Sensitive to δ_{CP} through **electron (anti-) neutrino disappearance**

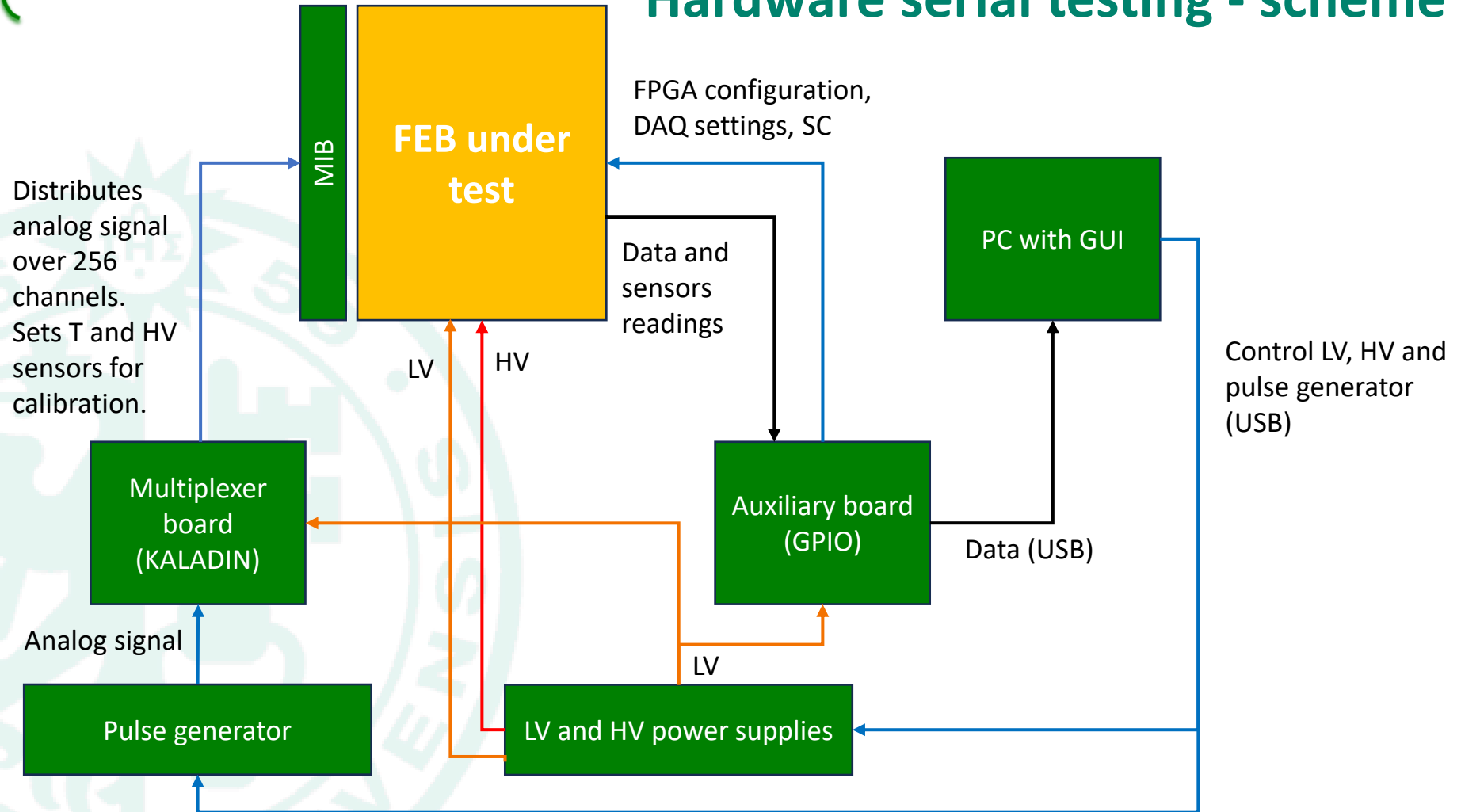
Sensitive to Δm^2_{32} and θ_{23} through **muon (anti-) neutrino appearance**

➤ Near detector is being upgraded with 3 new subdetectors (Super-FGD, High-angle TPCs, TOF)

❖ Super-FGD: new neutrino active target



Hardware serial testing - scheme



➤ Safety:

Test HV current limiter circuit

➤ Slow control

Test slow control lines (FPGA to backplane, FPGA to CITIROC,) with loopback circuits (FPGA driven)

➤ Analog input

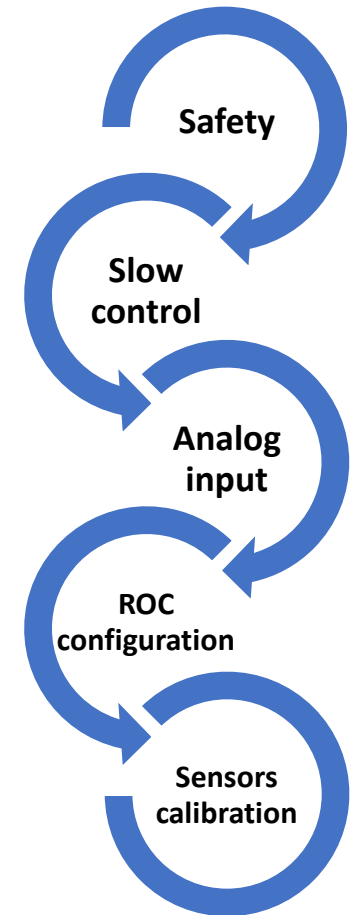
Test all channels against open/short circuits. Check ADC output validity range. Evaluate noise and baseline – extensive use of Kaladin board

➤ ROC configuration

Check that the FPGA is able to configure the CITIROCs with different trigger configurations (ability to control the CITIROC programmable devices)

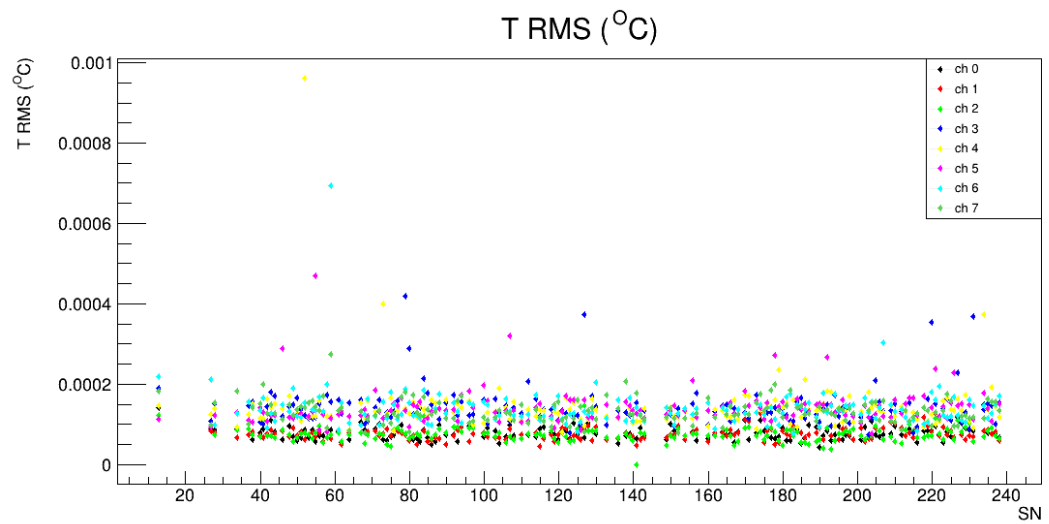
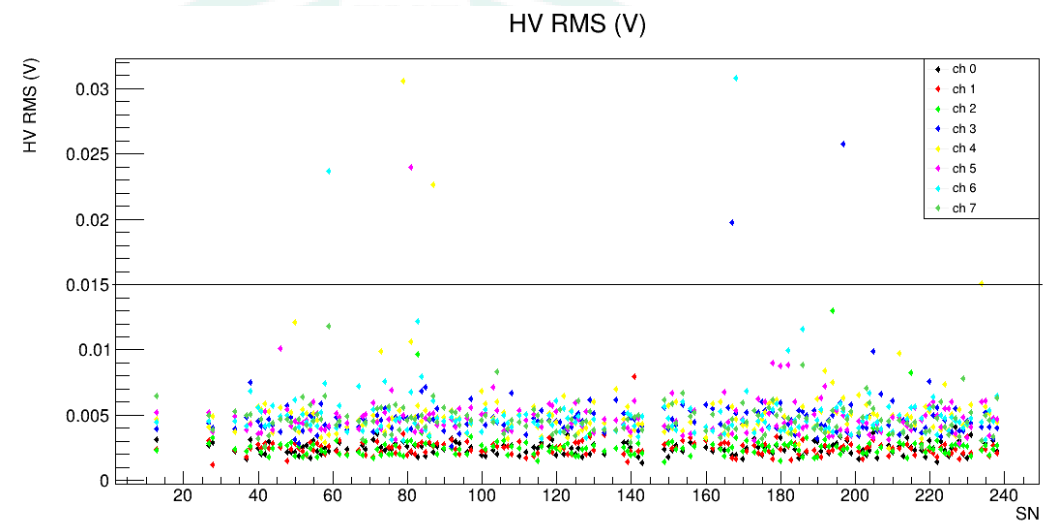
➤ Sensors calibration

Calibrate the HV and T sensors and check that the calibration constants are stored in the EEPROM. Measure RMS (RC filter test)



Global results on T/HV sensors precision [gain equalization]

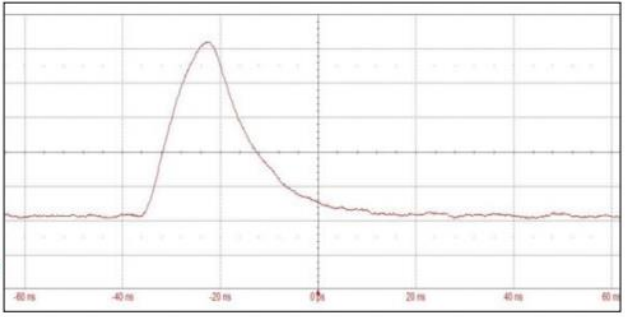
➤ RMS values of the T and HV sensors to evaluate overall performances



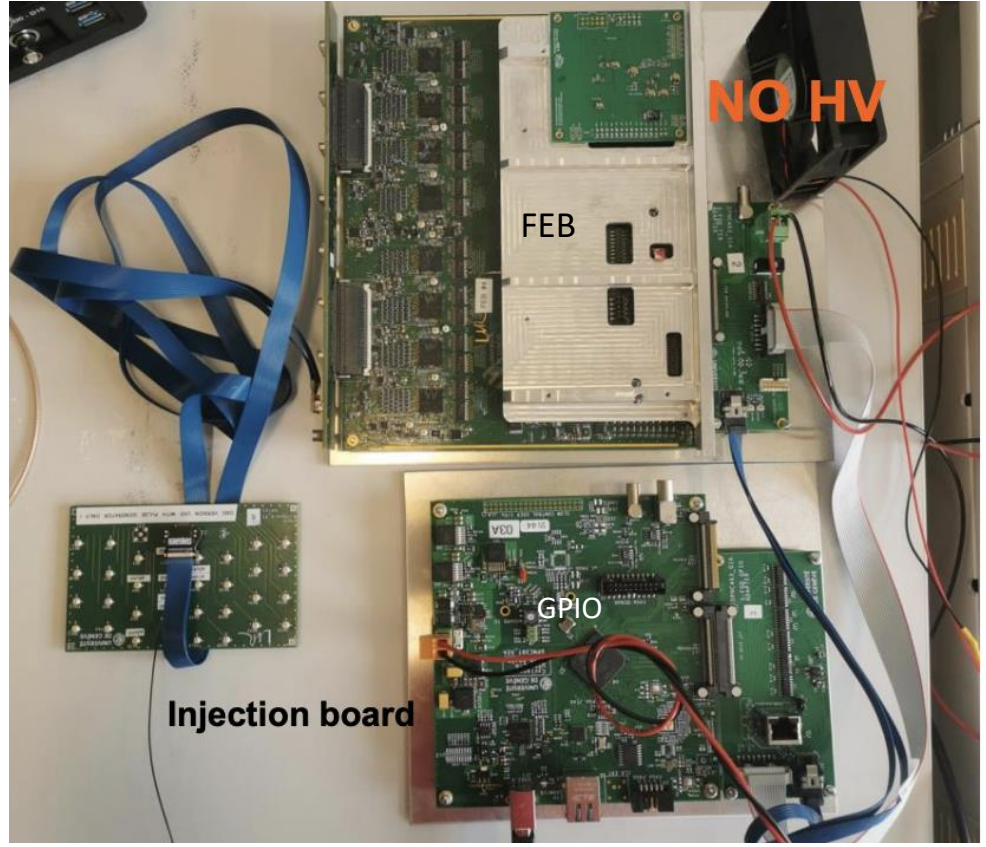
Gain equalization:
 $55\text{mV}/^\circ\text{C}$ HV gain change in MPPC sets requirement on RMS(V)

Linearity range & resolution - setup

Pulse generator + RC filter



To FEB



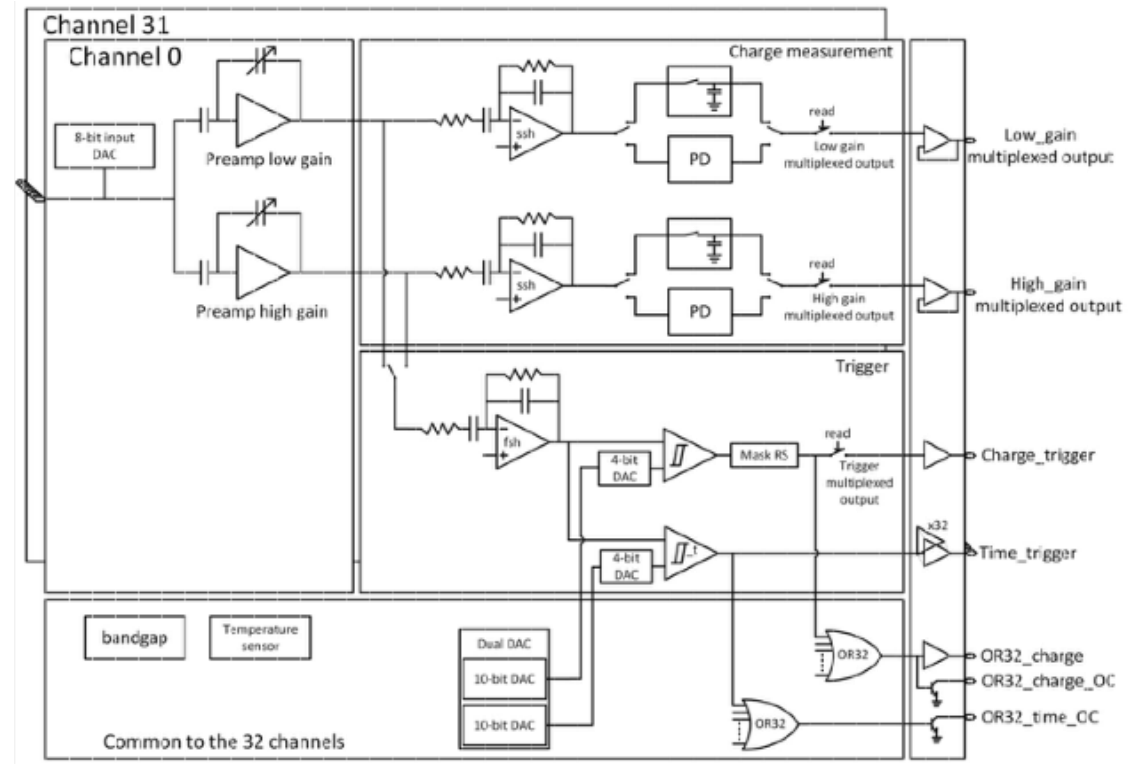
➤ 32 channels

Types of read-out:

- Timing: constant threshold trigger output
- Charge: dual gain with peak detector (HG, LG)

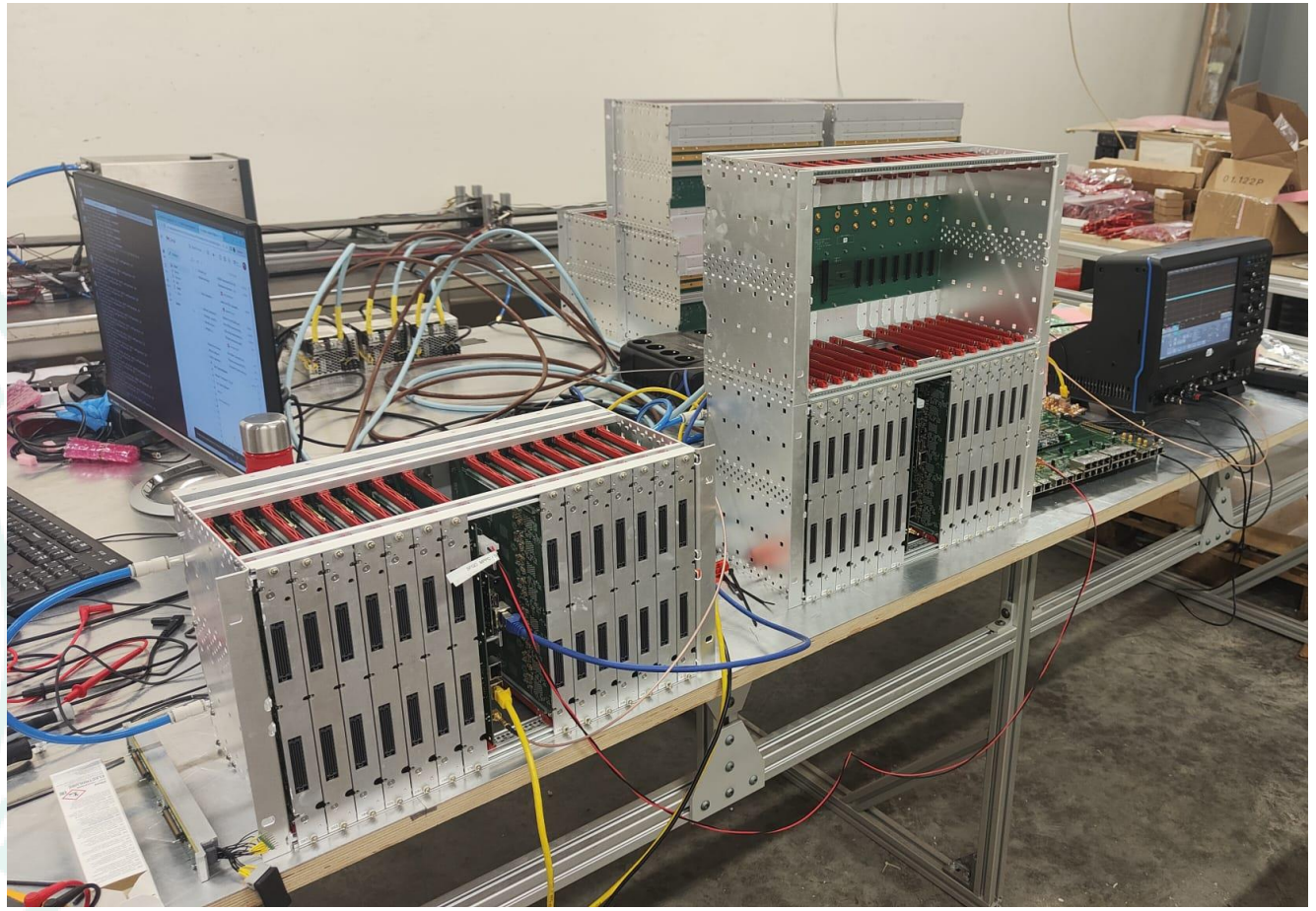
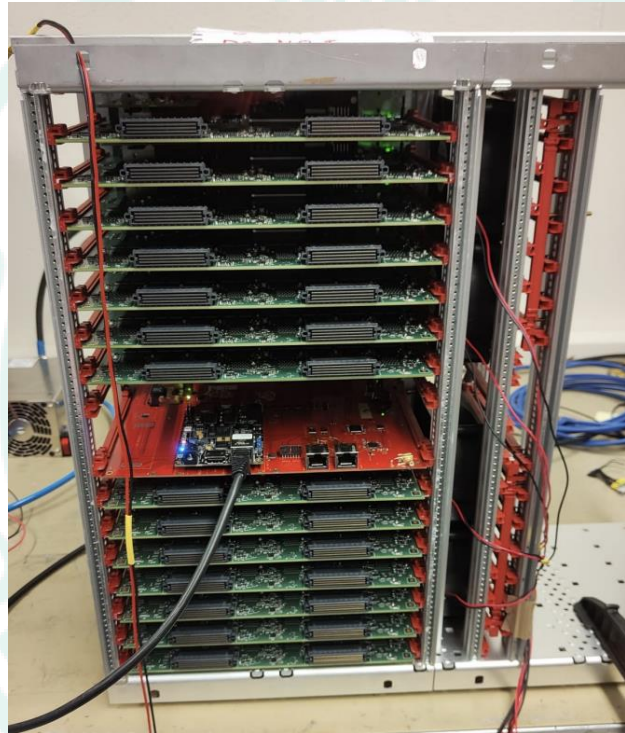
Programmable devices:

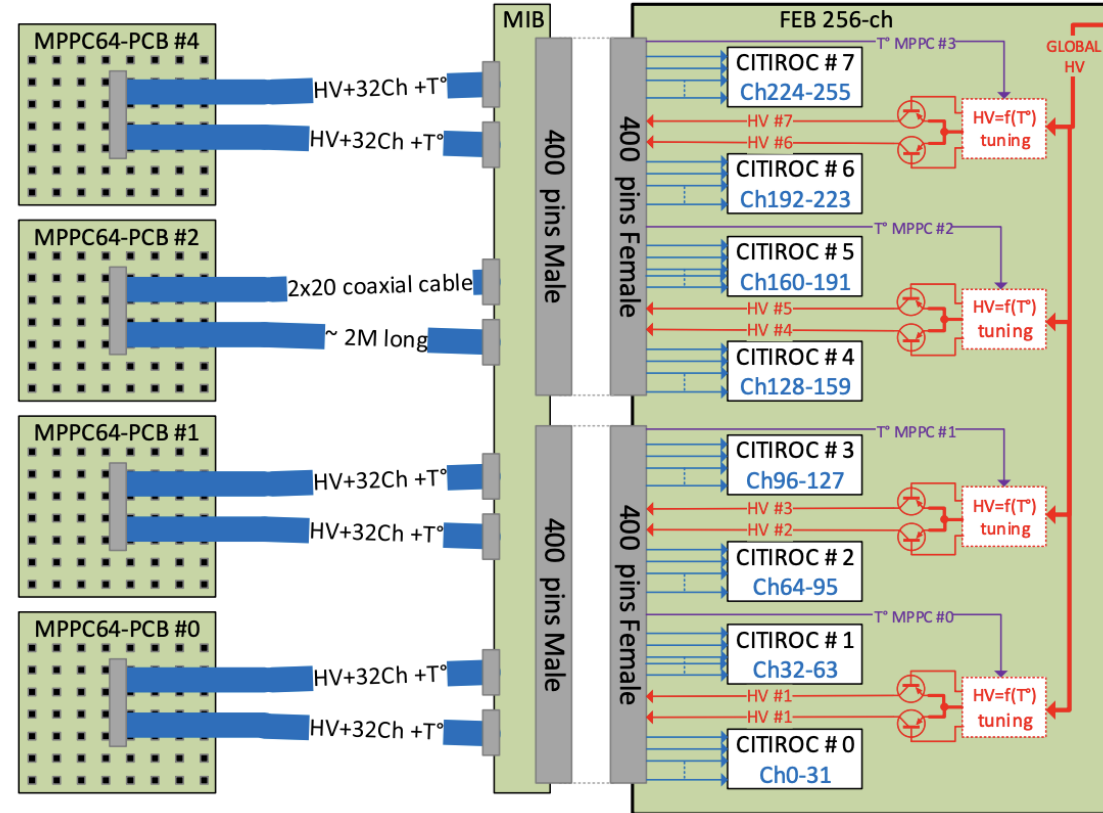
- Timing and analog thresholds: 10(+4)-bit
- Input DAC for MPPC voltage tuning: 8-bit
- Gain for charge readout: 6-bit
- Shaping time: 3-bit



[1] add CITIROC reference here

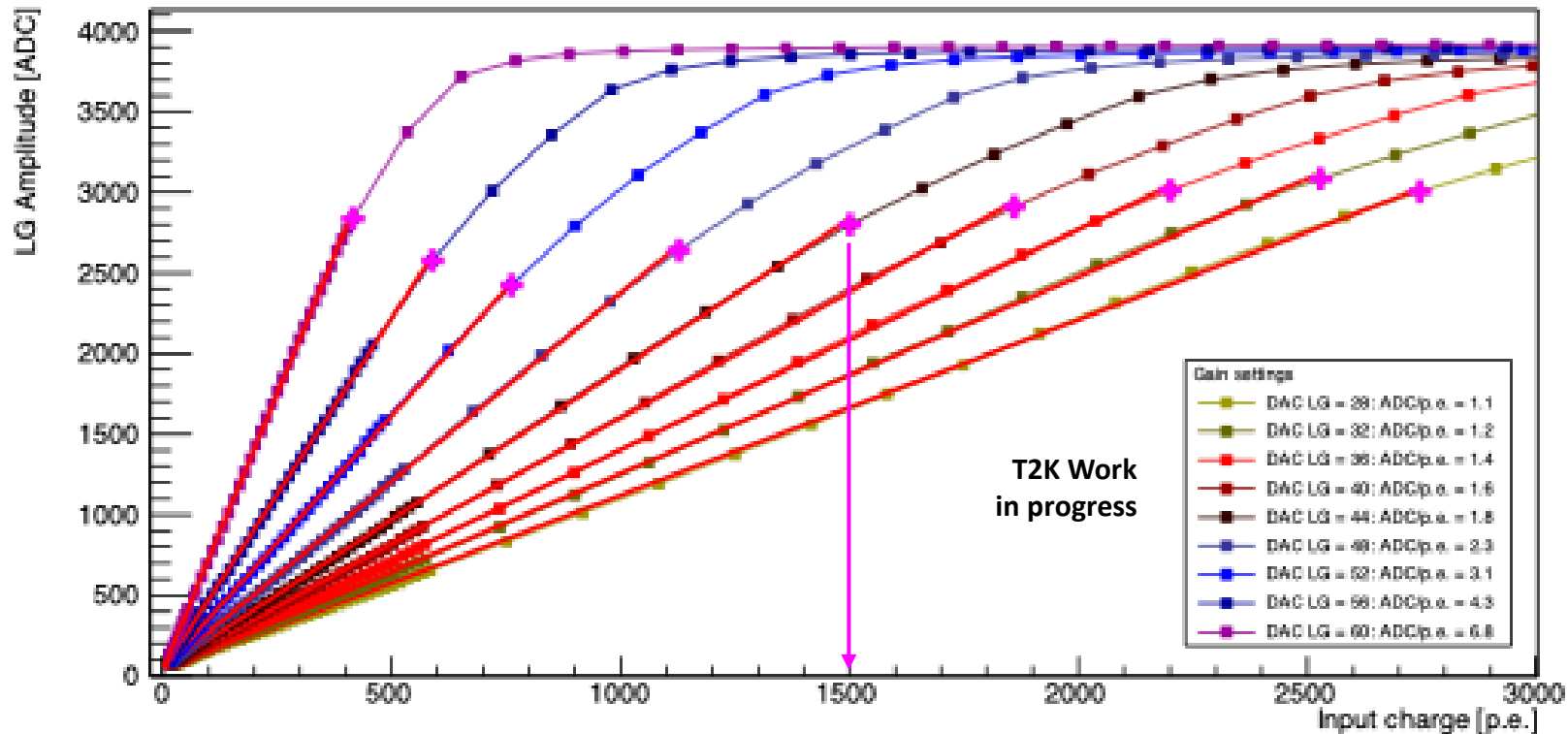
- Full crate “burning test”
- BER tests (OCB-FEB)
- OCB-FEB communication
- MCB-OCB communication
- DAQ stability tests





Dynamic range

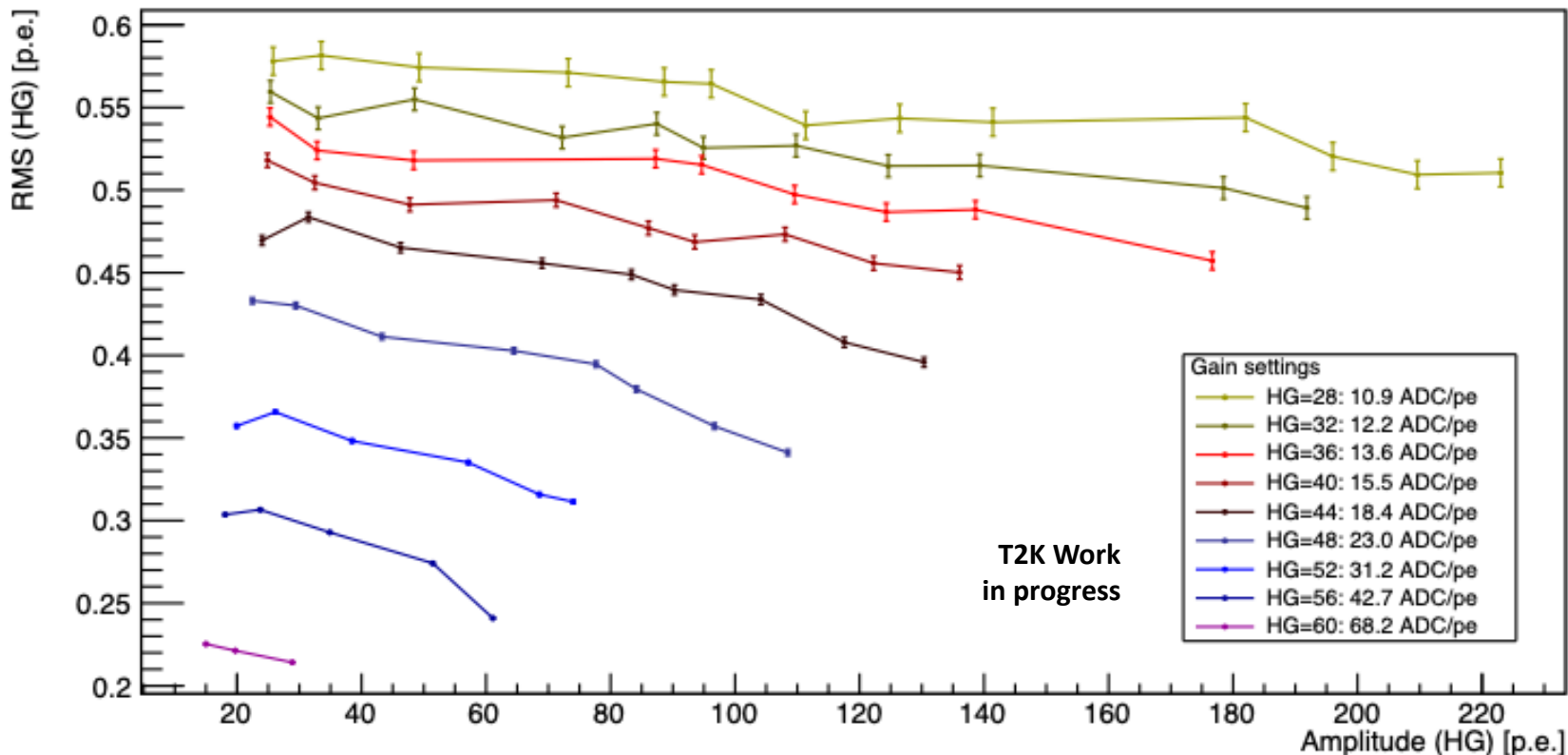
FEB low-gain signal response (ch 0)



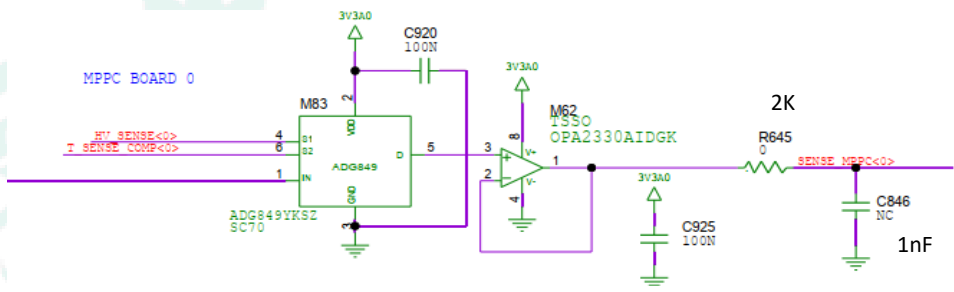
T2K Work
in progress

Energy resolution (HG output)

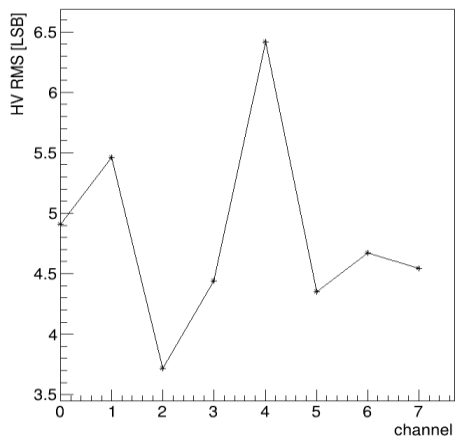
RMS vs Amplitude (FEB ch 0) in the linearity regime



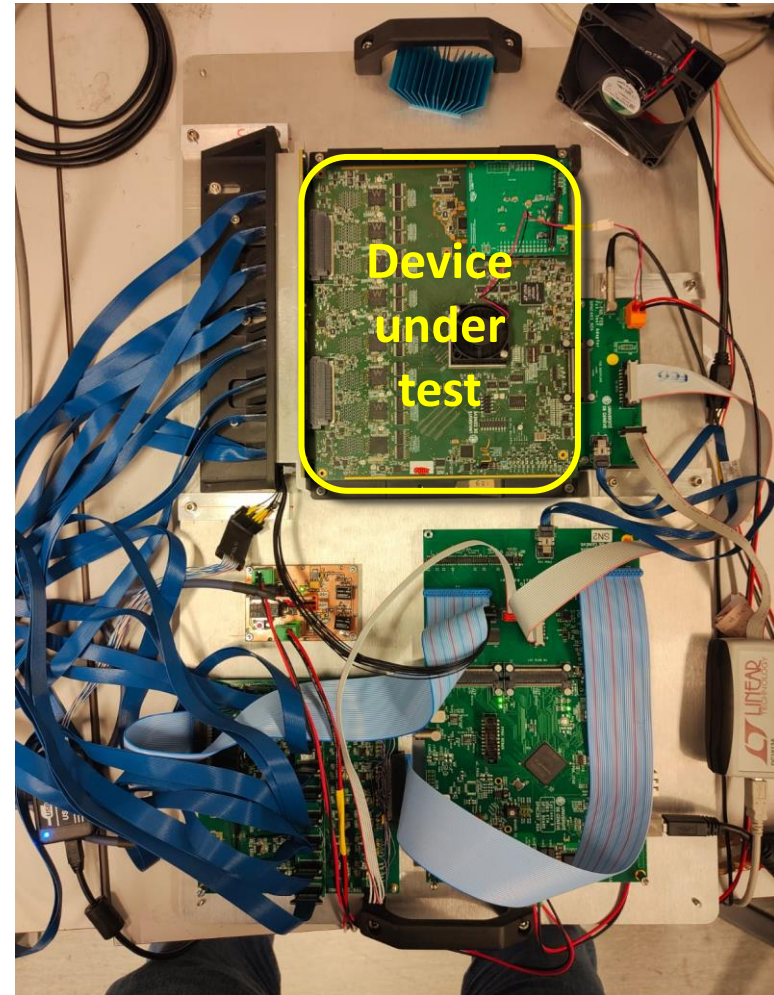
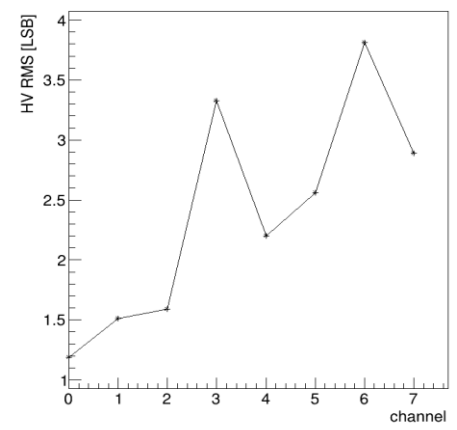
- Calibration of HV and NTC sensors
 - ❖ Check passive components



HV RMS **fail**



HV RMS **pass**



➤ We want to make sure that the resistor in the current limiter circuit is 150KΩ.

❖ $|V_{gs}| < 20 \text{ V}$ to not damage transistor

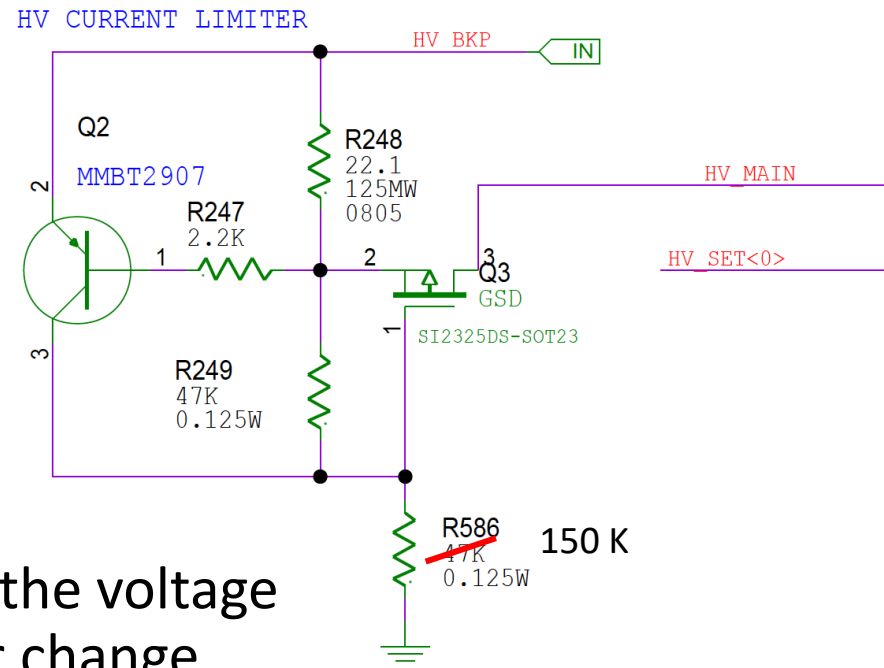
➤ The GS threshold voltage is between -2.5 and -4.5 V

➤ V_{GS} is computed as (given $R=R586$):

$$V_{GS} = V_{PS} \cdot \left(\frac{R}{(47+R+0.022)} \right) - \left(V_{PS} \cdot \frac{(47+R)}{(47+R+0.022)} \right)$$

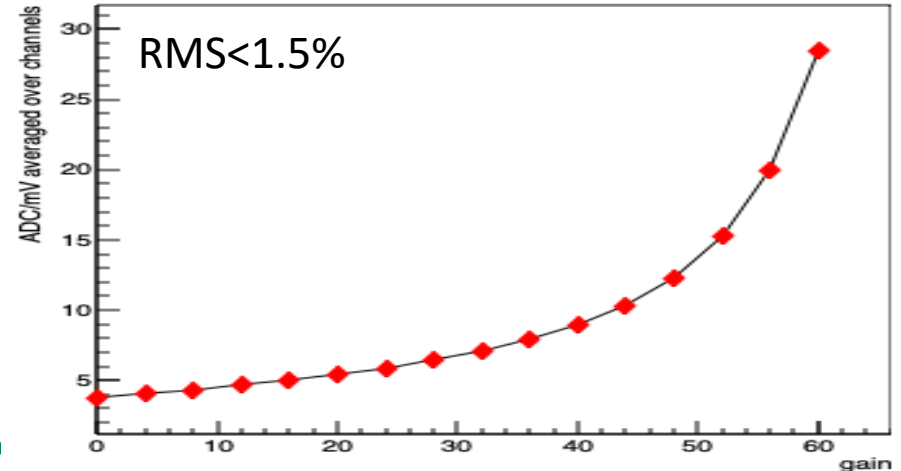
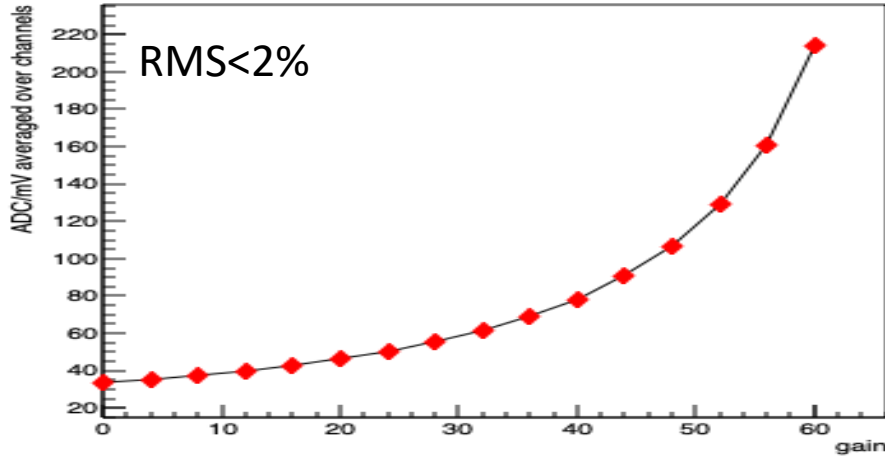
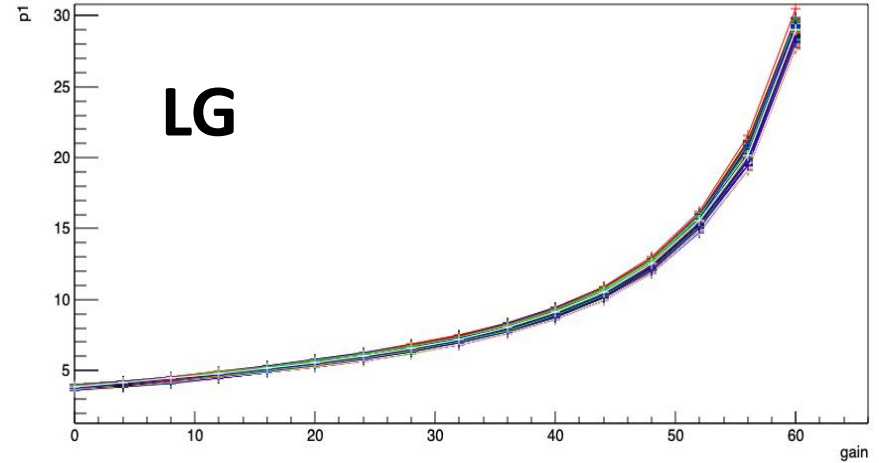
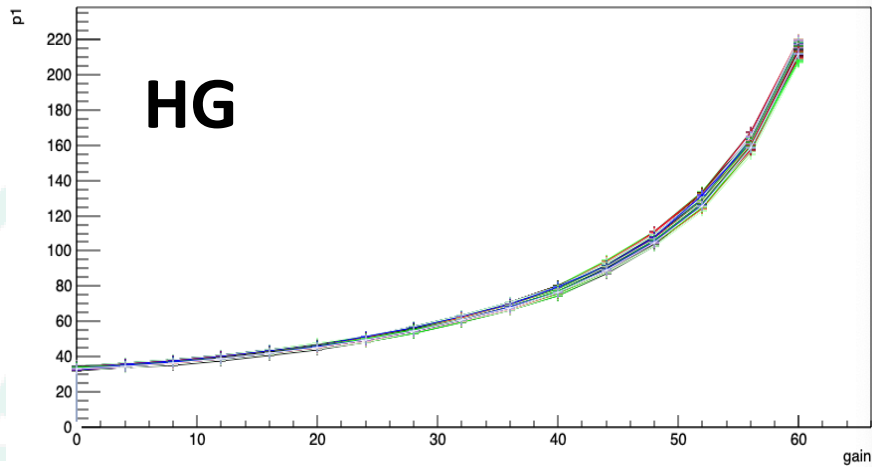
V_{PS} : voltage set on Power supply

- For the same V_{PS} , if the resistance changes, the voltage applied on the GS terminals of the transistor change.
- With higher R , the V_{PS} necessary to enable the transistor is higher

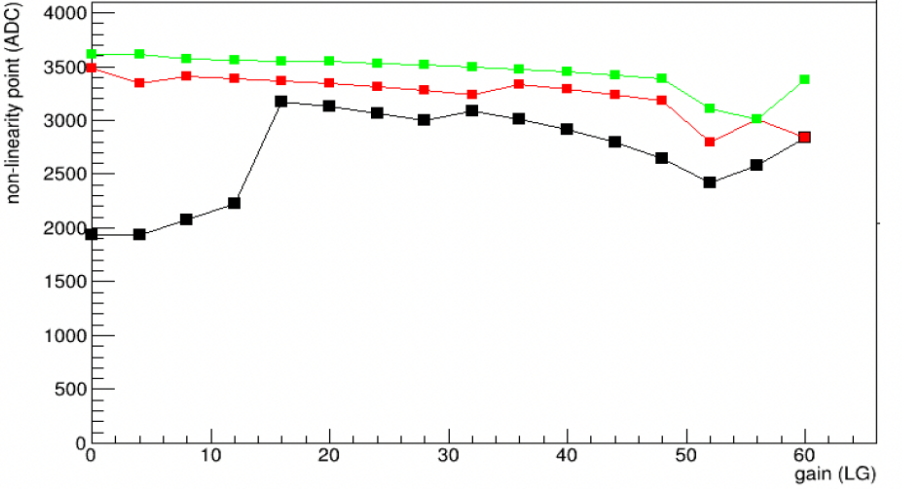
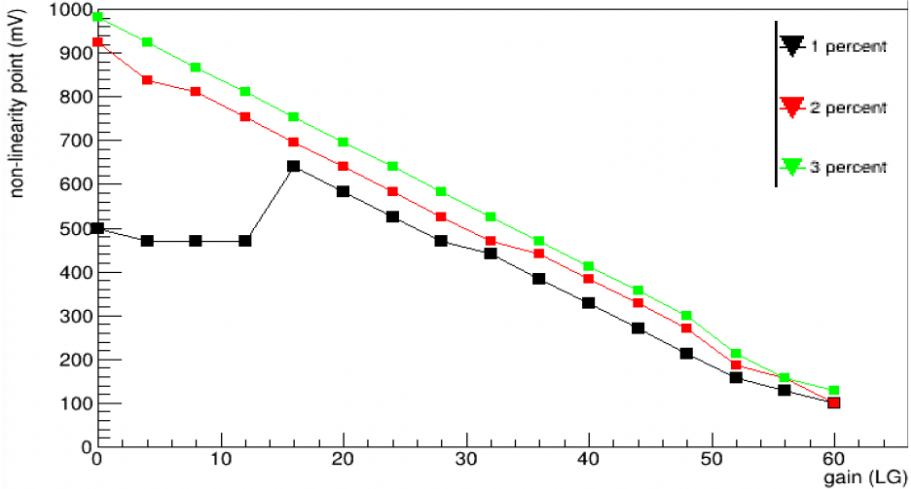
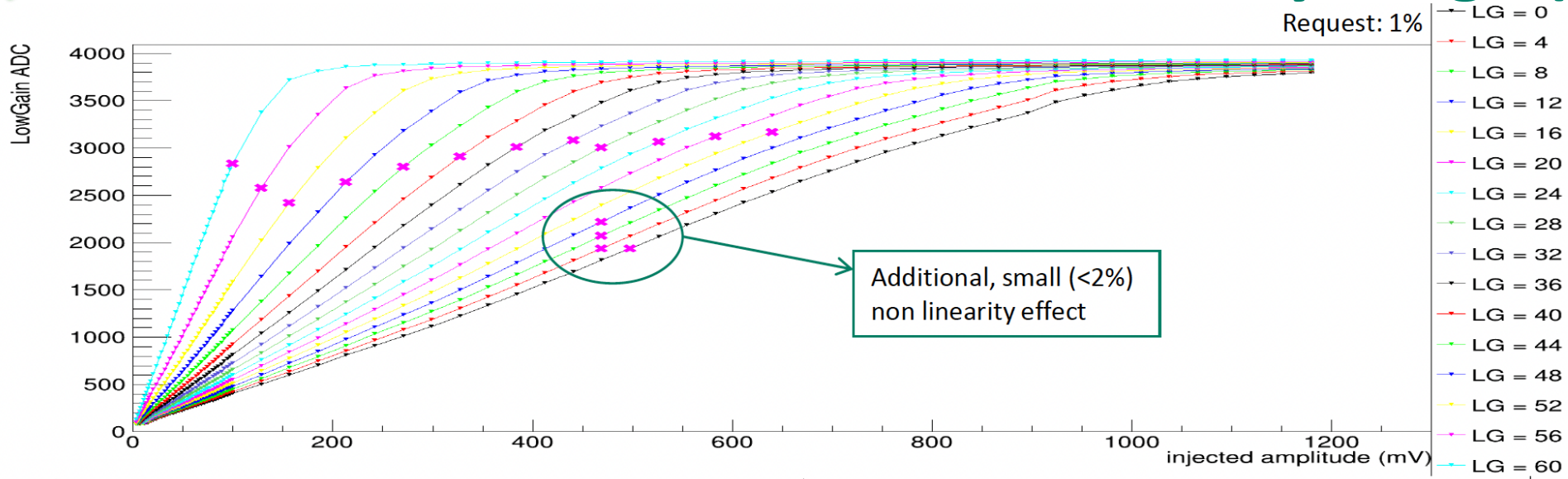


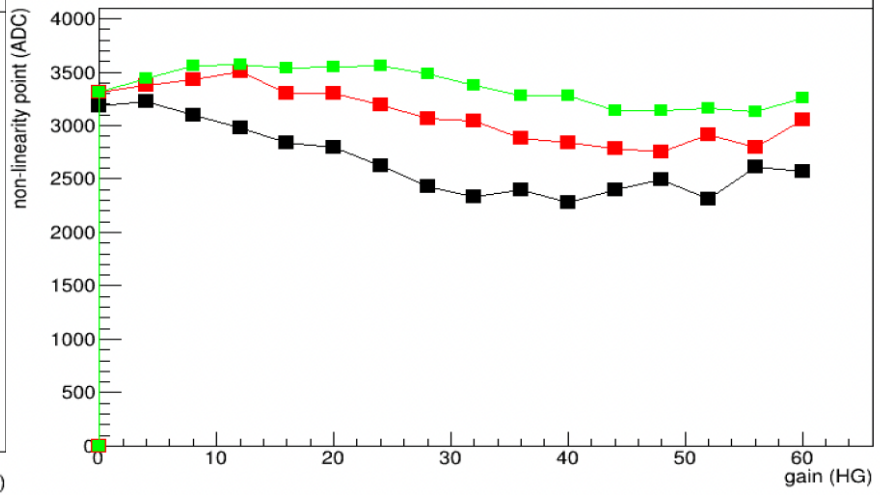
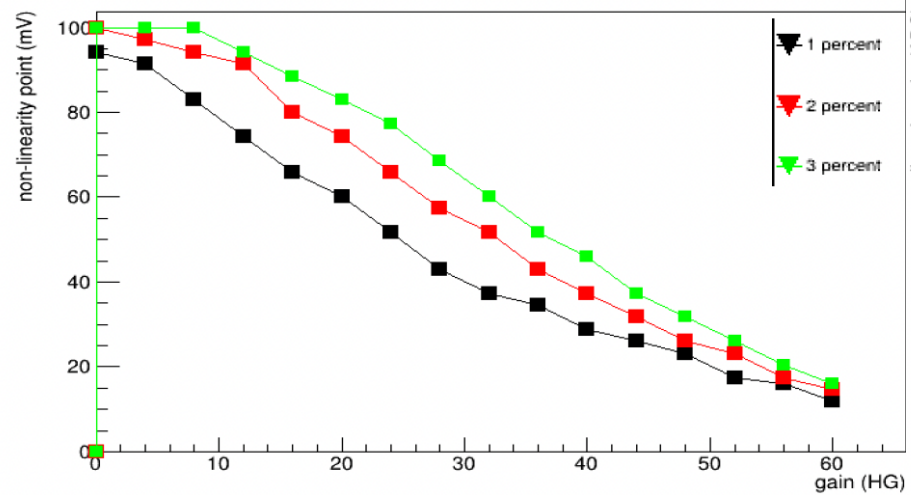
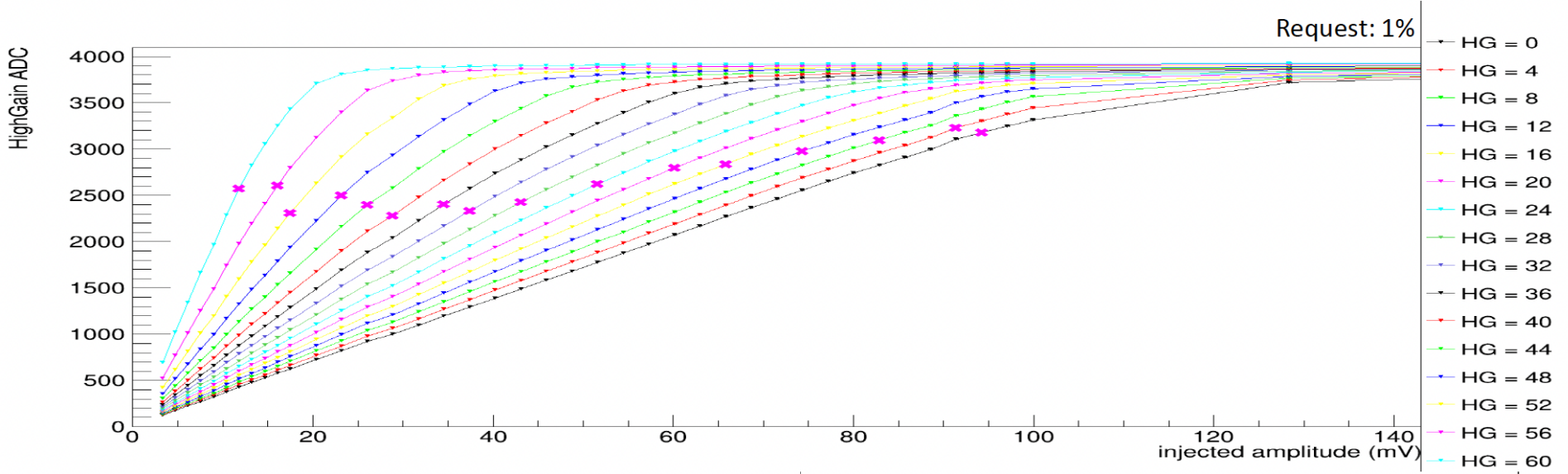
SPECIFICATIONS $T_J = 25 \text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}, I_D = -250 \text{ } \mu\text{A}$	-150			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \text{ } \mu\text{A}$	-2.5		-4.5	V

➤ Measured gain (ADC/mV) for all 256 FEB channels



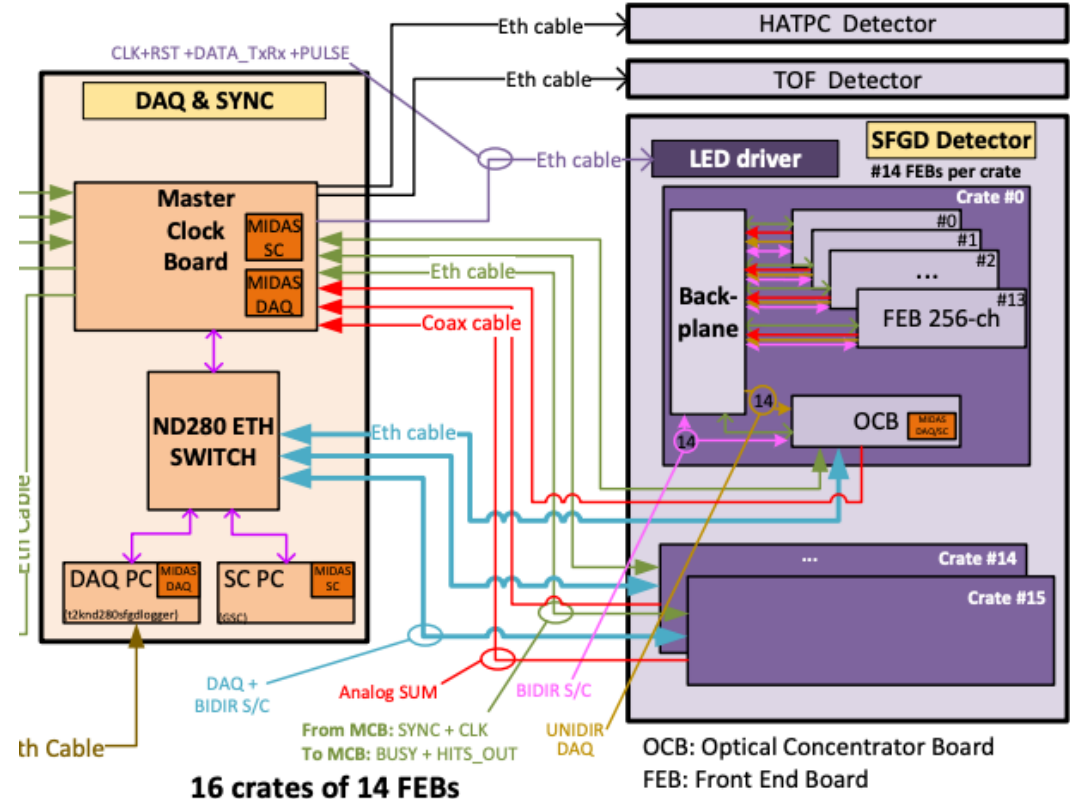
Linearity range (LG)



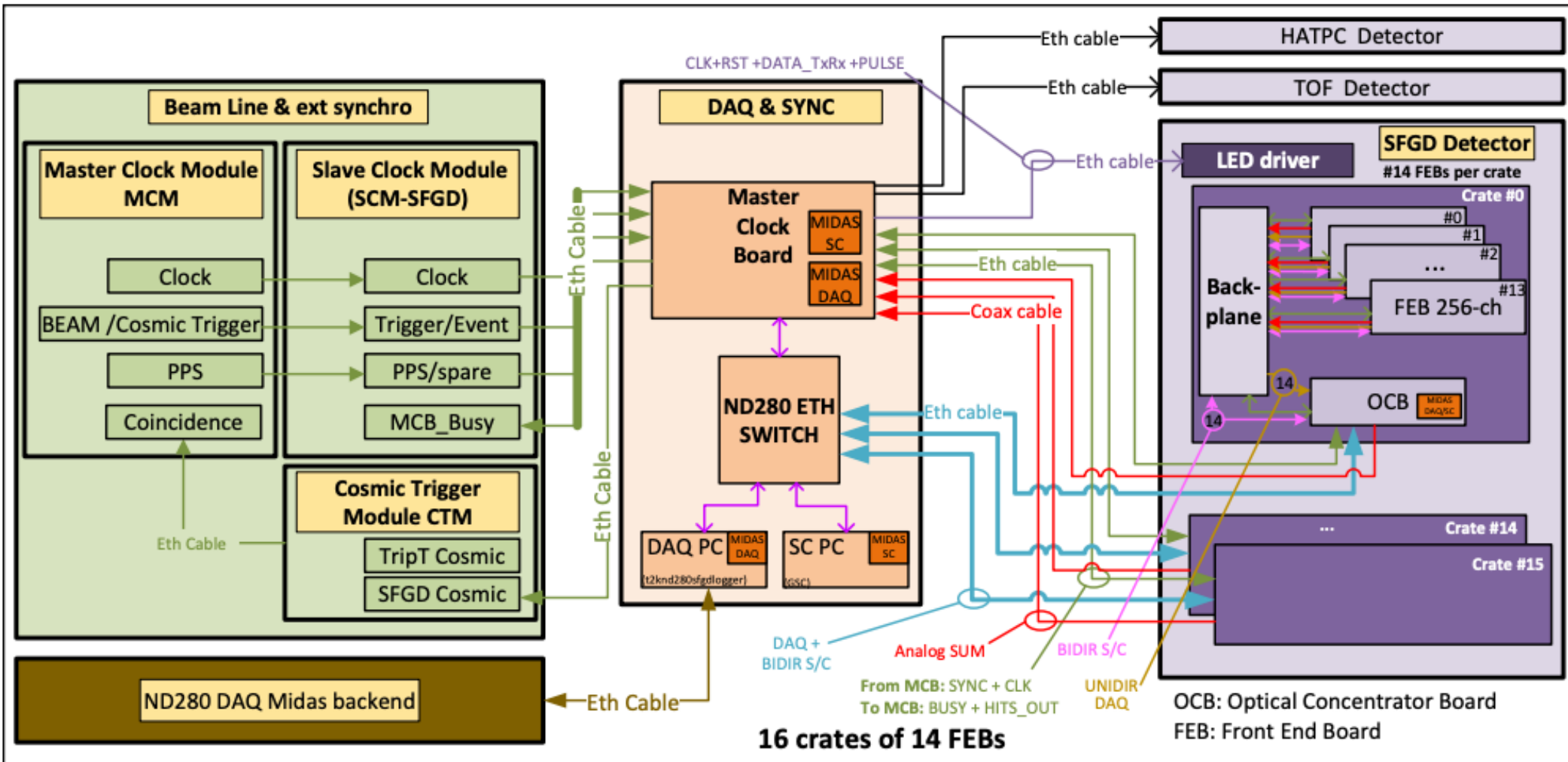


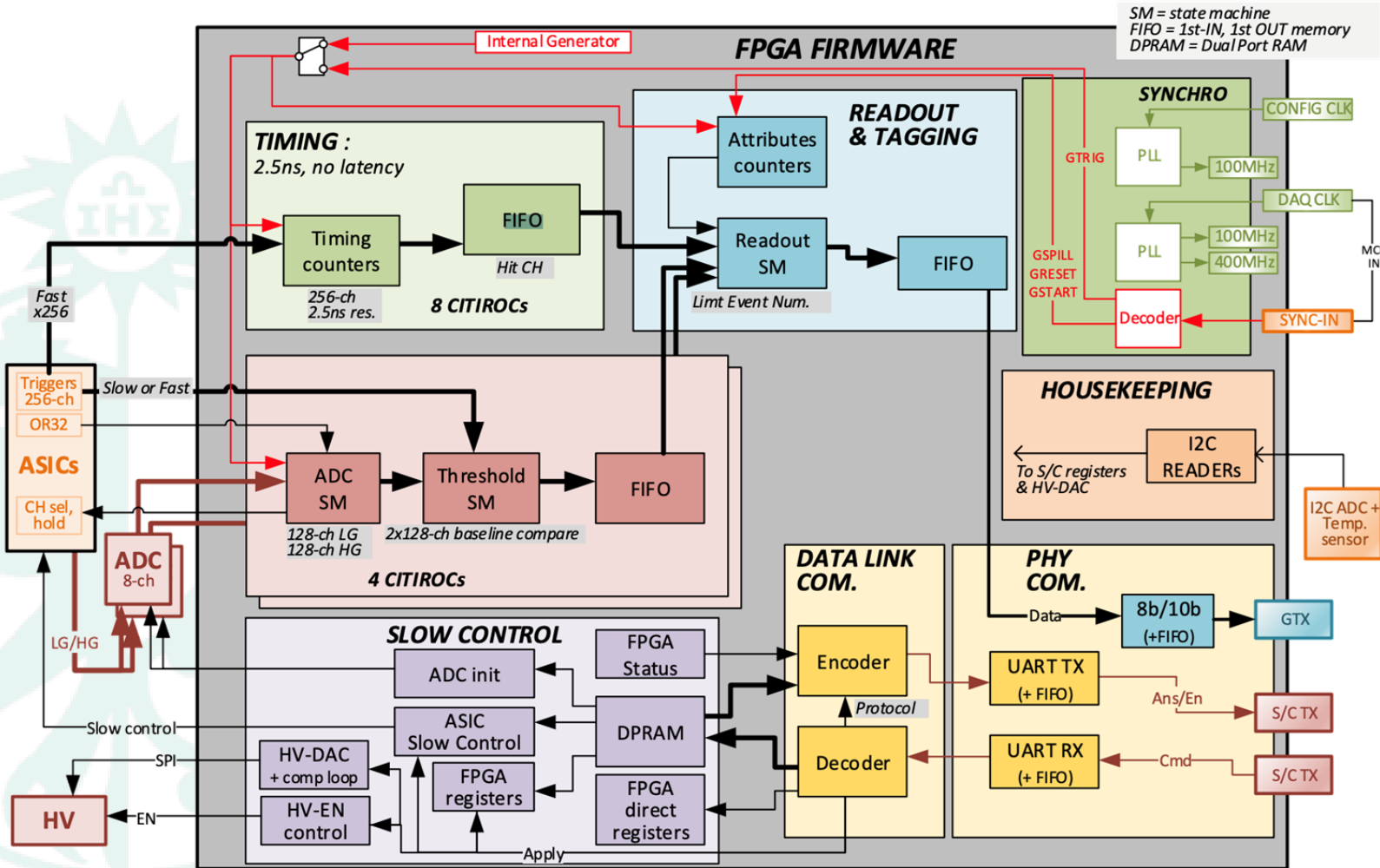
16 crates – 14 FEBs per crate – 256 read out channels per FEB

- Master Clock Board (MCB):
 - ❖ → CLK, SYNC to OCB
- Optical Concentrator Board (OCB)
 - ❖ → CLK, SYNC to FEB
 - ❖ ← Data from FEB
 - → Data to DAQ PC
 - ❖ ⇔ S/C to and from FEB
- Front-end Board (FEB)
 - ❖ ← CLK, SYNC from OCB
 - ❖ → Data to OCB
 - ❖ ⇔ S/C to and from OCB
- Backplane:
 - ❖ OCB-FEB interface and power distribution



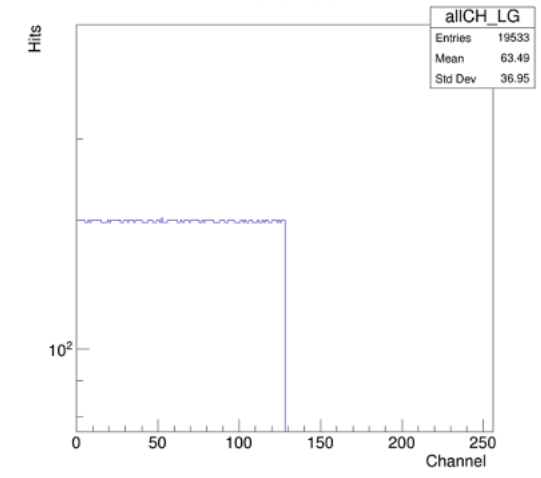
OVERVIEW: 16 crates – 14 FEBs per crate – 256 read out channels per FEB





- Problem: CITIROC (group 1) configuration fails
- Cause: reflections on the ROC-FPGA bidirectional level translator
 - ❖ Due to change in design between FEB v1 and v2
- Solution: increase current on FPGA pin out
 - ❖ Design improvement in v3 (adding capacitor, change level translator)

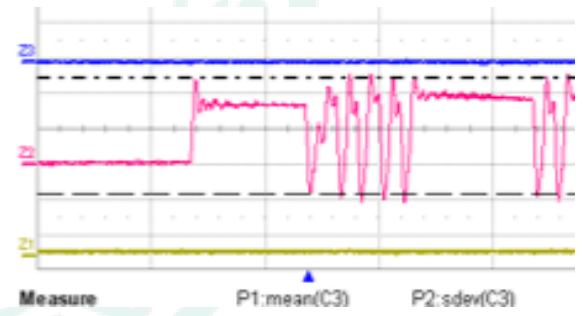
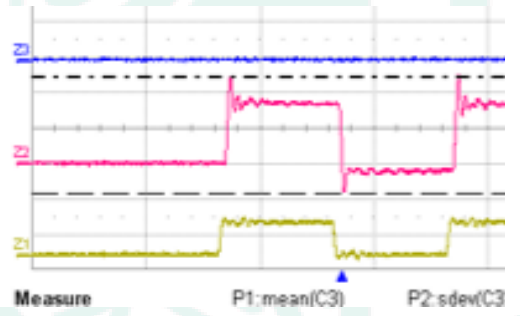
QC test symptom:



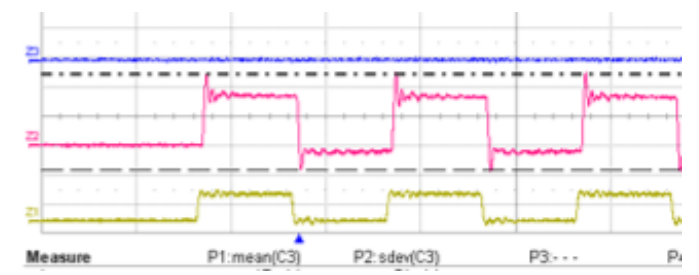
Test S/C signal:

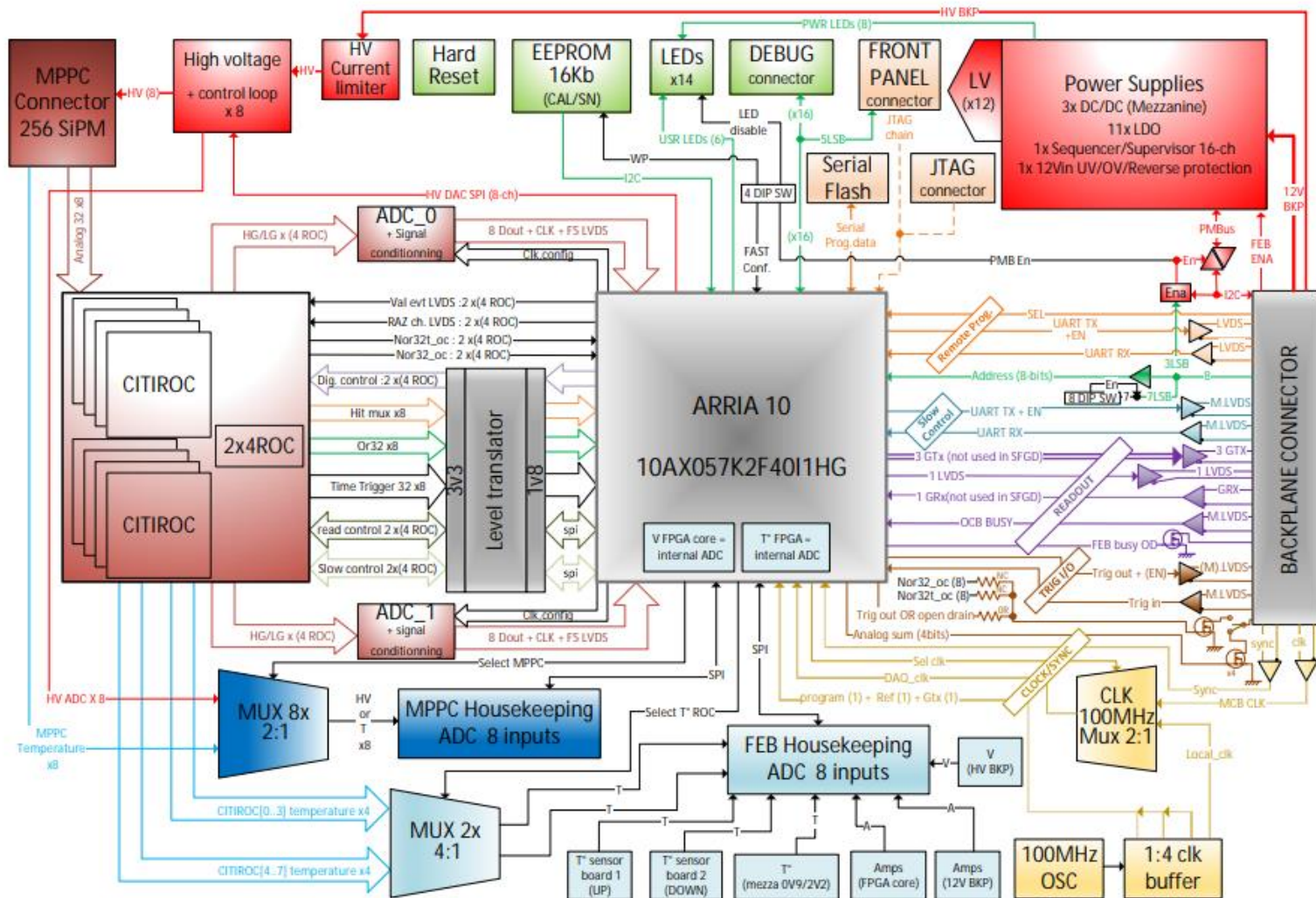
Normal behavior

Faulty FEB



4 mA on FPGA pin-out:





Typical light yields in SFGD

