UNIVERSITÉ DE GENÈVE

Performance tests and hardware qualification of the FEBs for the Super-FGD of T2K Phase II

Topical Workshop on Electronics for Particle Physics

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Outline

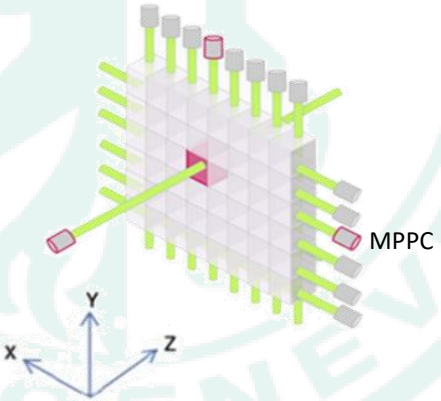
1. Introduction: what is the Super-FGD ?
2. Electronics overview
3. Requirements and FEB performance tests
4. FEB mass production serial testing
5. Conclusions

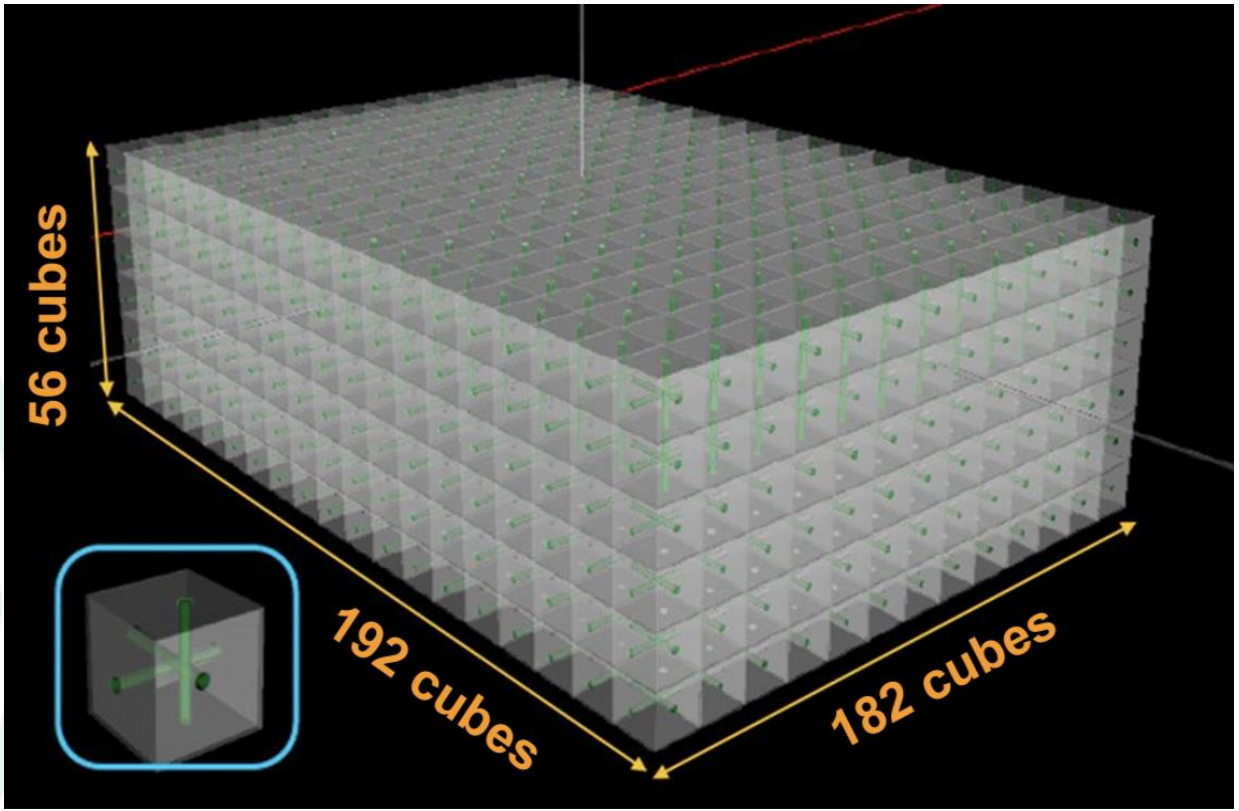
1. What is the Super-FGD?

The Super Fine-Grained Detector

New neutrino active target for T2K Near Detector

- 2-million 1-cm^3 polystyrene cubes
  - 2 tons fiducial mass
  - high granularity
  - 3D tracking
- ~60k optic fibers + SiPM
  - ⇨ 60k readout channels





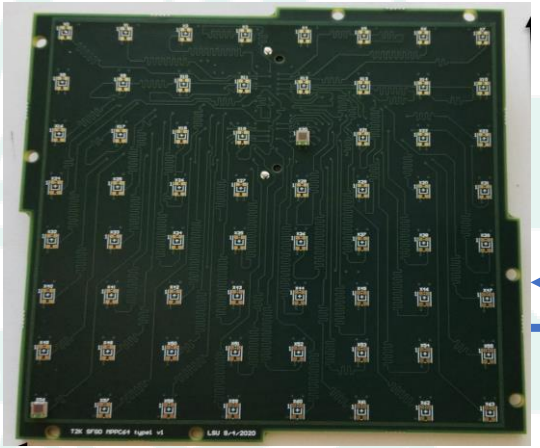
2. Electronics overview and requirements

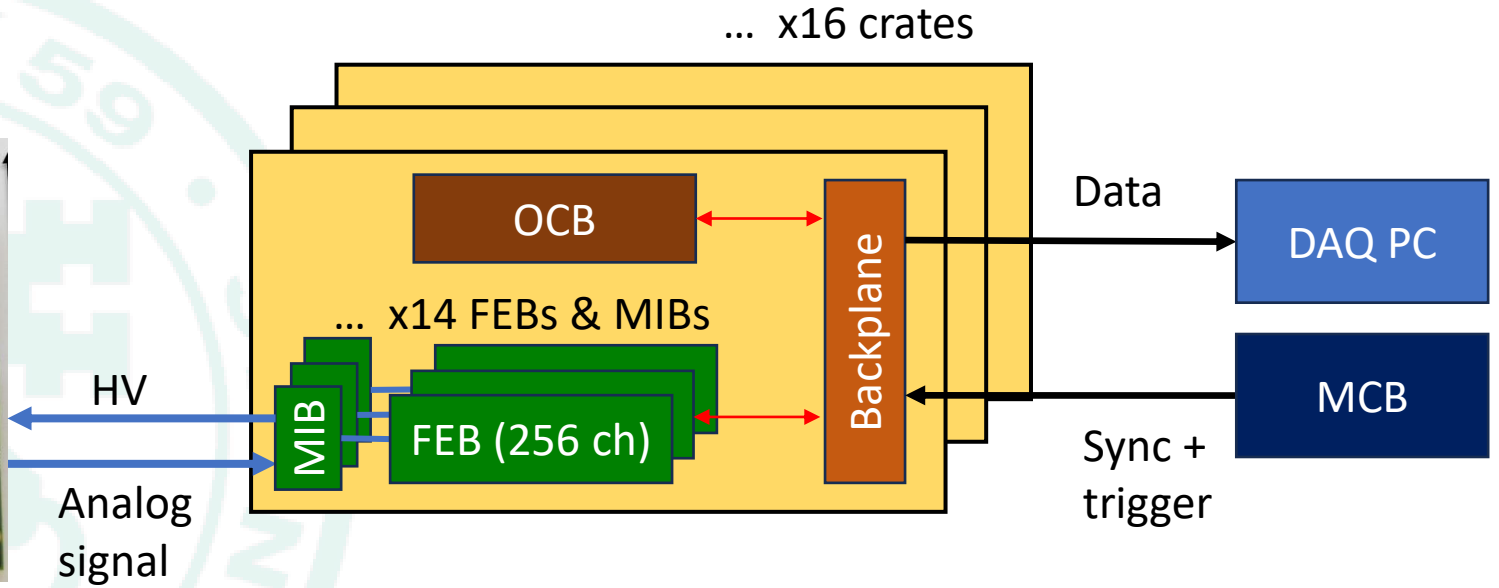
SFGD electronics overview

55’888 SiPM channels ⇒ 16 Crates, 14 FEBs each

OCB (1 per crate) and MCB: S/C, data concentration, sync, trigger

Sensors: MPPC64 (x881)





Focus of this talk: FEB:

Amplification, shaping and digitization of 256 channels

FEB architecture

256 channel charge + timing readout

- 8 CITIROC by Omega [1]:

32-ch read out chips

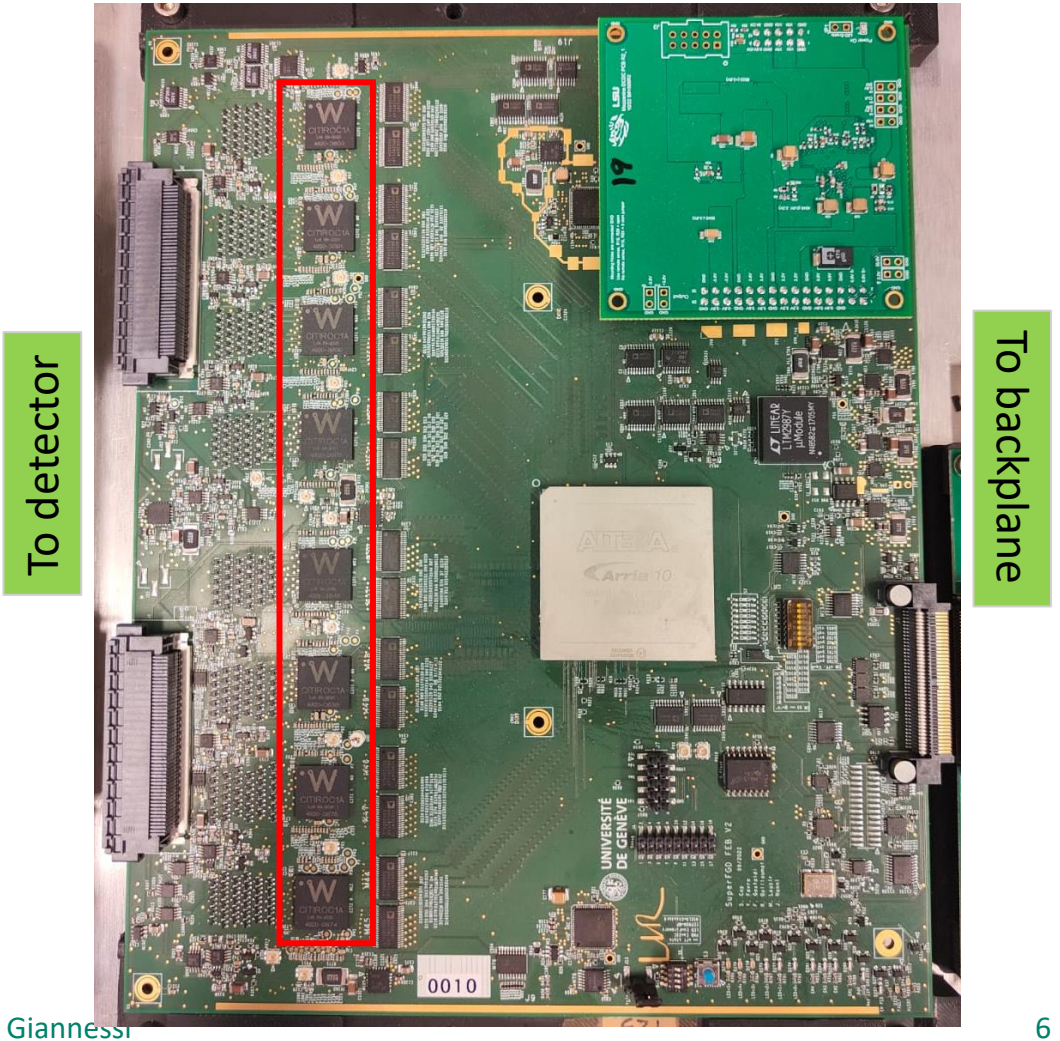
Types of read-out:

- Timing: constant threshold trigger output
- Charge: dual gain peak detector (HG, LG)

Programmable devices:

- Timing and analog thresholds: 10(+4)-bit
- Gain for charge readout: 6-bit
- Shaping time: 3-bit

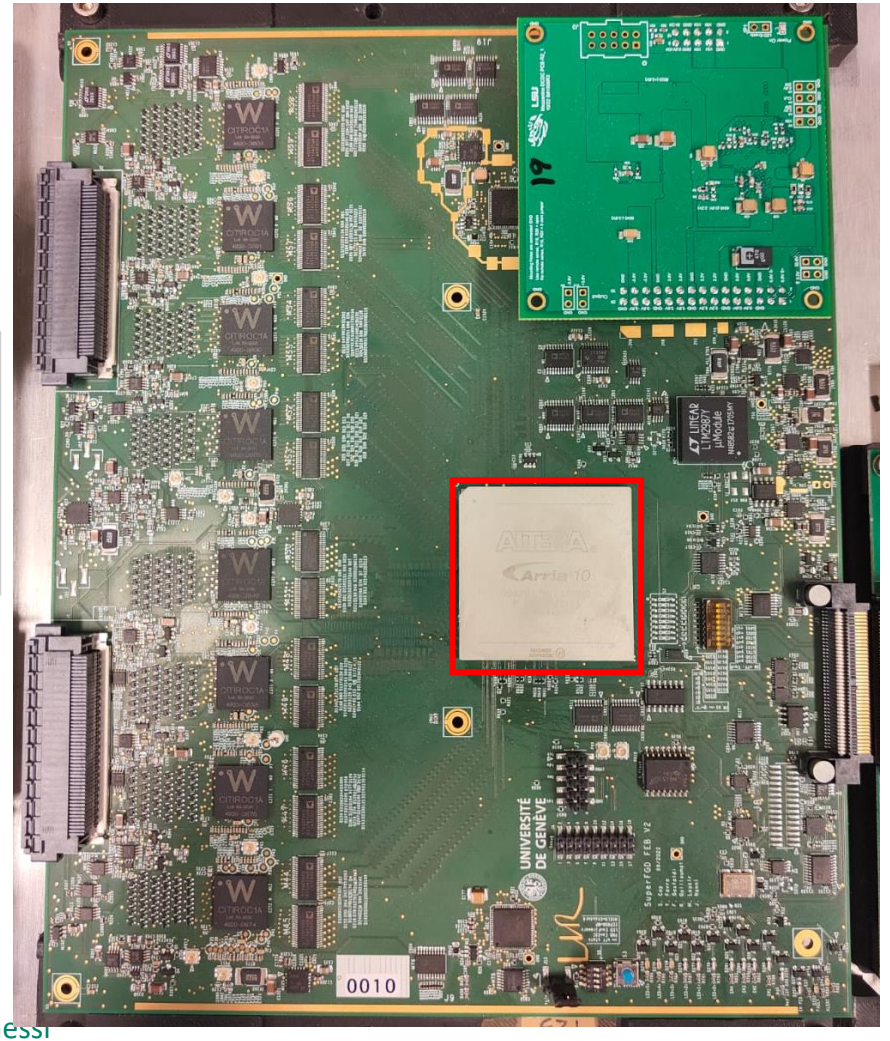
[1] CITIROC by Omega



FEB architecture

Configuration and slow control

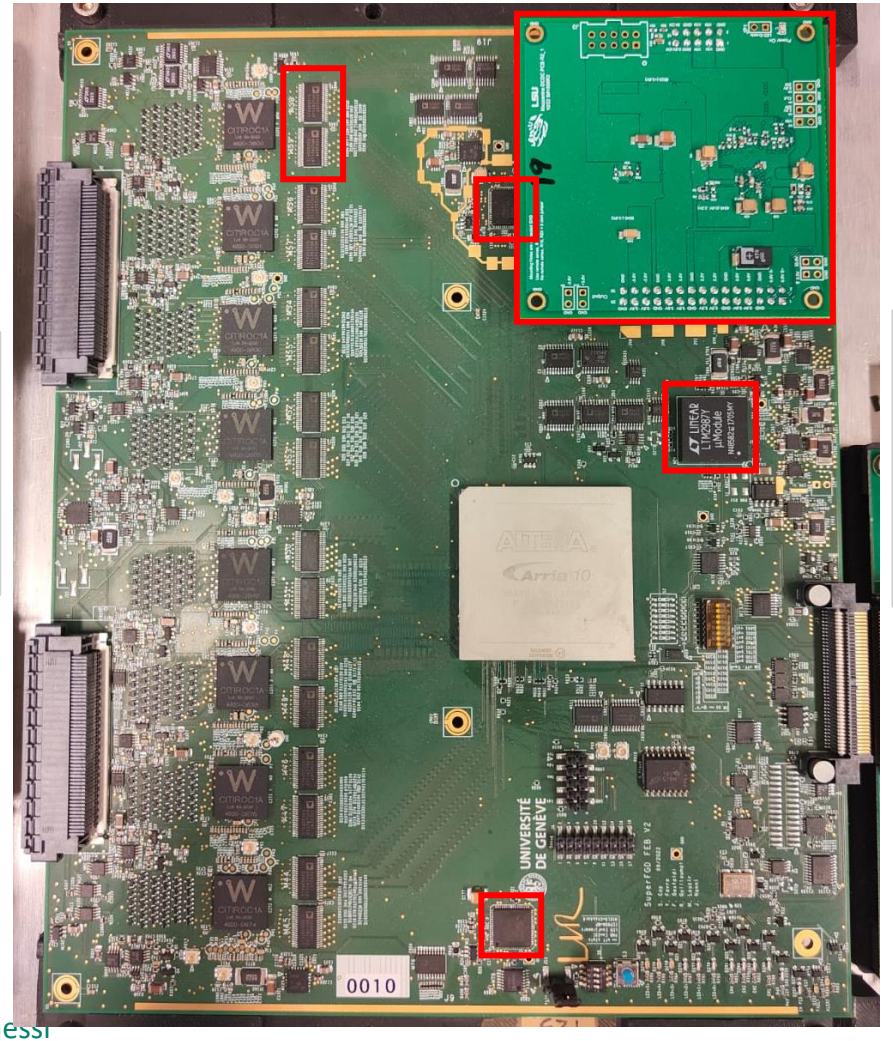
- FPGA ARRIA 10
  - Data concentration and S/C
  - 400 MHz sampling rate for timing measurement
  - ROC configuration
  - Housekeeping
  - Remote programming



FEB architecture

Digitization, power, housekeeping

- Two 8-ch 12-bit ADCs for charge digitization
- Sensors for temperature, voltage and currents
- Supervisor chip
- DC-DC mezzanine board
- 16 3v3-1v8 level translators
- EEPROM for calibration data



3. Requirements and performance tests

Validation of the FEB design against detector requirements

Requirements

- Dynamic range: 1 – 1000 p.e (or 100 fC – 100 pC)
- Energy resolution < 1 p.e. in HG mode
- Electronics cross talk below 1%
- 1 ns timing resolution

Challenges:

~1 year for production + hardware testing + installation

Limited space inside UA1 magnet

~10 years expected lifetime

Dynamic range & energy resolution

Dynamic range

Limited by **non-linearity** of the CITIROC response.

Upper limit: LG linear limit

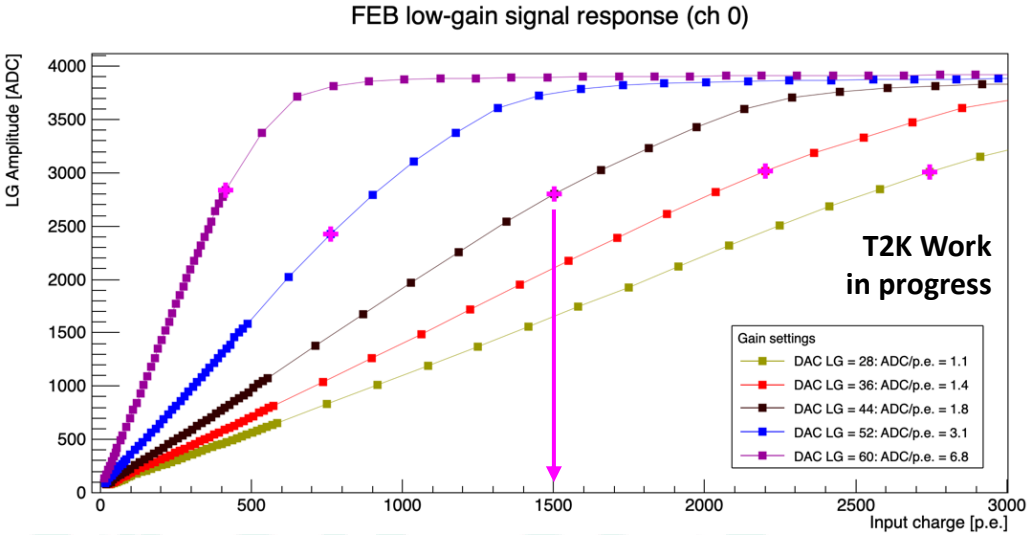
LG linear limit > 1000 p.e

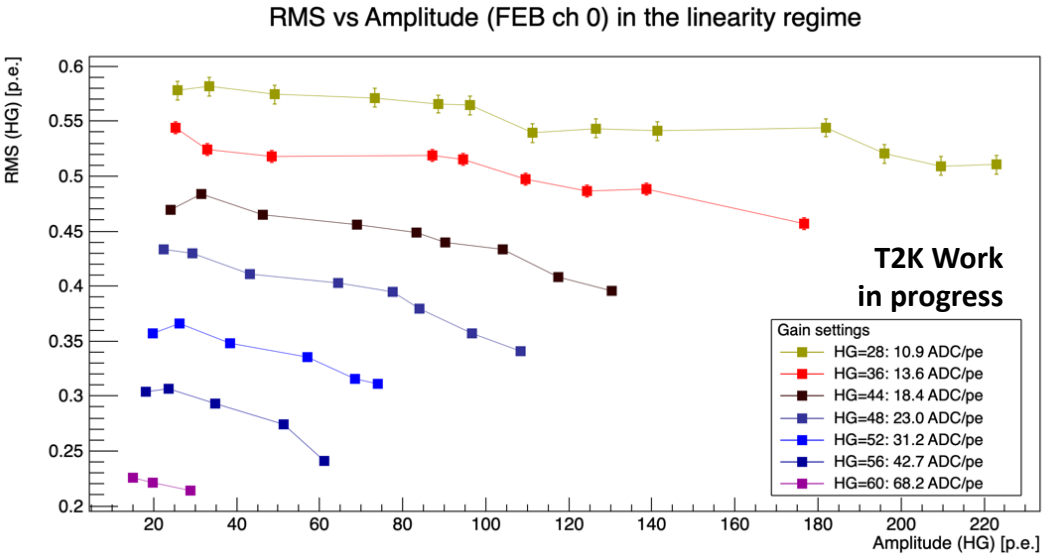
Energy resolution (HG output)

Electronic noise degrades energy resolution.

Study RMS of the signal in HG mode.

RMS < 1 p.e.



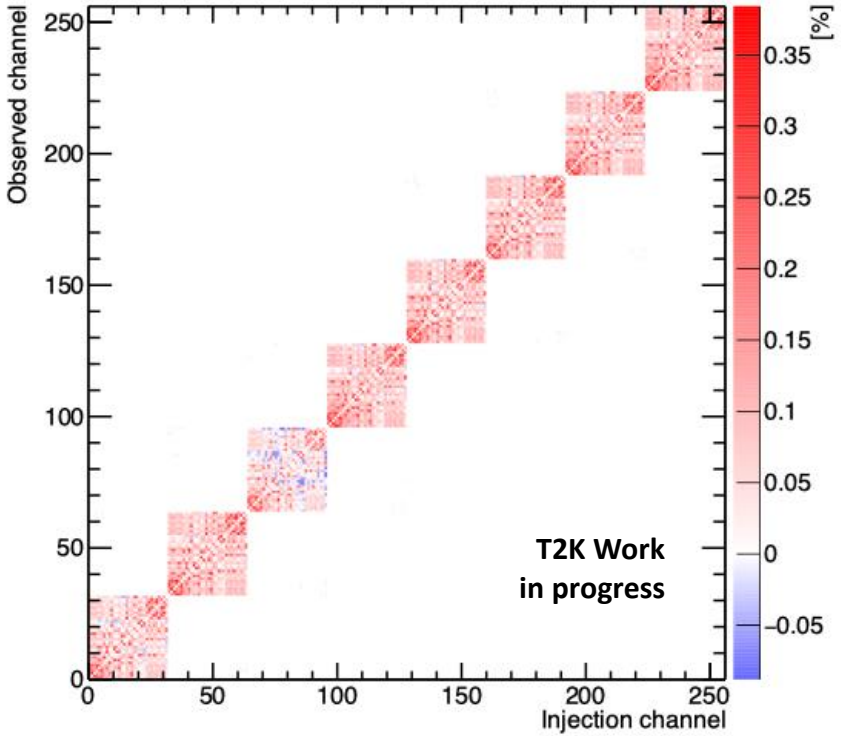


Cross talk & timing

Electronics cross talk:

< 0.5 %

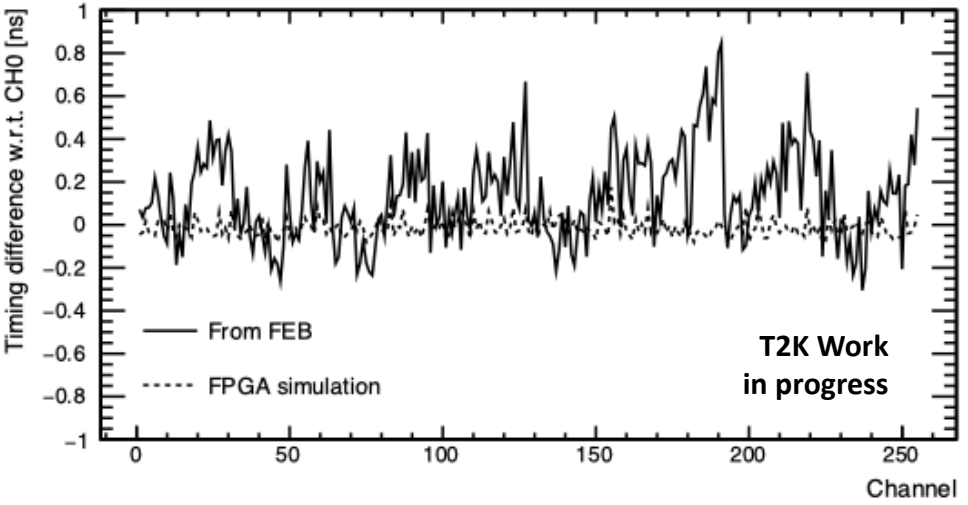
Only intra-ROC



Channel-by-channel timing delays:

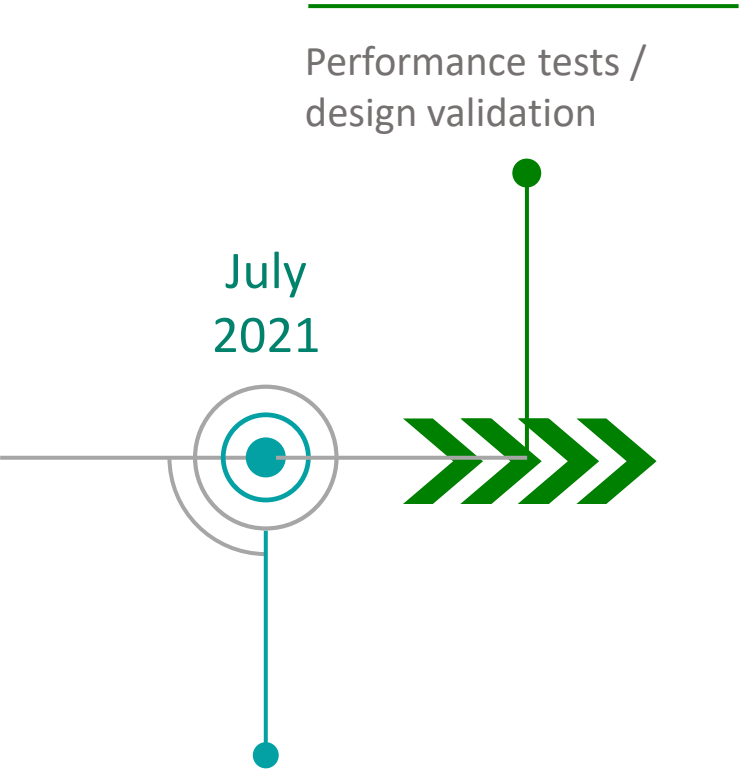
~ 1 ns

→ Need time calibration or FPGA programmable delay

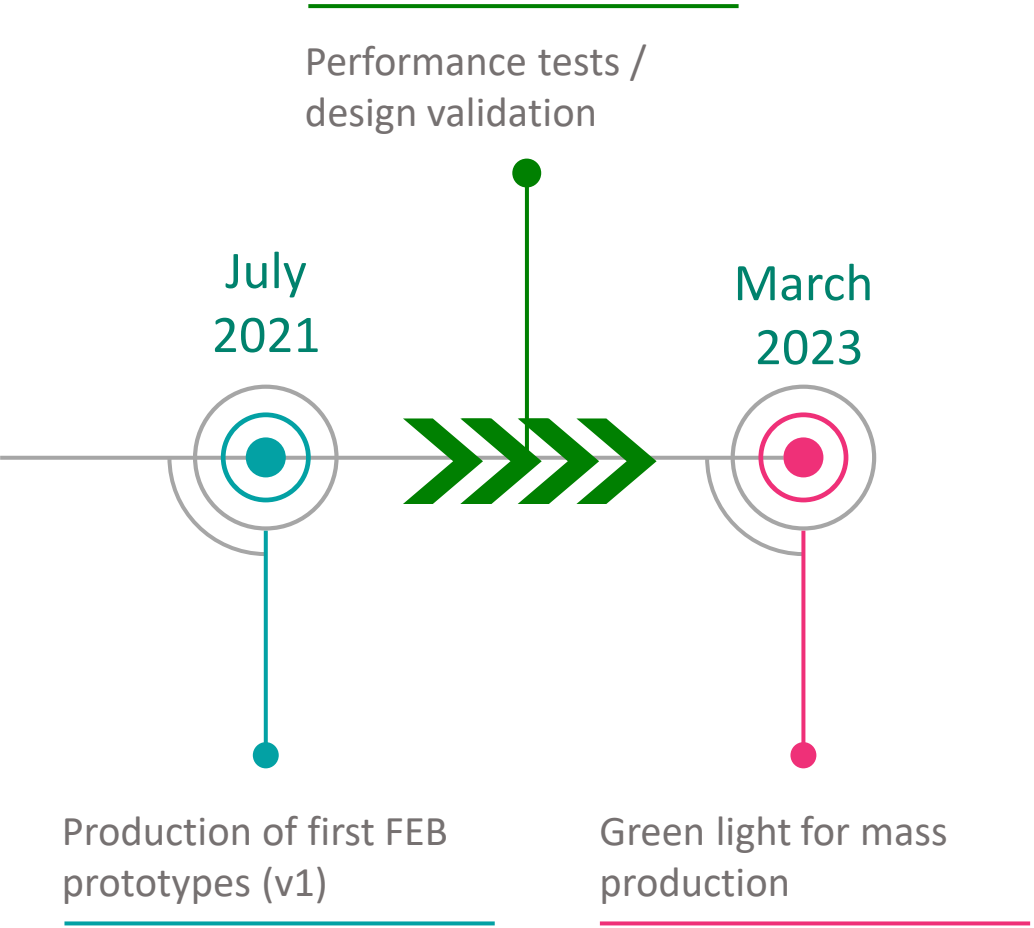


Work by J.Chakrani

History of the Super-FGD FEBs



History of the Super-FGD FEBs



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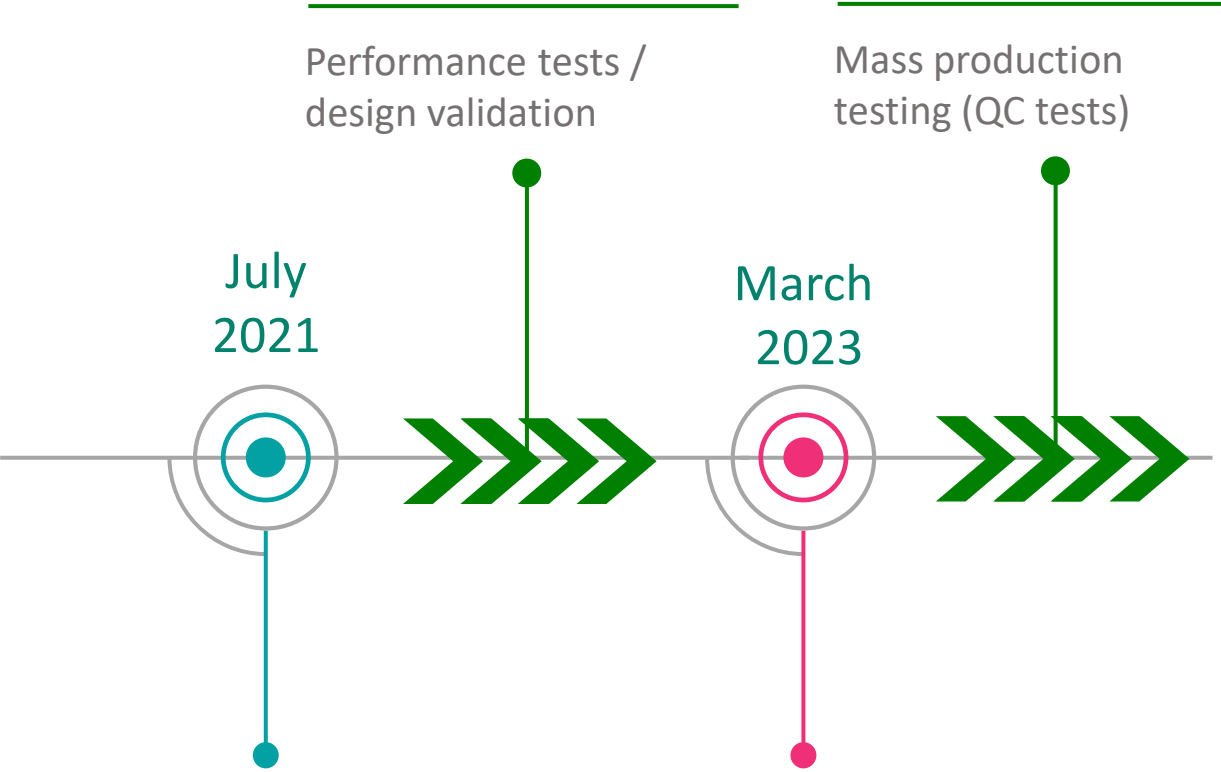


4. Mass production testing

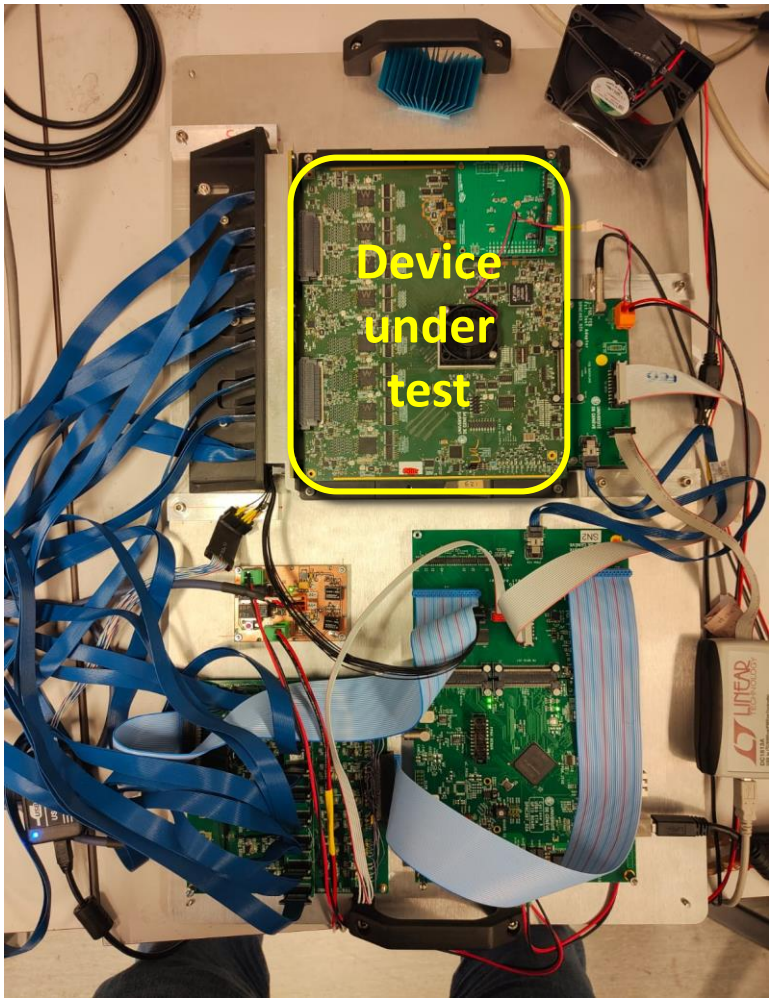
Hardware quality check for the FEB mass production

Hardware serial testing

Mass production: 240 FEBs -> serial hardware testing

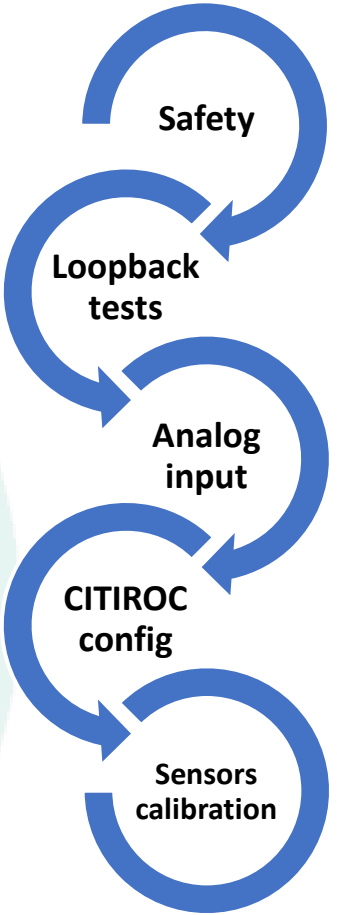
Challenge: need to speed up the testing (and repairing!) process.

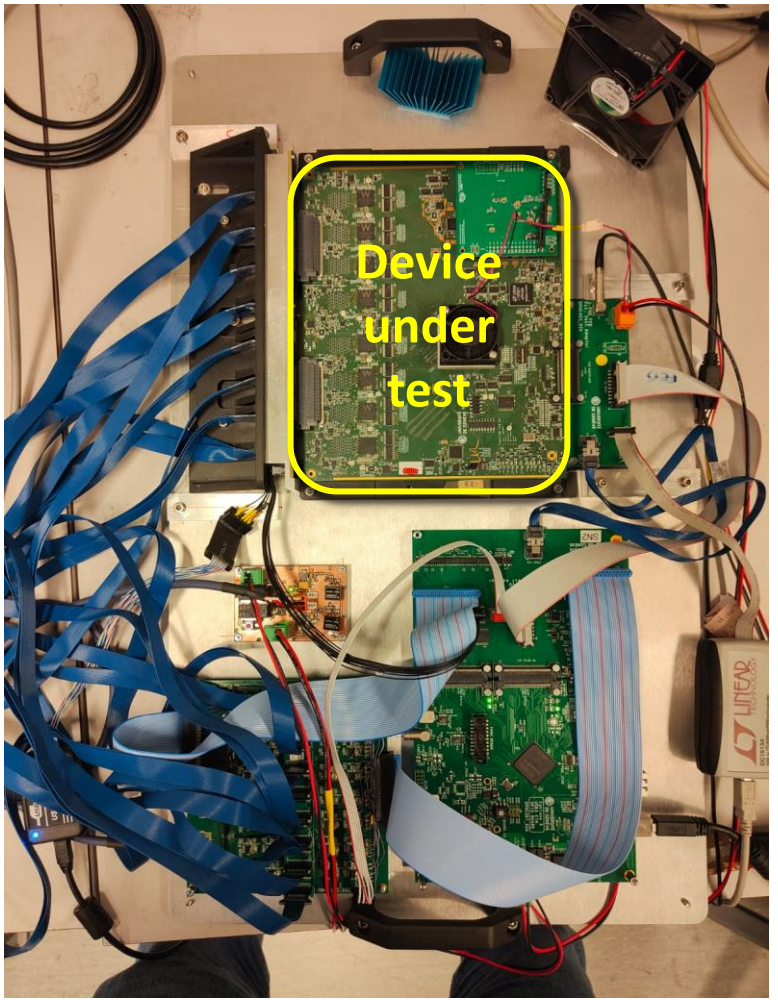
Solution: custom QC test bench with "*symptom → HW issue*" diagnostic.



Hardware serial testing

- Table-top setup, **6 minutes**
- ***99%*** hardware coverage:
  - Analog traces
  - Sync, clk, trigger, busy
  - CITIROC configuration, S/C
  - HV/T sensors + calibration
- Custom auxiliary board
- **Flexible**: edit software to test specific hardware problems
- **Locate** HW problems



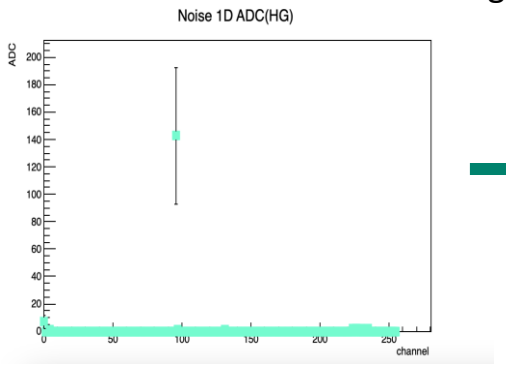


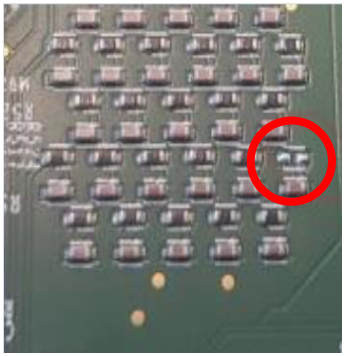
Hardware serial testing

Some problems are easy to understand and fix

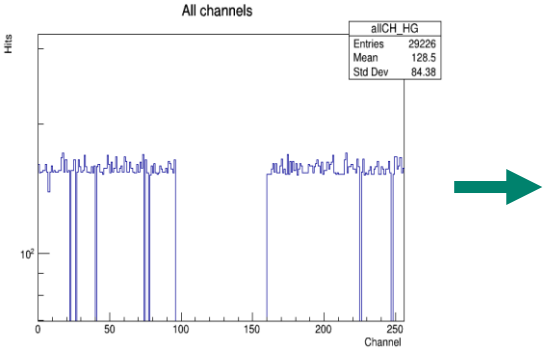
- Bad/cold soldering
- Missing/wrong passive component
- Shorts on surface components

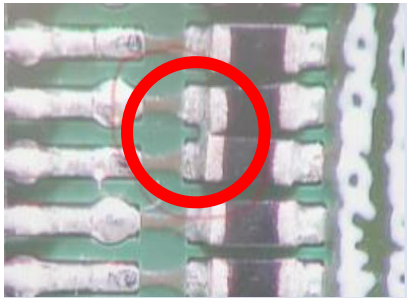
Missing resistor





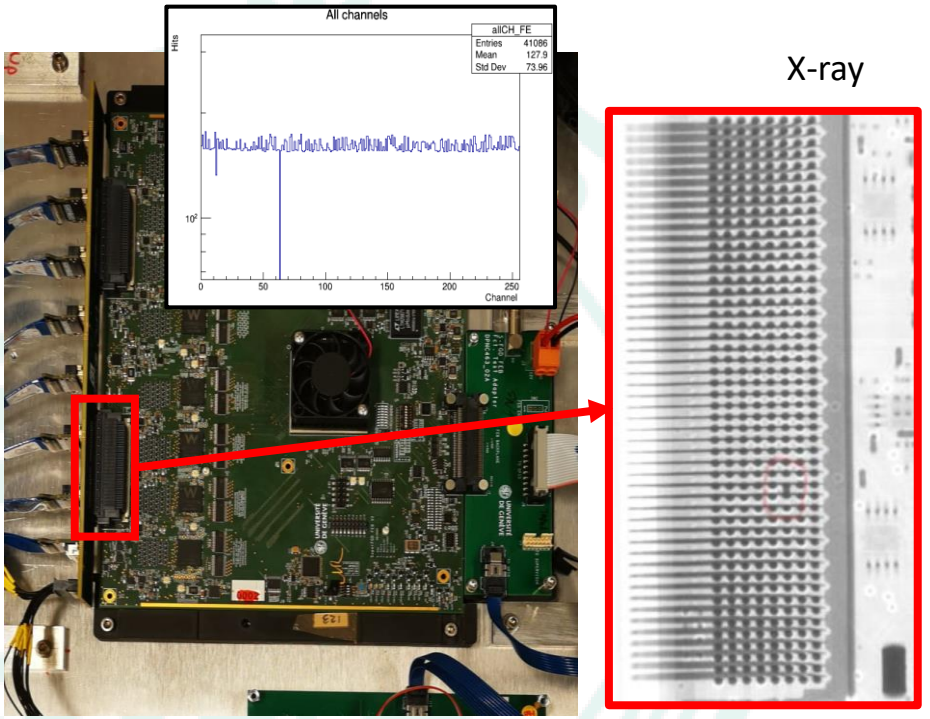
Shorted components





Hardware serial testing

Short circuit in connector



Others can be nasty…

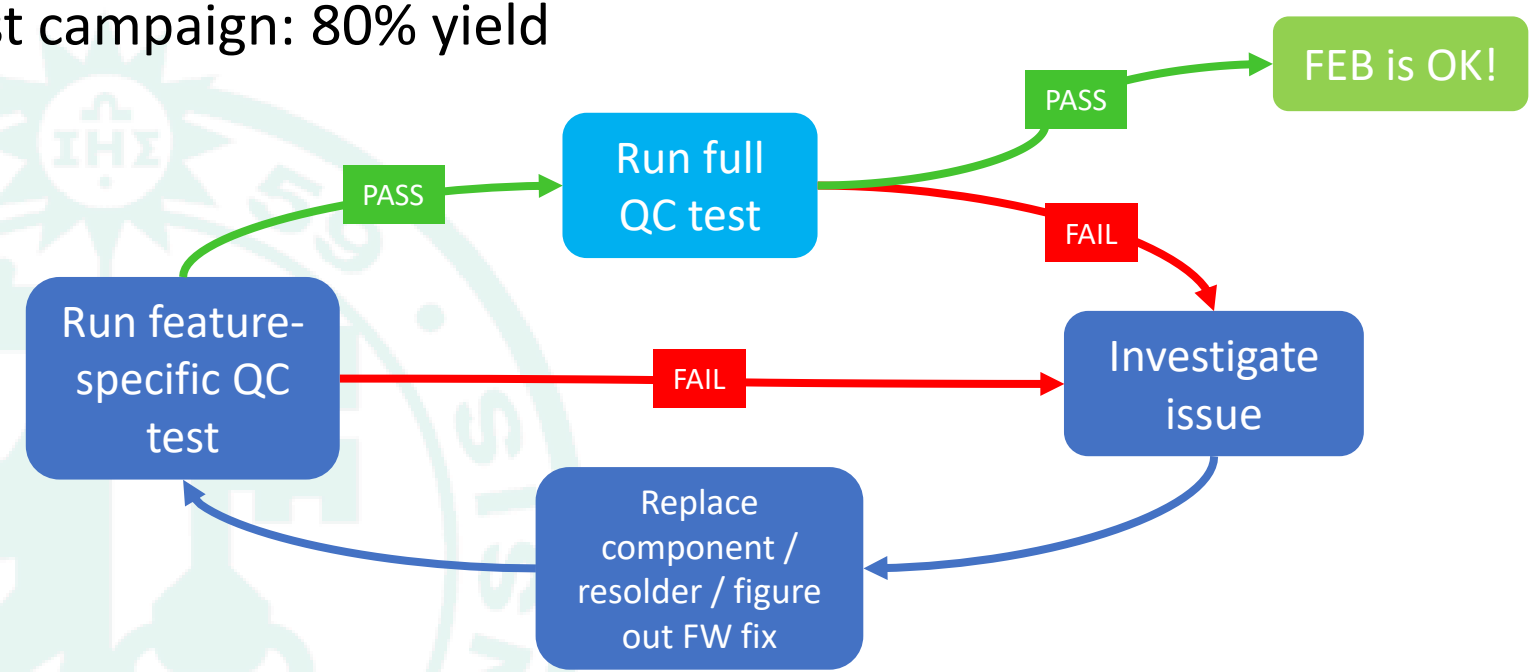
- Shorts under connectors
- Cold-soldered BGA
- CITIROC to be replaced
- Bad PCB routing

Ship back to manufacturer:
major delay

Yield recovery

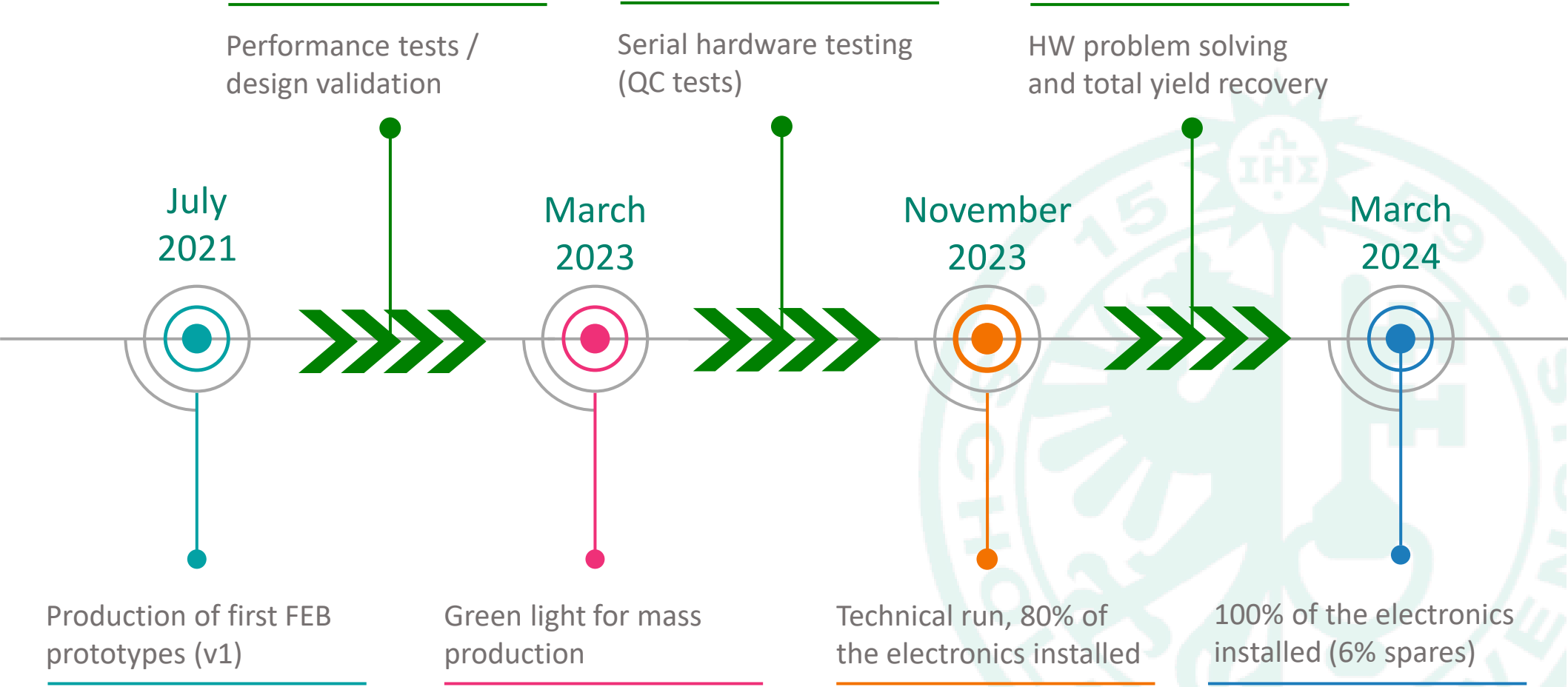
Initial plan: 222 FEBs installed + 10% spares

First QC test campaign: 80% yield



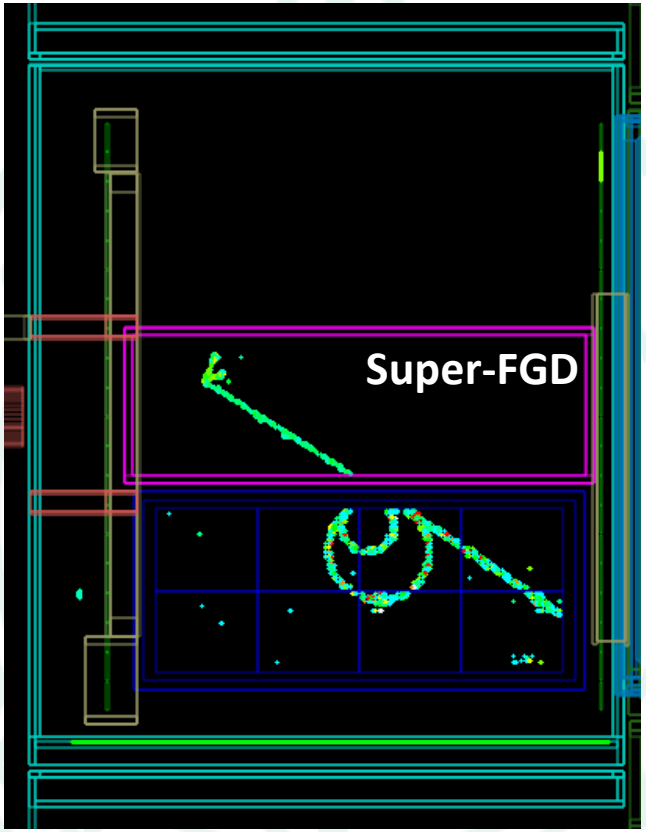
Take-home message: A custom, versatile QC setup is more work, but ends up saving time and resources.

History of the Super-FGD FEBs



5. Conclusions

- FEBs for the Super-FGD performances validated and 240 FEBs successfully tested (repaired) and installed
  - Custom, table-top QC test bench proven to be essential



First neutrino beam run of T2K phase II (June 2024)

Back up

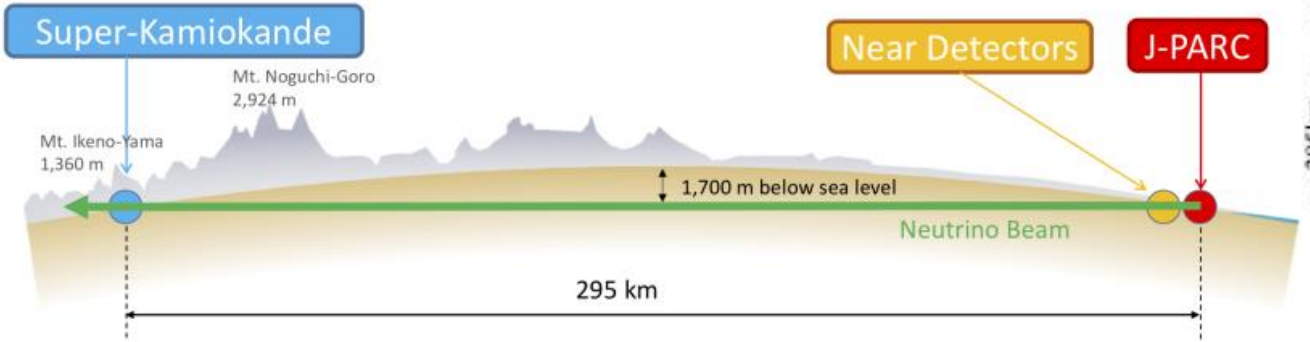
The T2K Experiment

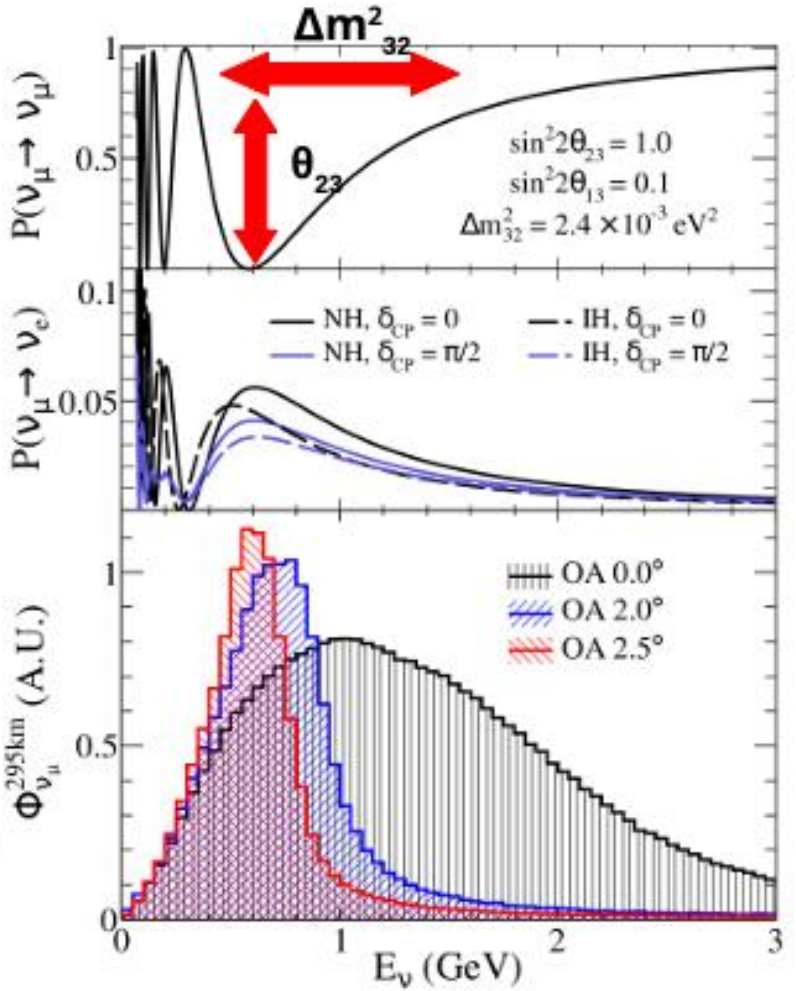
T2K is a **long baseline neutrino oscillation experiment**

Sensitive to δ_{CP} through **electron (anti-) neutrino disappearance**

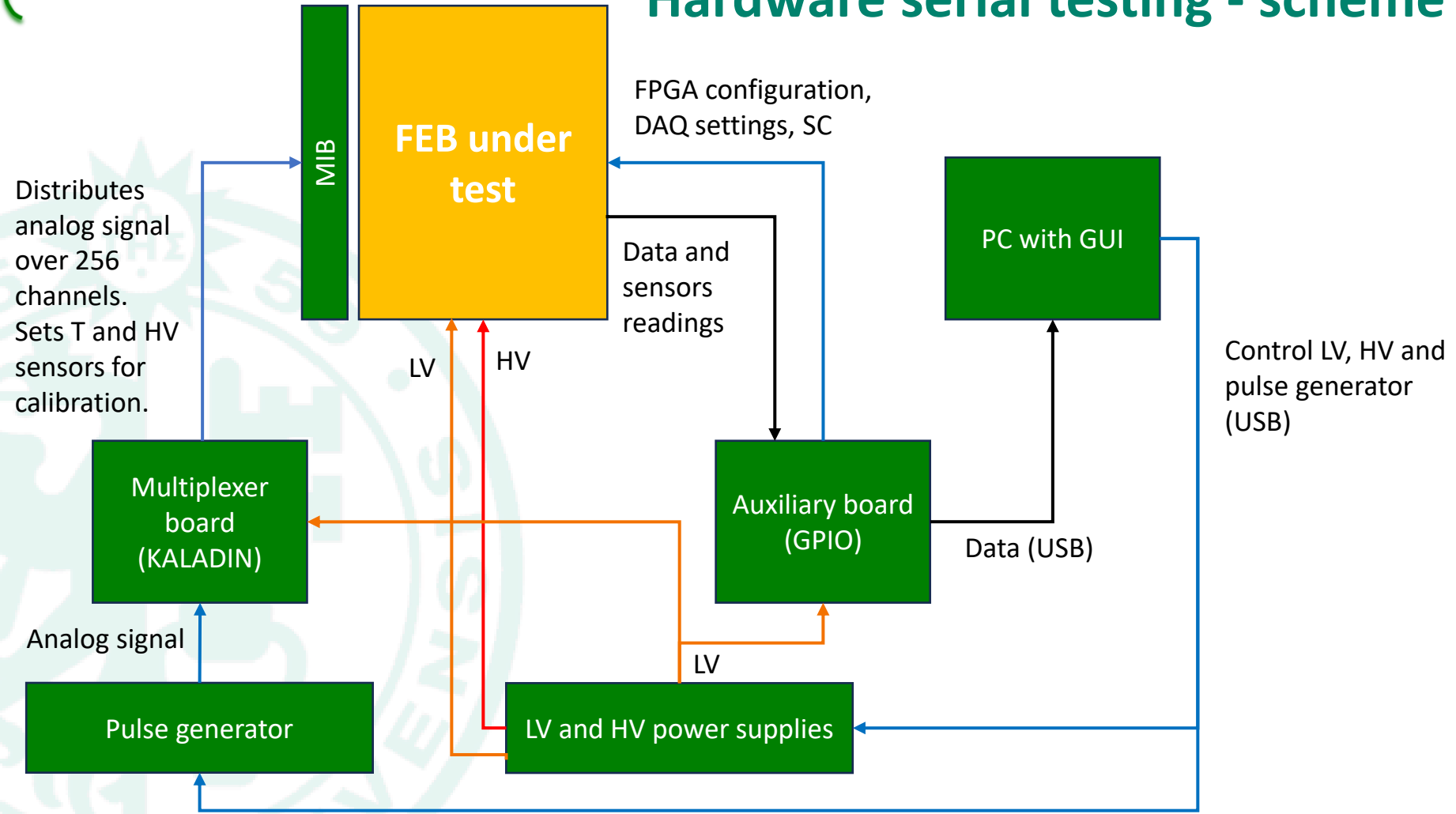
Sensitive to Δm^2_{32} and θ_{23} through **muon (anti-) neutrino appearance**

- Near detector is being upgraded with 3 new subdetectors (Super-FGD, High-angle TPCs, TOF)
  - Super-FGD: new neutrino active target





Hardware serial testing - scheme



Hardware serial testing

- **Safety:**

Test HV current limiter circuit

- **Slow control**

Test slow control lines (FPGA to backplane, FPGA to CITIROC,) with loopback circuits (FPGA driven)

- **Analog input**

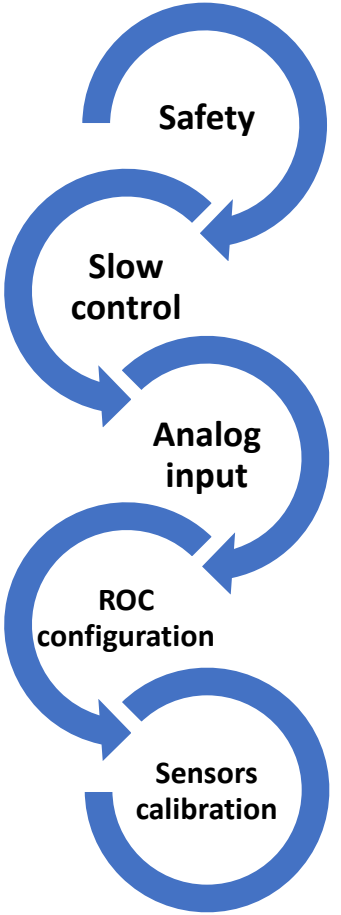
Test all channels against open/short circuits. Check ADC output validity range. Evaluate noise and baseline – extensive use of Kaladin board

- **ROC configuration**

Check that the FPGA is able to configure the CITIROCs with different trigger configurations (ability to control the CITIROC programmable devices)

- **Sensors calibration**

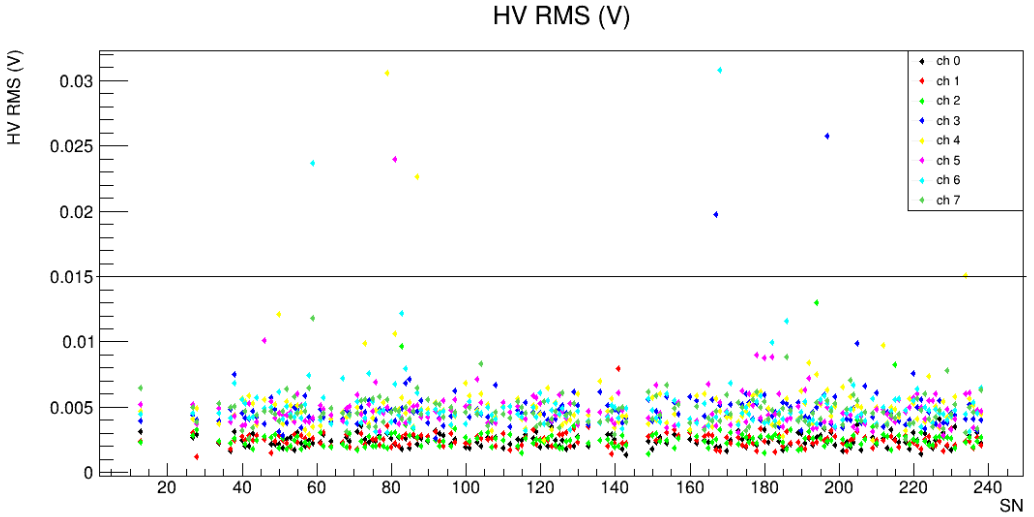
Calibrate the HV and T sensors and check that the calibration constants are stored in the EEPROM. Measure RMS (RC filter test)

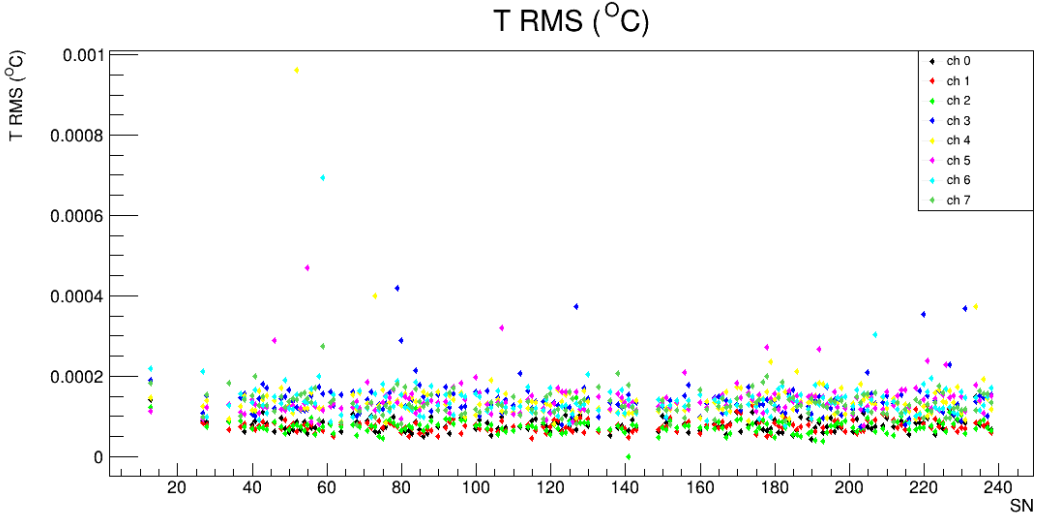


Global testing

Global results on T/HV sensors precision [gain equalization]

- RMS values of the T and HV sensors to evaluate overall performances

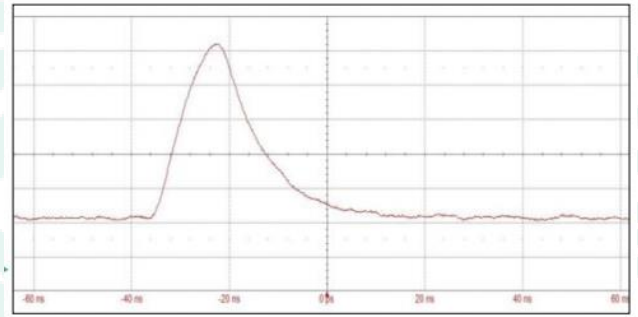




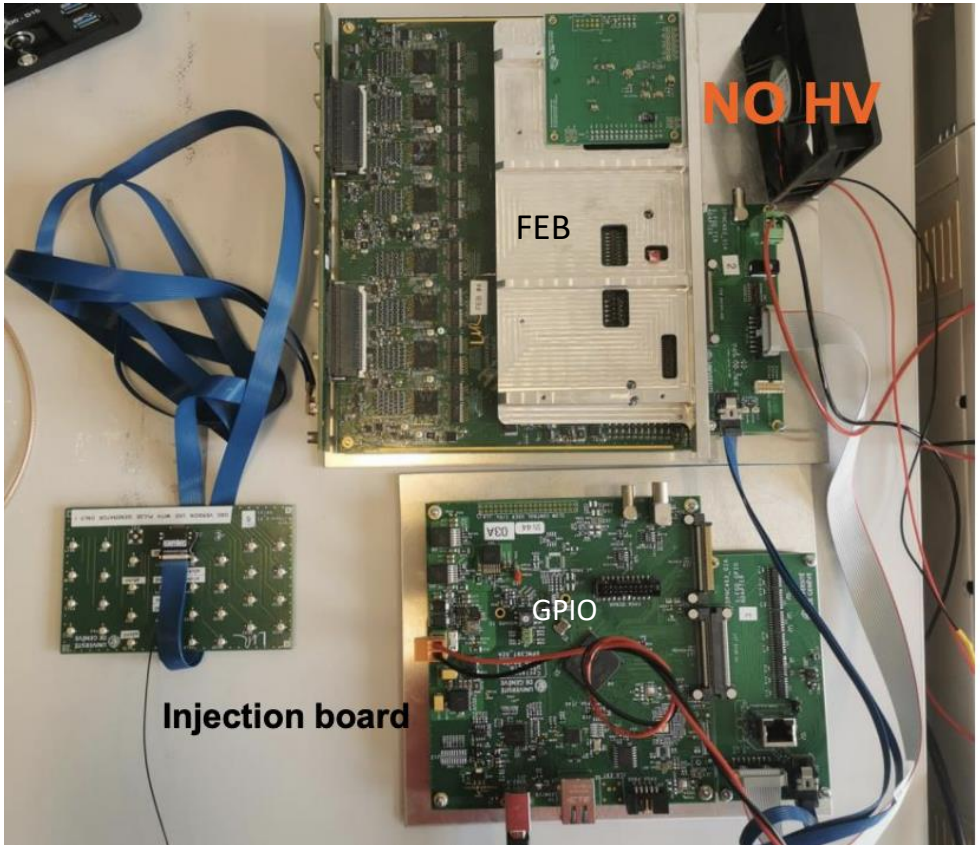
Gain equalization:
55mV/°C HV gain change in MPPC sets requirement on RMS(V)

Linearity range & resolution - setup

Pulse generator + RC filter



To FEB



FEB architecture - CITIROC

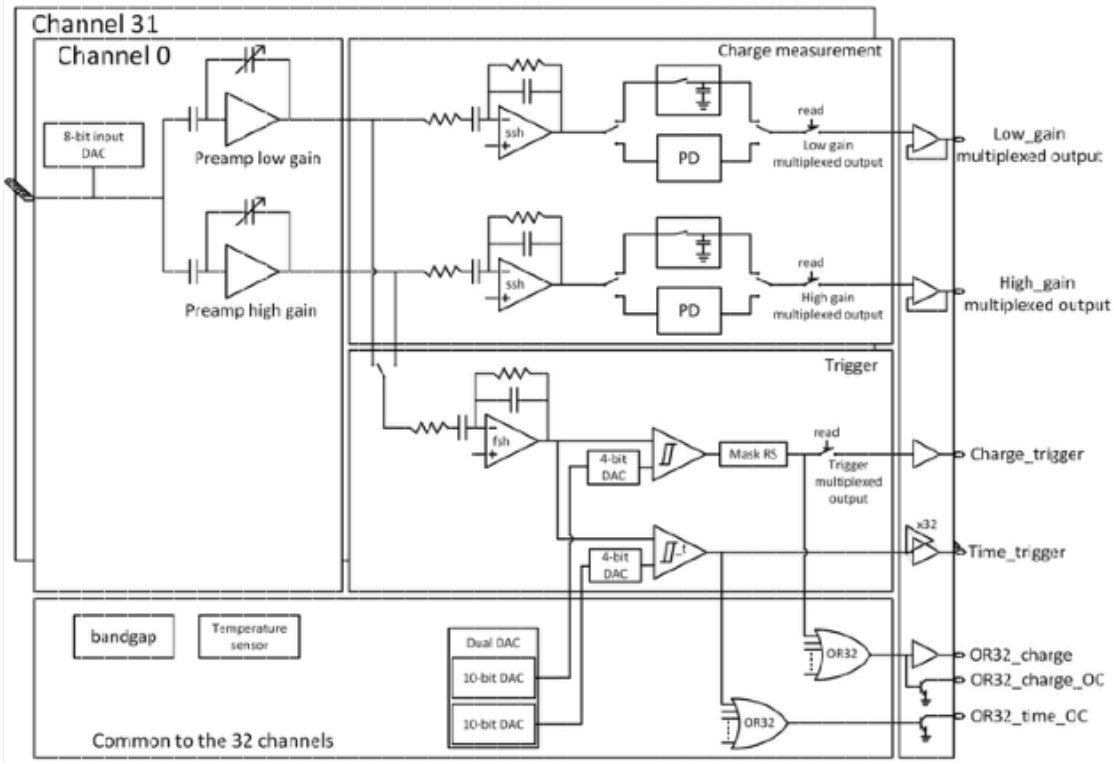
- 32 channels

Types of read-out:

- Timing: constant threshold trigger output
- Charge: dual gain with peak detector (HG, LG)

Programmable devices:

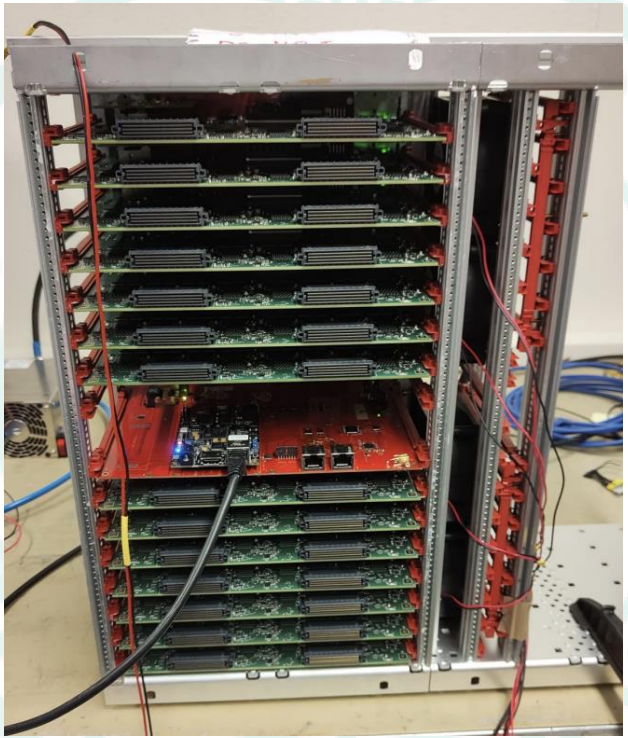
- Timing and analog thresholds: 10(+4)-bit
- Input DAC for MPPC voltage tuning: 8-bit
- Gain for charge readout: 6-bit
- Shaping time: 3-bit

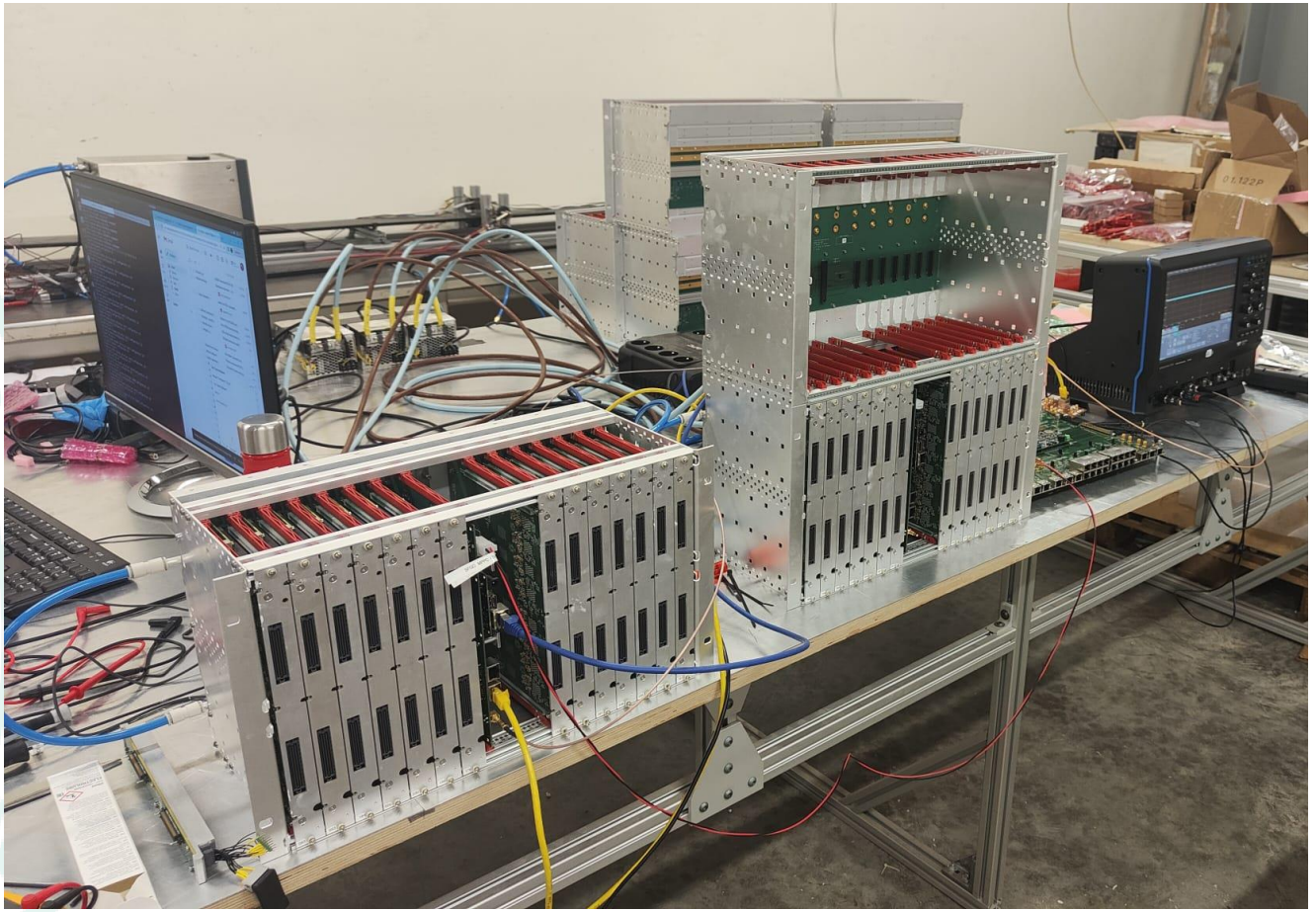


[1] add CITIROC reference here

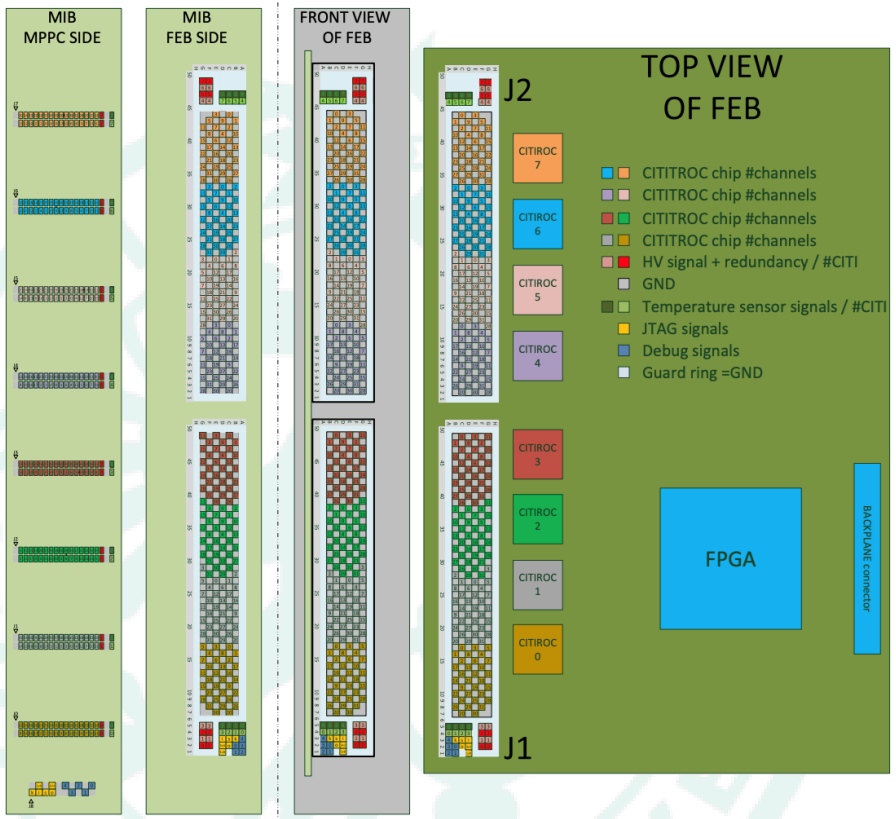
Other tests

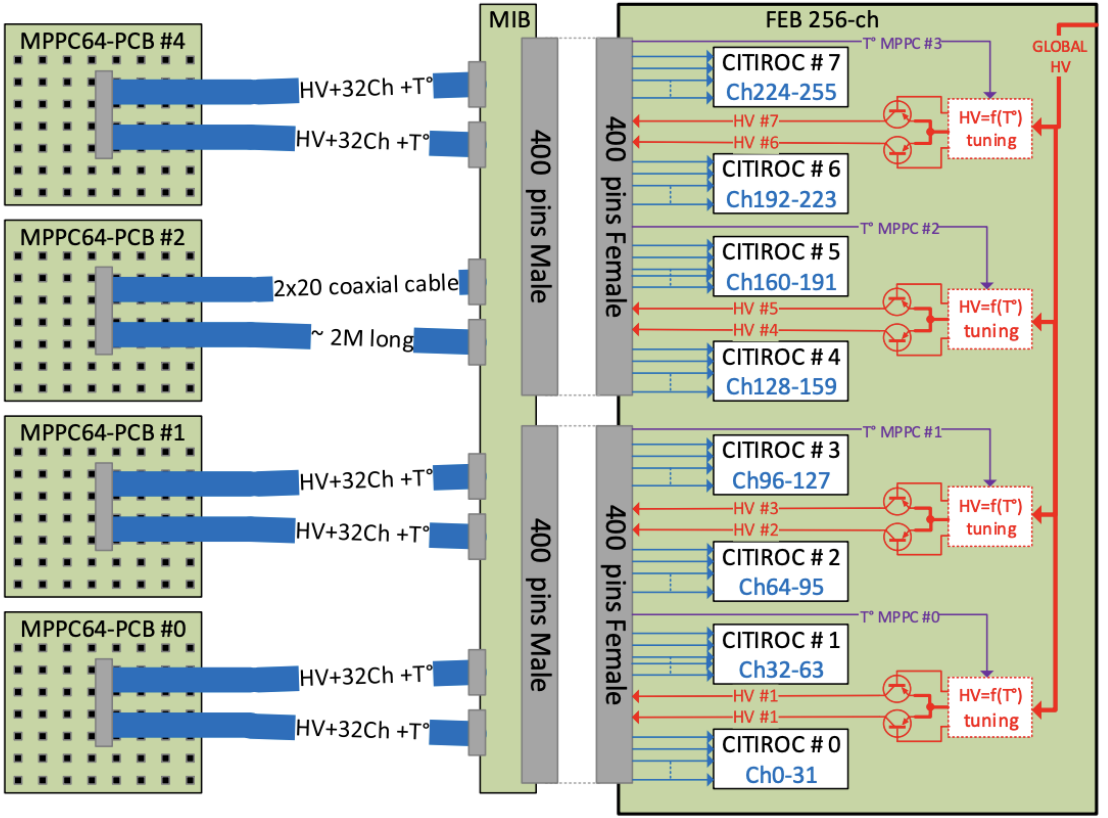
- Full crate “burning test”
- BER tests (OCB-FEB)
- OCB-FEB communication
- MCB-OCB communication
- DAQ stability tests





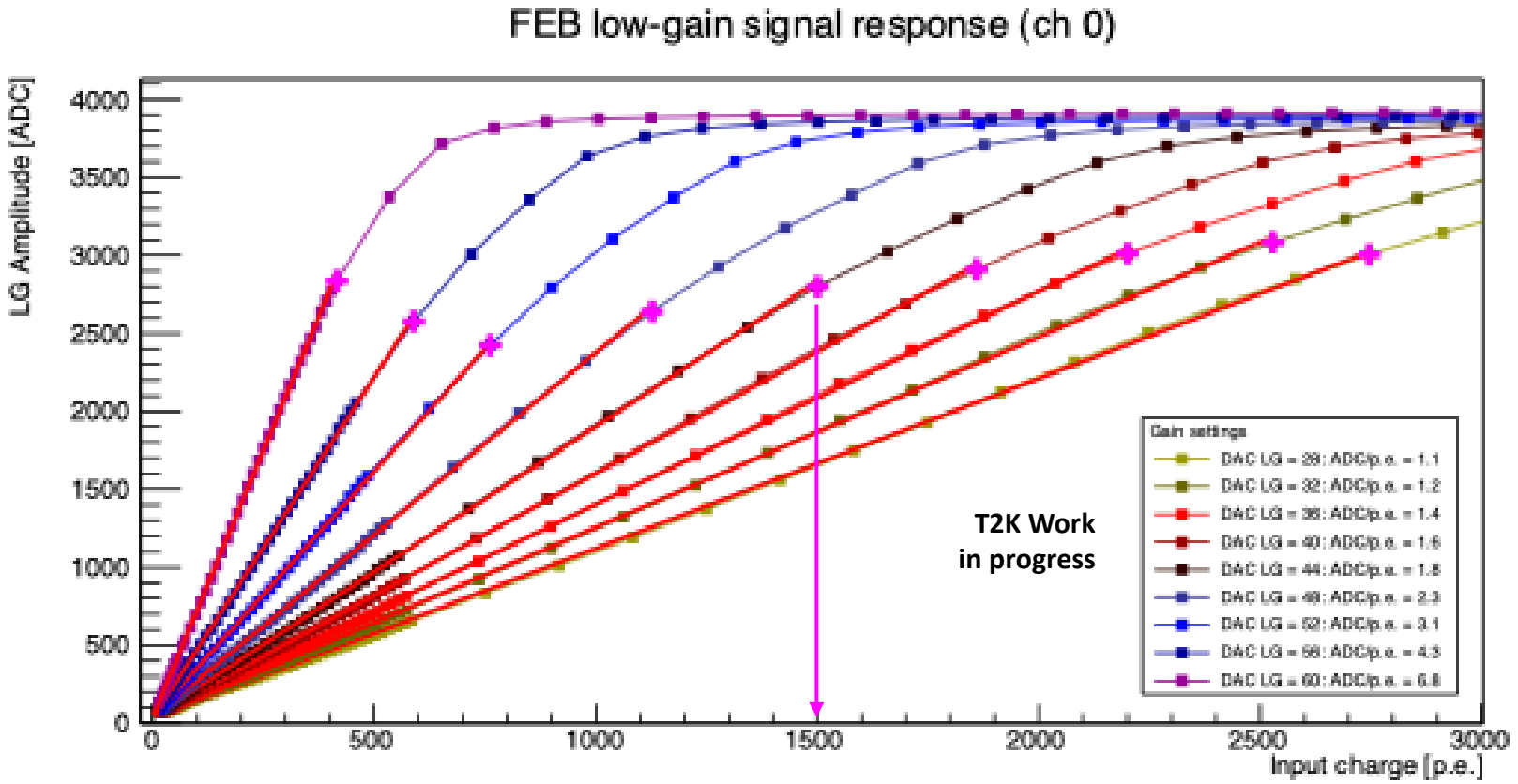
Connectivity





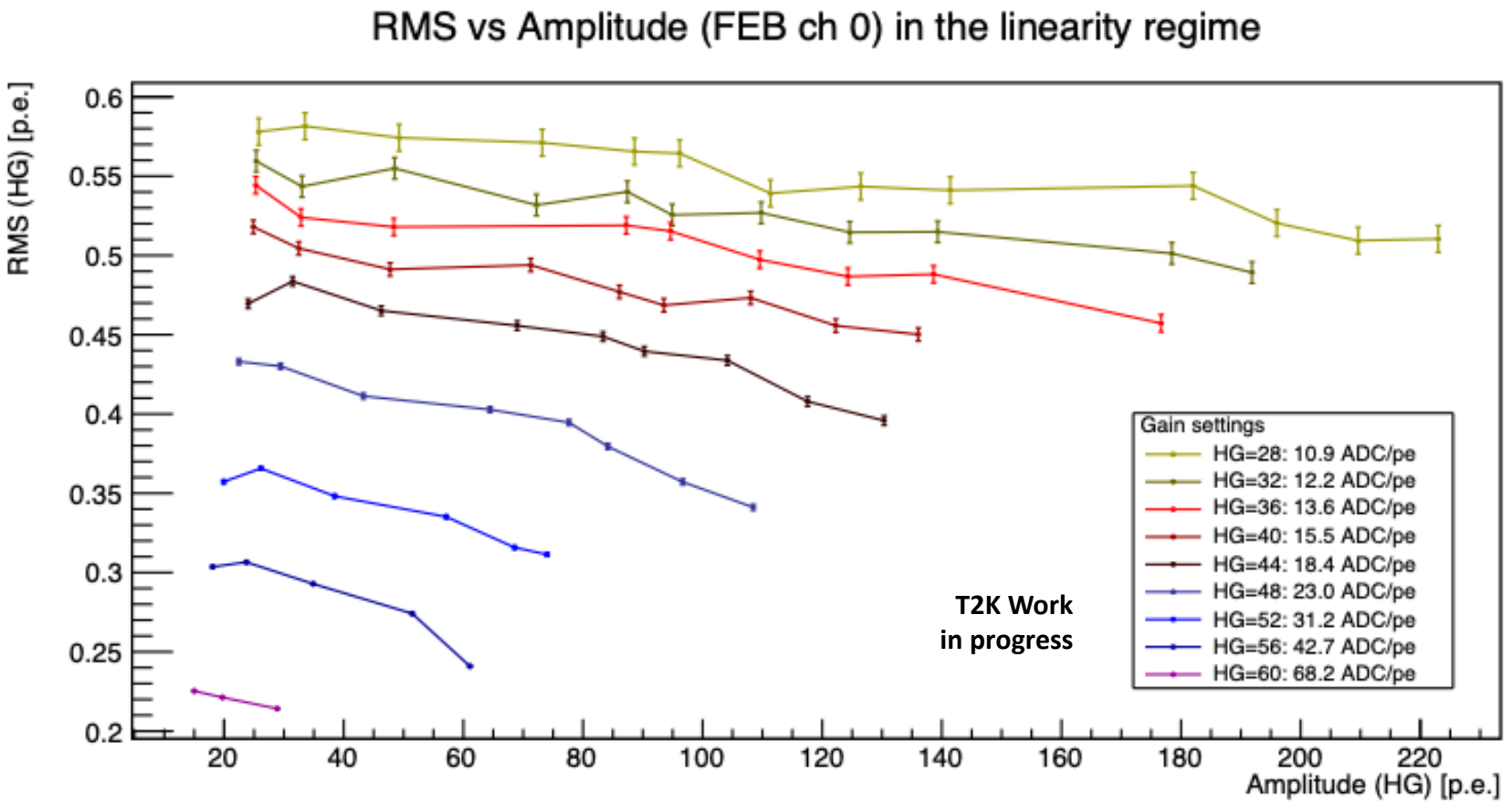
Linearity & energy resolution

Dynamic range



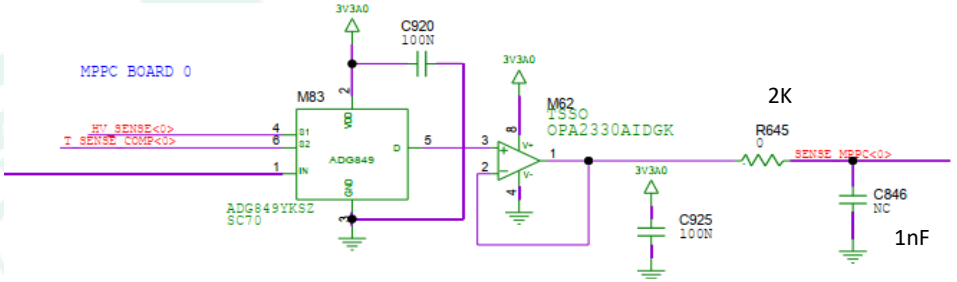
Linearity & energy resolution

Energy resolution (HG output)

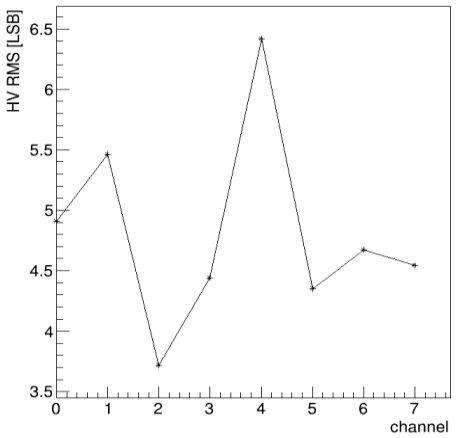


Hardware test: RC filter

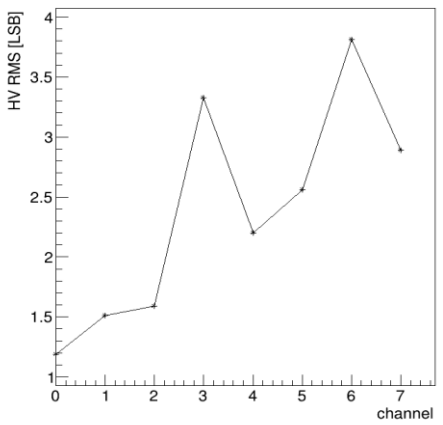
- **Calibration** of HV and NTC sensors
  - **Check passive components**

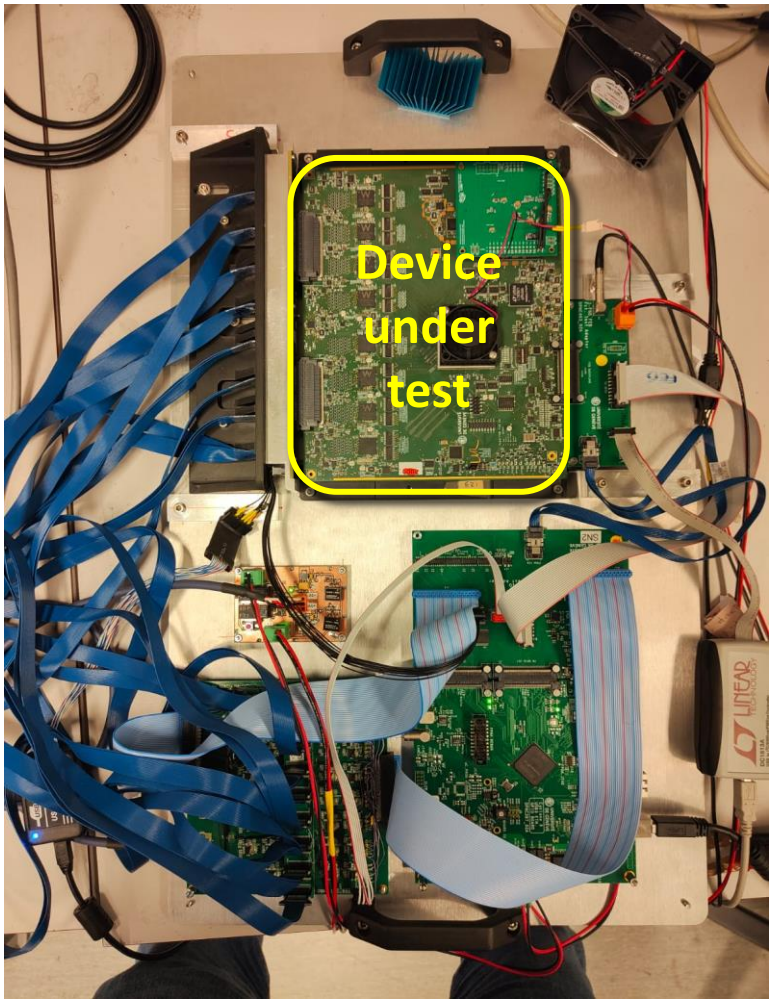


HV RMS **fail**



HV RMS **pass**



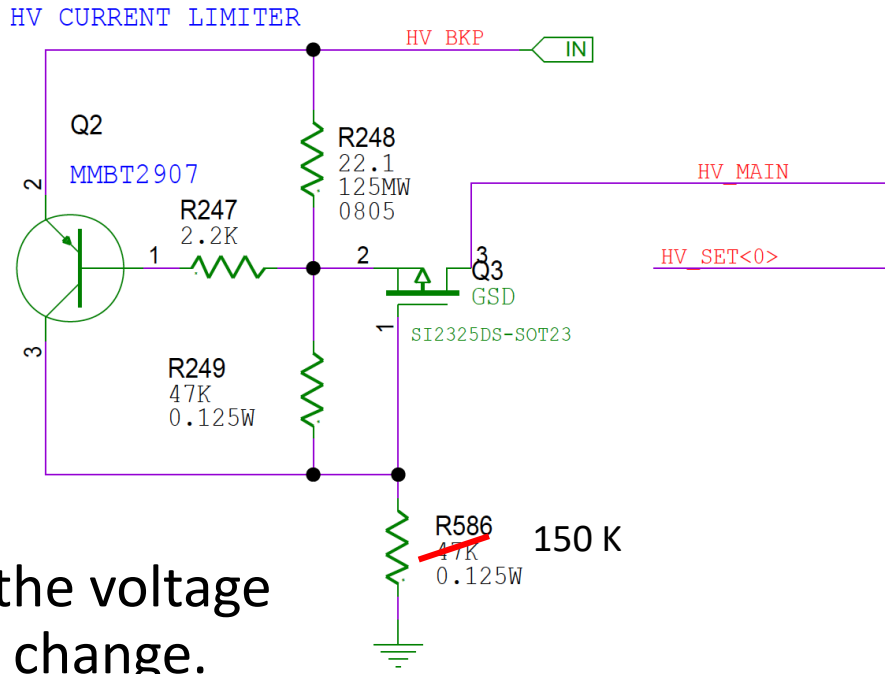


Hardware test: HV current limiter

- We want to make sure that the resistor in the current limiter circuit is 150KΩ.
  - $|V_{gs}| < 20$ V to not damage transistor
- The GS threshold voltage is between -2.5 and -4.5 V
- V_{GS} is computed as (given R=R586):

$$V_{GS} = V_{PS} \cdot \left(\frac{R}{(47+R+0.022)} \right) - \left(V_{PS} \cdot \frac{(47+R)}{(47+R+0.022)} \right)$$

V_{PS}: voltage set on Power supply

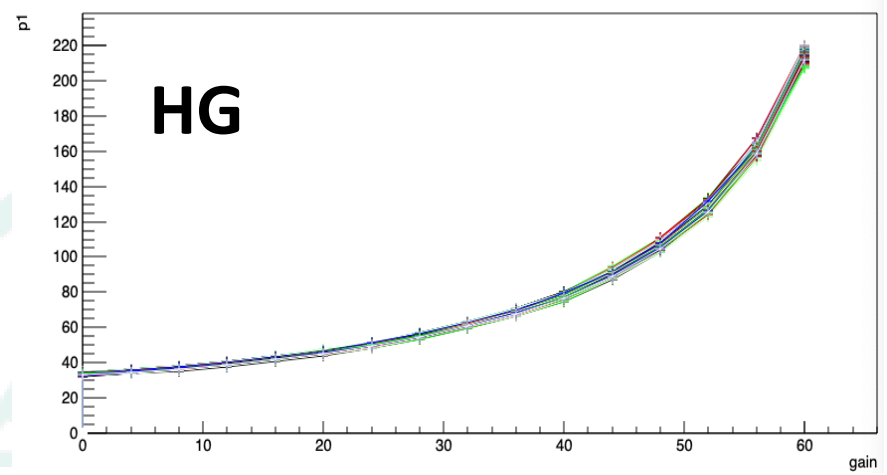


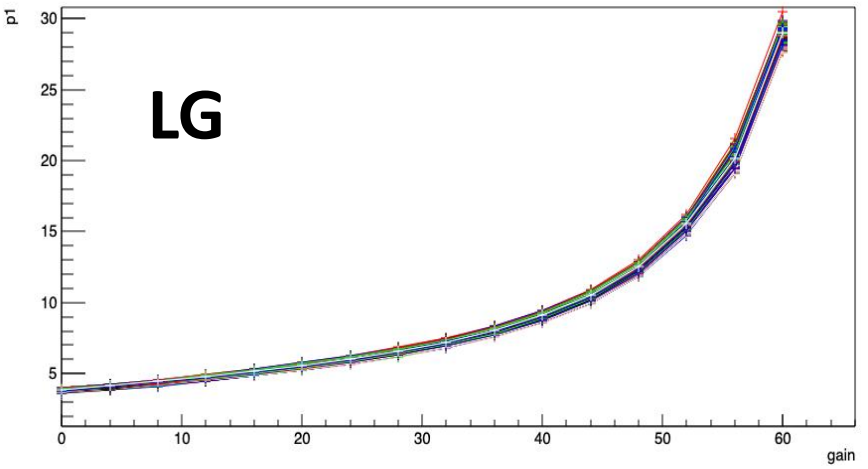
- For the same V_{PS} , if the resistance changes, the voltage applied on the GS terminals of the transistor change.
- With higher R, the V_{PS} necessary to enable the transistor is higher

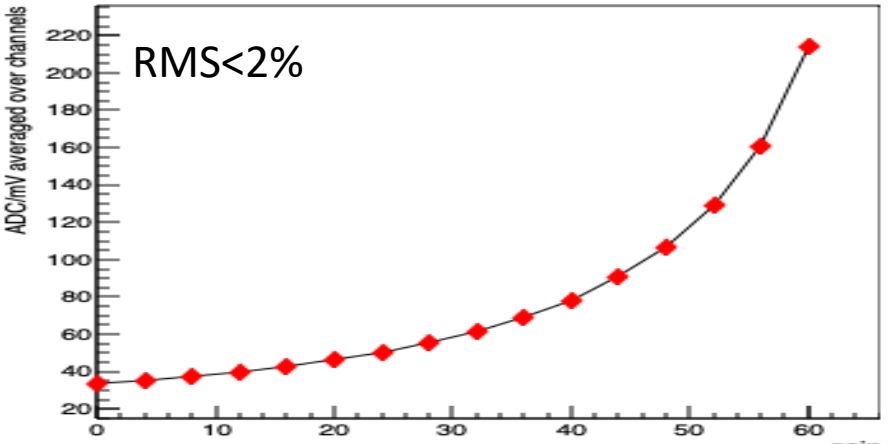
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min.	**Typ.**	**Max.**	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = - 250 µA	- 150			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2.5		- 4.5	

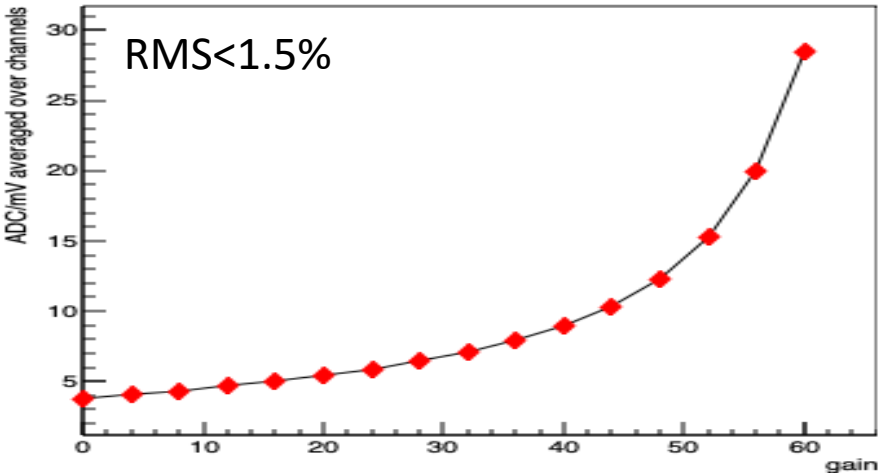
Gain uniformity

- Measured gain (ADC/mV) for all 256 FEB channels

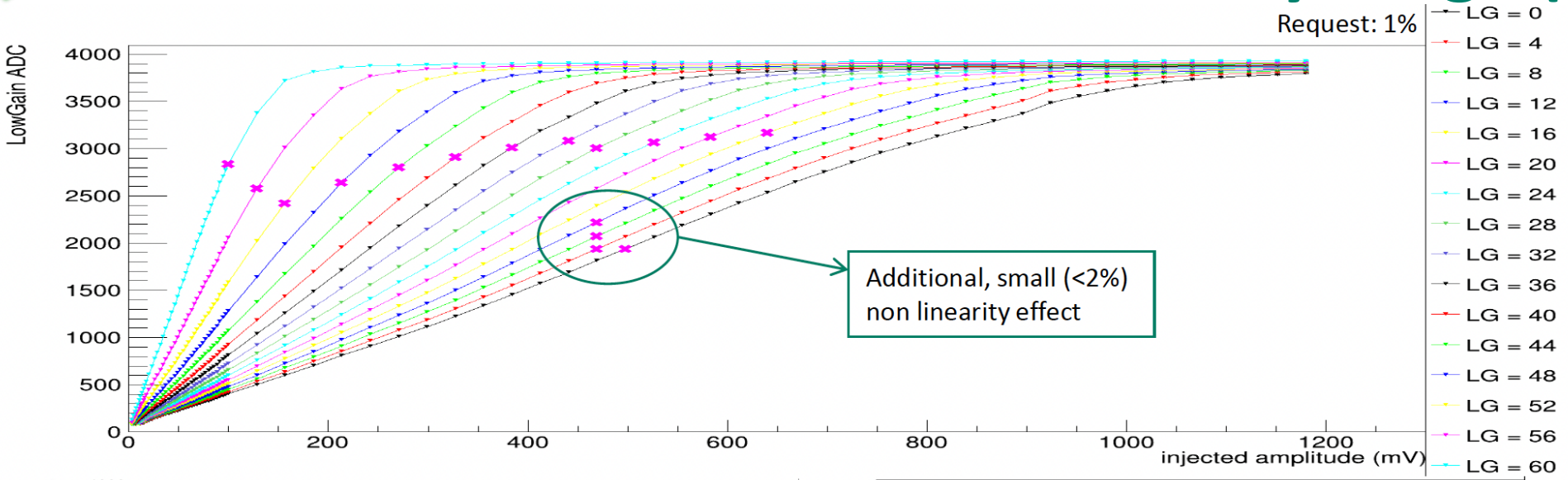


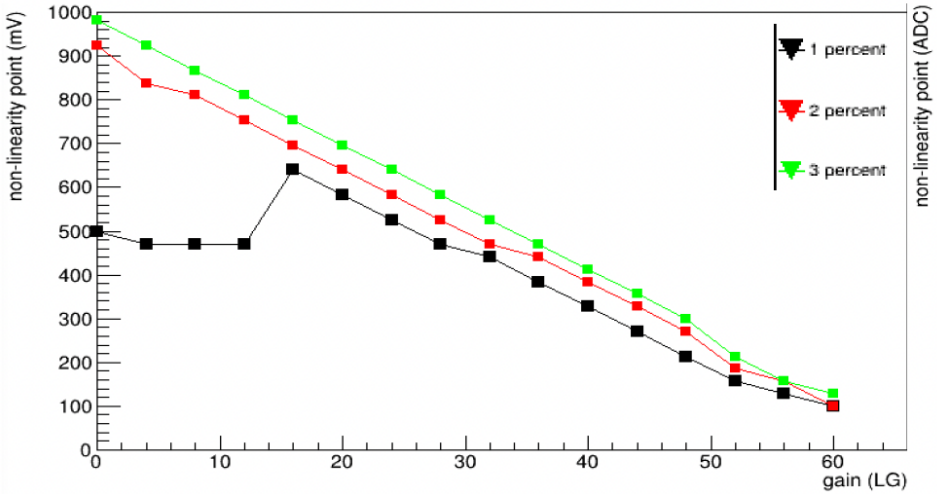


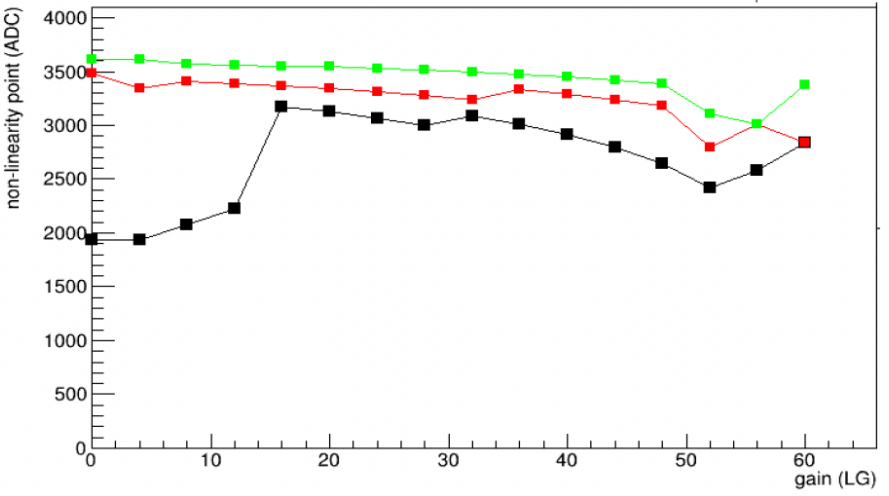




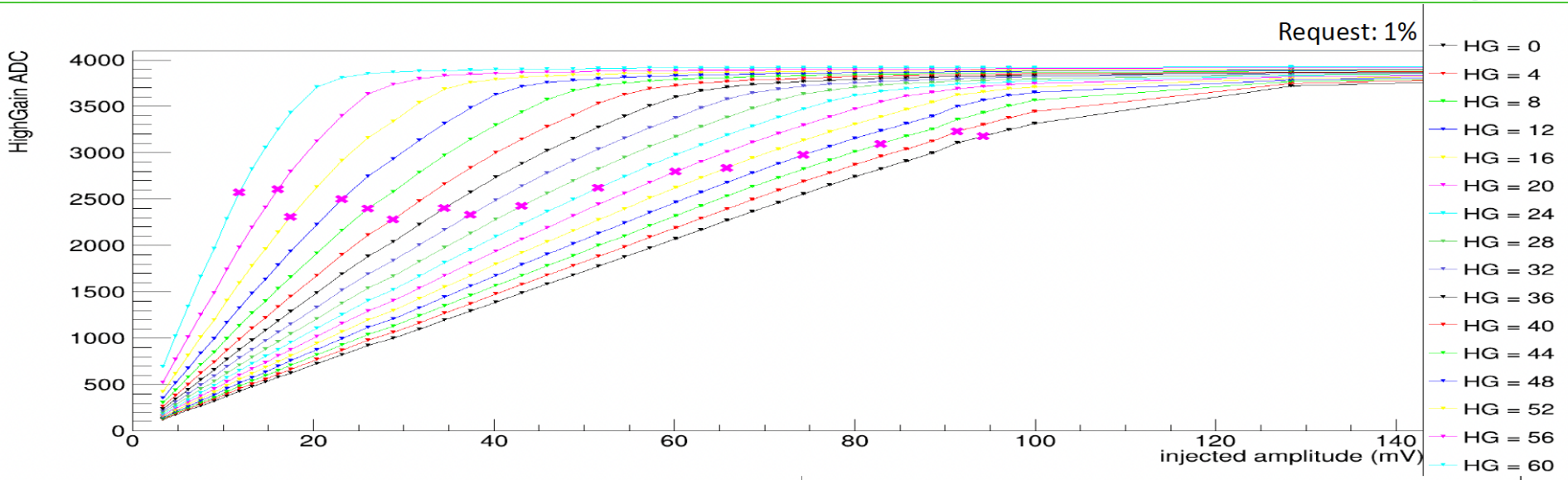
Linearity range (LG)

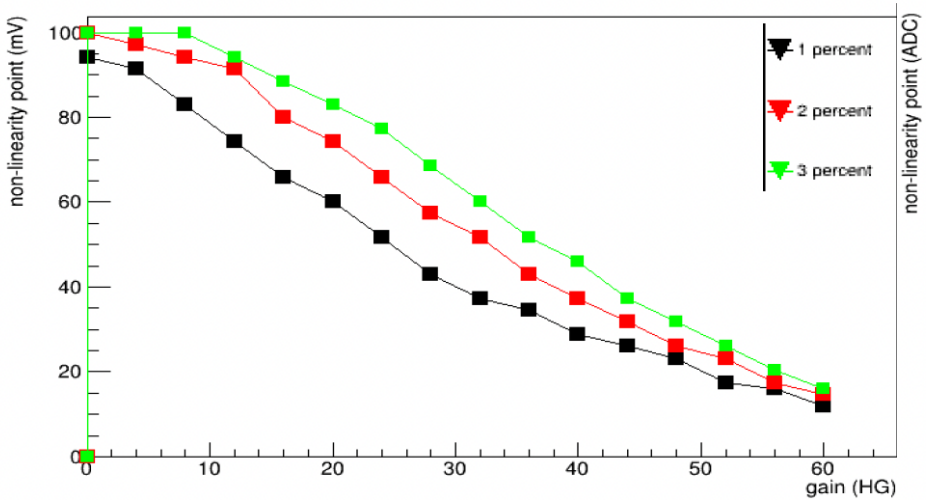


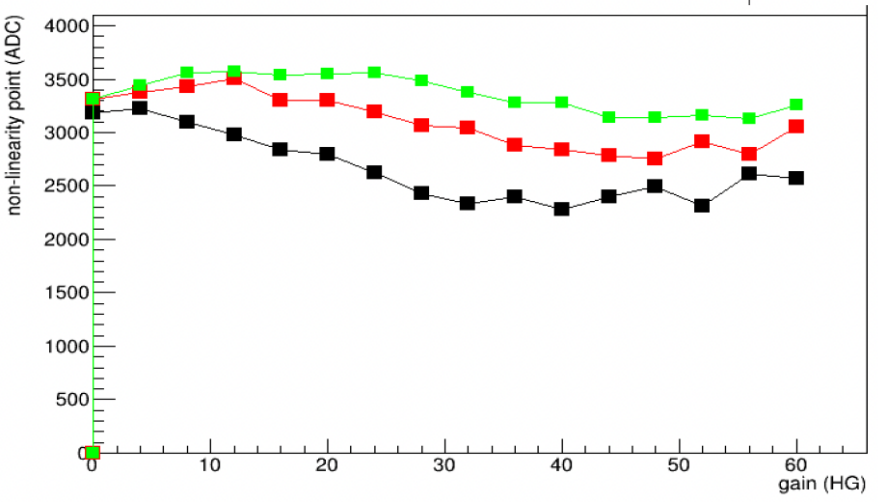




Linearity range (HG)



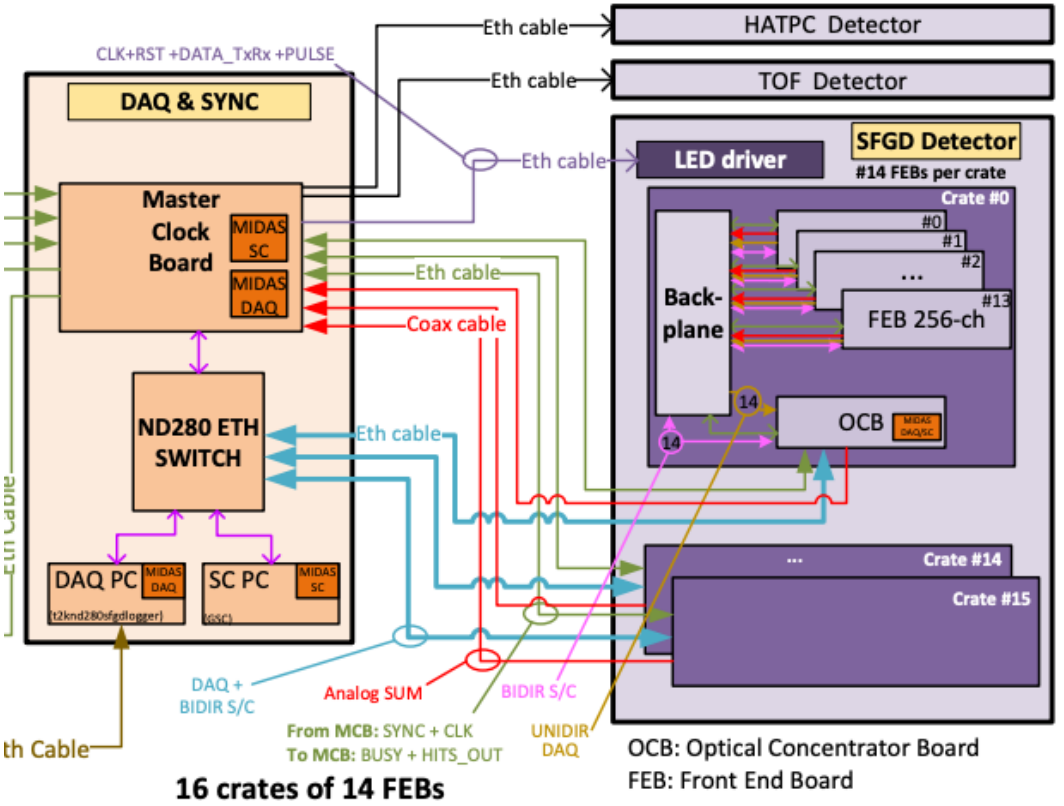




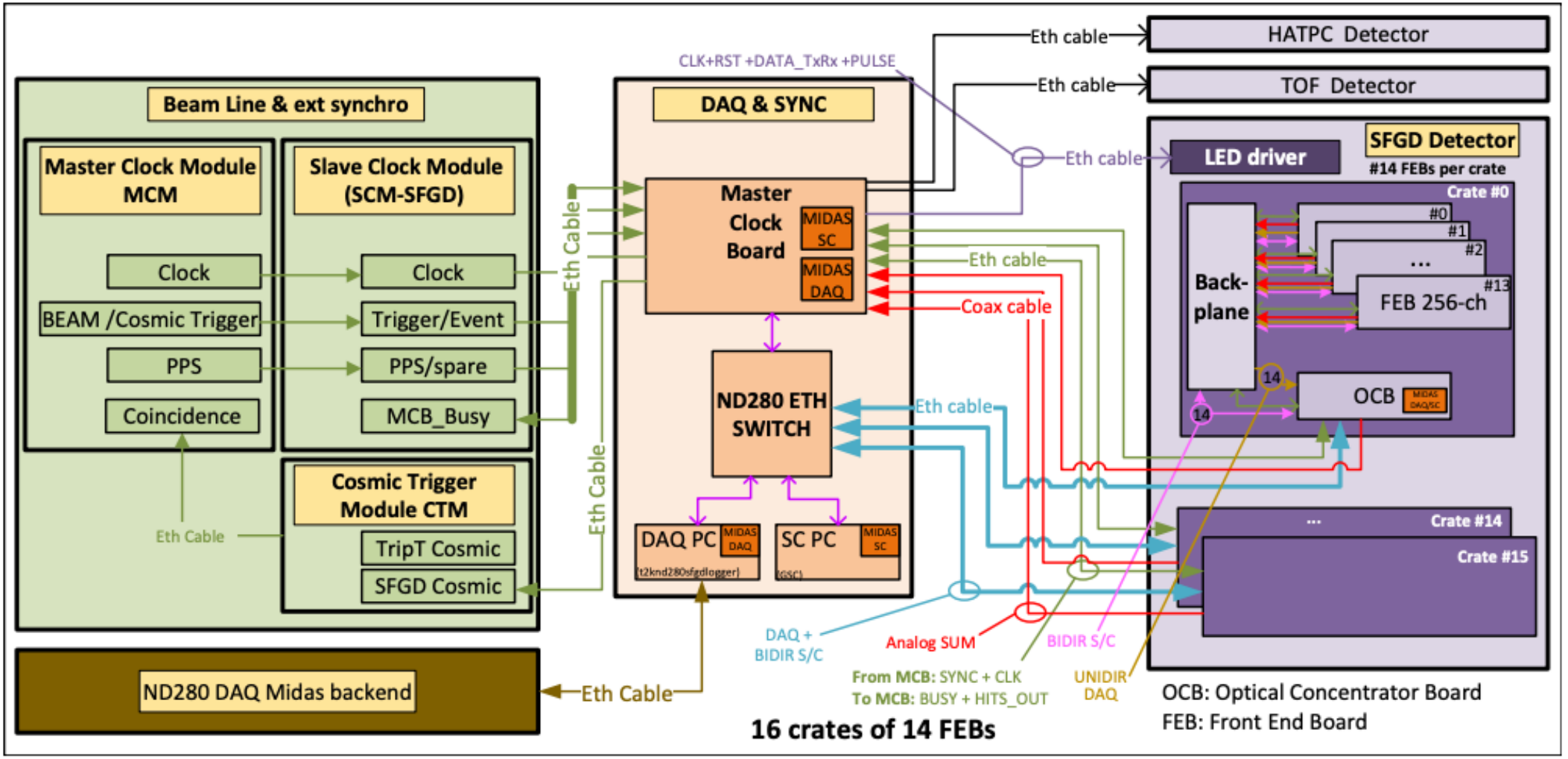
Electronics overview

16 crates – 14 FEBs per crate – 256 read out channels per FEB

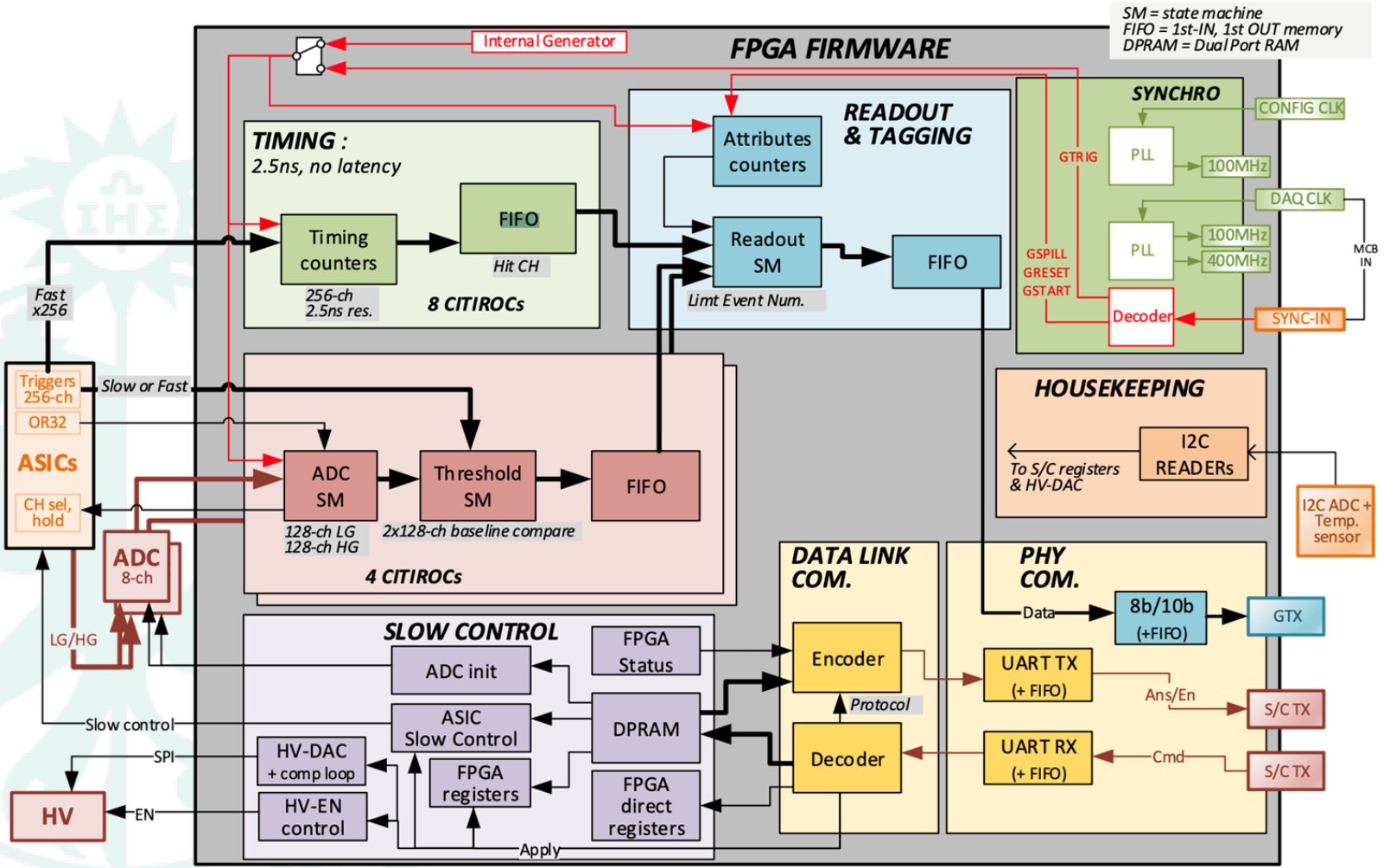
- Master Clock Board (MCB):
  - → CLK, SYNC to OCB
- Optical Concentrator Board (OCB)
  - → CLK, SYNC to FEB
  - ← Data from FEB
    - → Data to DAQ PC
  - ⇆ S/C to and from FEB
- Front-end Board (FEB)
  - ← CLK, SYNC from OCB
  - → Data to OCB
  - ⇆ S/C to and from OCB
- Backplane:
  - OCB-FEB interface and power distribution



OVERVIEW: 16 crates – 14 FEBs per crate – 256 read out channels per FEB



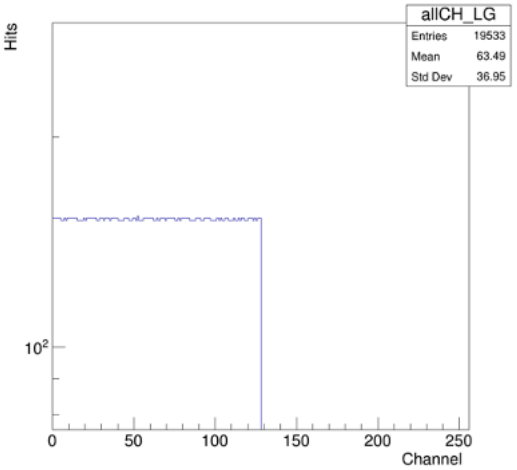
Firmware


SM = state machine
FIFO = 1st-IN, 1st OUT memory
DPRAM = Dual Port RAM
FPGA FIRMWARE
Internal Generator
TIMING :
2.5ns, no latency
Timing counters
256-ch
2.5ns res.
FIFO
Hit CH
8 CITIROCs
READOUT & TAGGING
Attributes counters
Readout SM
Limt Event Num.
FIFO
SYNCHRO
CONFIG CLK
GTRIG
PLL
100MHz
DAQ CLK
PLL
100MHz
400MHz
MCB IN
GSPILL
GRESET
GSTART
Decoder
SYNC-IN
Fast x256
Triggers 256-ch
OR32
ASICs
CH sel, hold
Slow or Fast
ADC 8-ch
LG/HG
ADC SM
Threshold SM
FIFO
128-ch LG
128-ch HG
2x128-ch baseline compare
4 CITIROCs
HOUSEKEEPING
To S/C registers & HV-DAC
I2C READERs
I2C ADC + Temp. sensor
DATA LINK COM.
Encoder
Protocol
Decoder
PHY COM.
Data
8b/10b (+FIFO)
GTX
UART TX (+ FIFO)
Ans/En
S/C TX
UART RX (+ FIFO)
Cmd
S/C TX
SLOW CONTROL
ADC init
FPGA Status
ASIC Slow Control
DPRAM
HV-DAC + comp loop
FPGA registers
FPGA direct registers
HV-EN control
Slow control
SPI
HV
EN
Apply

Example of “FW fix”

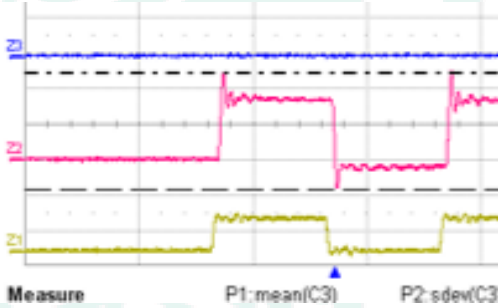
- Problem: CITIROC (group 1) configuration fails
- Cause: reflections on the ROC-FPGA bidirectional level translator
  - Due to change in design between FEB v1 and v2
- Solution: increase current on FPGA pin out
  - Design improvement in v3 (adding capacitor, change level translator)

QC test symptom:

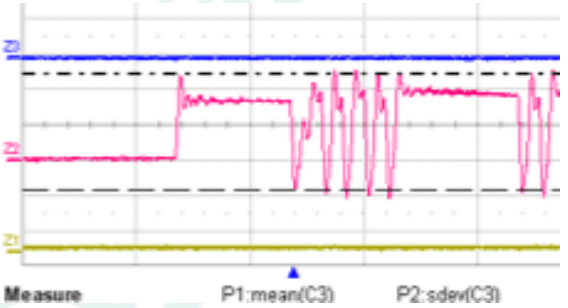


Test S/C signal:

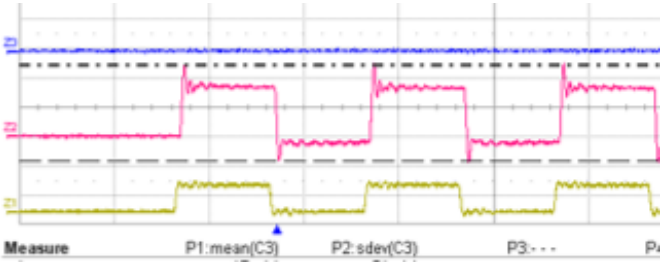
Normal behavior



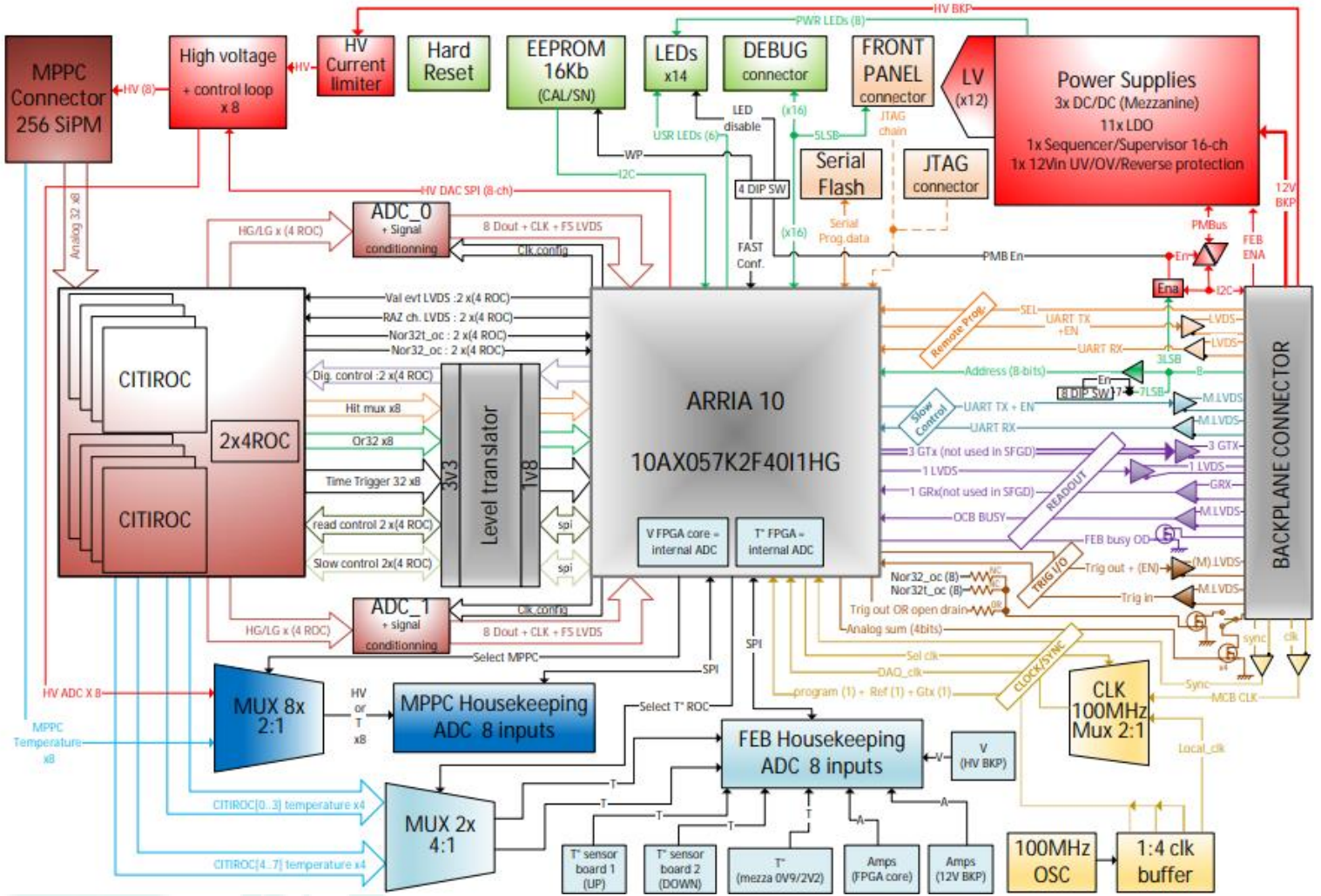
Faulty FEB



4 mA on FPGA pin-out:



FEB architecture



Typical light yields in SFGD