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Performance tests and hardware qualification of the FEBs for the novel Super-Fine Grained Detector of T2K Phase II

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T2K is a long baseline neutrino experiment, entering Phase II with a Near Detector upgrade.
A challenge of T2K Phase II is the development and testing of the Front-end electronics boards (FEB) for the read-out of the Super-FGD, new active tracking neutrino target. We hereby present the performance tests confirming that the FEB aligns with design requirements, and the hardware qualification of 243 FEBs through a custom QC test bench designed to detect and locate hardware failures. Complete installation in the detector took place in March 2024, one year after the beginning of the FEB mass production.
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Summary (500 words)

The Super-Fine Grained Detector (Super-FGD) is the new active neutrino target of the T2K Near Detector (ND280). It consists of nearly 2 million scintillating cubes (182 x 56 x 192) traversed by optic fibers and read by MPPC arrays on the outer surface of the detector, allowing 3D tracking. This innovative design capitalizes on the granularity and mass of its 2 million optical units (the cubes) while utilizing 55,888 read-out channels.
The read-out electronics is organized in 16 crates of 14 highly-integrated Front-End Boards (FEB hereafter) each. The crates are located inside the UA1 magnet, imposing space limitations. In total, 222 FEBs are employed for the read out of the detector. Each FEB reads the signal of 256 MPPCs using 8 CITIROC read out chips [1]. The CITIROC provides double analog (low-gain and high-gain) and trigger time readout, with configurable gain and trigger threshold on 32 read-out channels. Two 8-channels/12-bits ADCs digitize high-gain and low-gain CITIROC outputs. On the FEB, an ARRIA X FPGA handles slow control operations, CITIROC configuration and data flow.
Several performance tests were carried out to validate the FEB design against the detector requirements. The dynamic range requirement is 2000 photoelectrons, and it's limited by the non-linearity of the digitized FEB response. This has been demonstrated to meet requirement, with low-gain output providing linear response up to 2500 photoelectrons (Figure 1) with typical gain settings. Furthermore, studies have demonstrated that the dynamic range of high-gain mode reaches ~190 photoelectrons with SNR below 3%, aligning with the envisioned performances (Figure 2). Finally, the requirement for the electronics cross talk is to be negligible with respect to the optical cross-talk, estimated above 1 %. This requirement is also met, with electronic cross-talk measured to be below 0.4 % (Figure 3).
Following performance tests, the mass production and hardware qualification of 243 FEBs (10 % spares) started.
A custom Hardware Quality Check (QC) test bench has been developed to test every FEB with 100 % coverage of its components before detector assembly. The QC test bench consists of a compact tabletop arrangement, incorporating a general-purpose input-output board (GPIO), a demultiplexer board (Kaladin) for analog signal injection, and interconnected passive boards designed for easy insertion and removal of FEBs (Figure 4). The QC test examines each read-out channel for short and open

circuits, evaluates noise in each channel, verifies all slow control lines, and calibrates the temperature and voltage sensors on the FEB. Limits of 0.1 K and 15 mV are set for the standard deviation of temperature and voltage measurements to approve the board's hardware (Figure 5). The QC test faces the challenge of swiftly identifying hardware issues, such as missing or incorrect components and faulty soldering, across numerous boards within a limited time frame. The software automatically assesses the hardware quality giving hints on failure locations and generates a database containing comprehensive information for each board. The full QC process lasts 6 minutes per FEB.

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