Experiences and Lessons Learned from the End-of-Substructure card production of the ATLAS ITk Strip Upgrade

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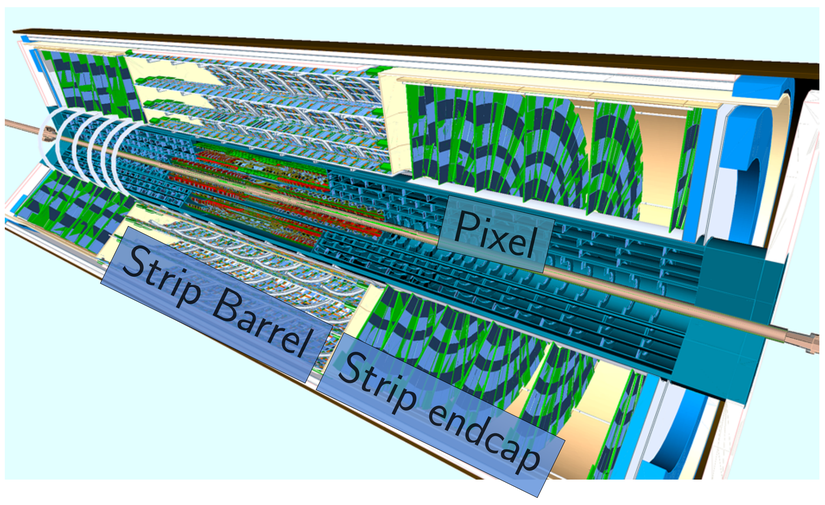
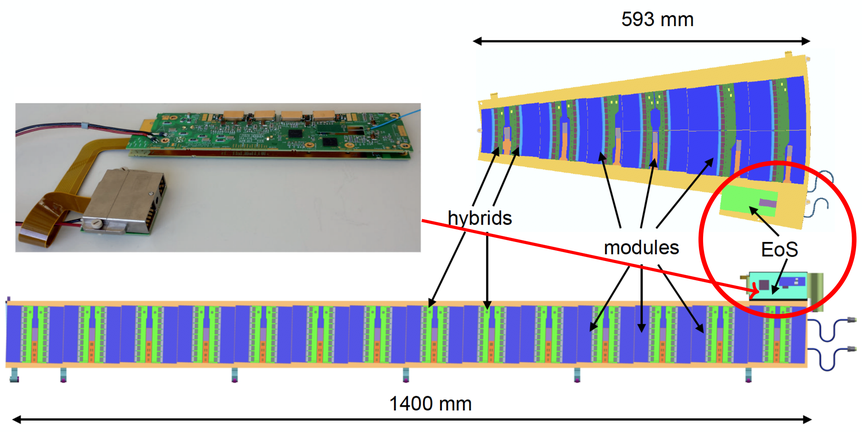
The ATLAS Inner Tracker (ITk)



Layout of the ATLAS ITk [1].

- **High-Luminosity LHC** (HL-LHC) upgrade planned for LS3 2026-2028
  ⇒ Increased pile-up (up to 200) and radiation damage
- ATLAS inner detector replaced by **Inner Tracker** (ITk)
- All-silicon detector with pixel and strip sensors
- Higher granularity, increased radiation hardness

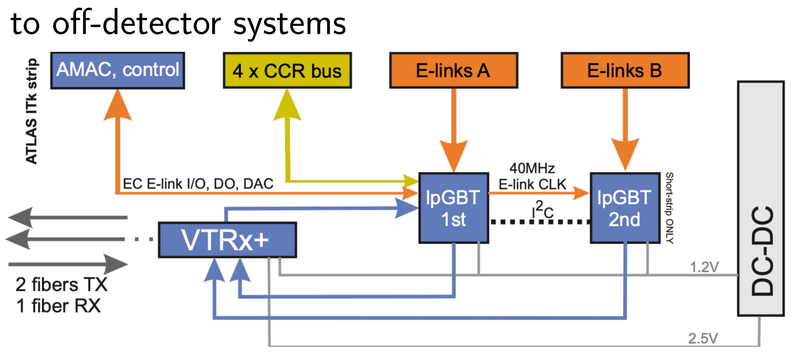


Layout of petals (top) and staves (bottom).

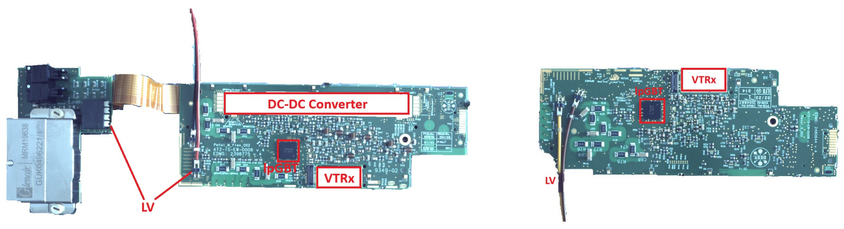
- Inner cylinder: Pixel system
- Outside: Strip system (ITk Strip)
  - 4 barrel layers built from **staves**
  - 6+6 endcap disks built from **petals**
  - Each stave/petal has a pair of **End-of-Substructure** (EoS) cards (main+secondary) for data, control and power connection to ITK Strip modules from outside detector

The End-of-Substructure Cards (EoS)

- 14+2 different EoS card flavours for Stave+Petal, ≈ 1600 cards in total (+ spares & preproduction)
- Power & HV distribution, data transmission, trigger and control
- Up to 14 differential pairs from modules and 10 Gbit s^{-1} optical links to off-detector systems

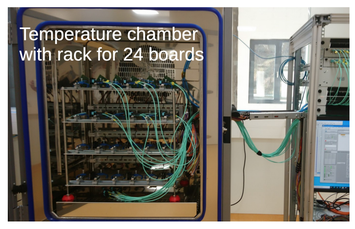


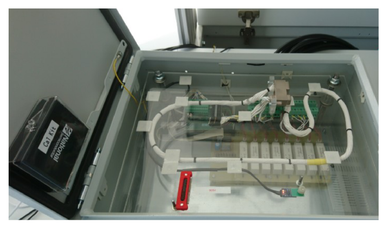
- **Low-power GigaBit Transceiver** (lpGBT) ASICs for data transmission, clock and control signals
- **Versatile Link PLUS (VL+) transceiver module** (VTRx+) for optical links
- 2-stage DC-DC buck-converters for 2.5 V and 1.2 V power supplies

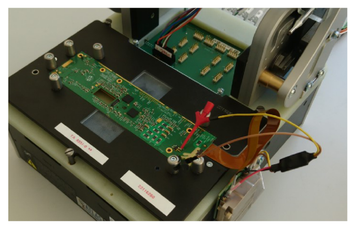


Pair of Petal EoS cards.

Quality Control (QC) Procedure







Testcoupons (CTCs):
- Resistance & Impedance, Bond-wire pull-test

Production workshop (DESY):
- Automatic Optical Inspection (AOI)
- Flying probe test: Impedance of each net

X-Ray images: at ISIT Fraunhofer Institute
- 3D X-ray of BGAs

Testbench 1: Reception test
- Database entry, Optical+IR imaging
- Flatness measurement, Basic electrical tests

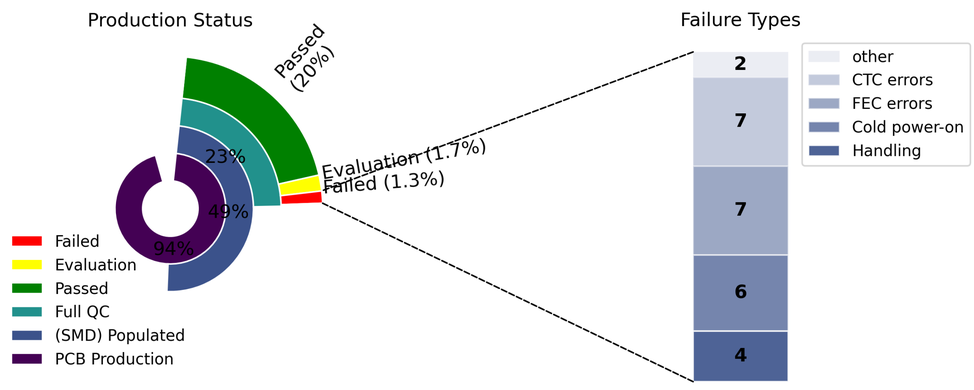
Testbench 2: Climate Chamber
- **10× at** −35 °C + **10× at** 25 °C
- Full function-test warm+cold

Testbench 3: High-voltage test
- Every HV line ramped to 1.1 kV, measure leakage current

Testbench 4: Needle Prober
- Needles under board connect to test-pads
- **Bit-Error-Rate-Test** (BERT) on all E-links
- Record **eye-diagrams** (up- & down-links)
- Reference voltage calibration

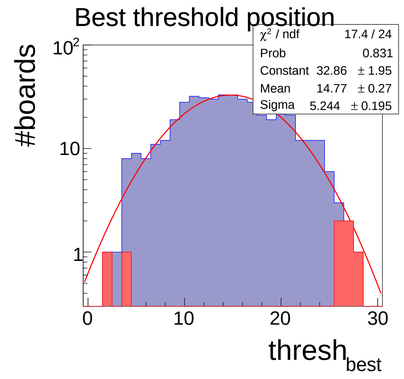
Production & QC Status

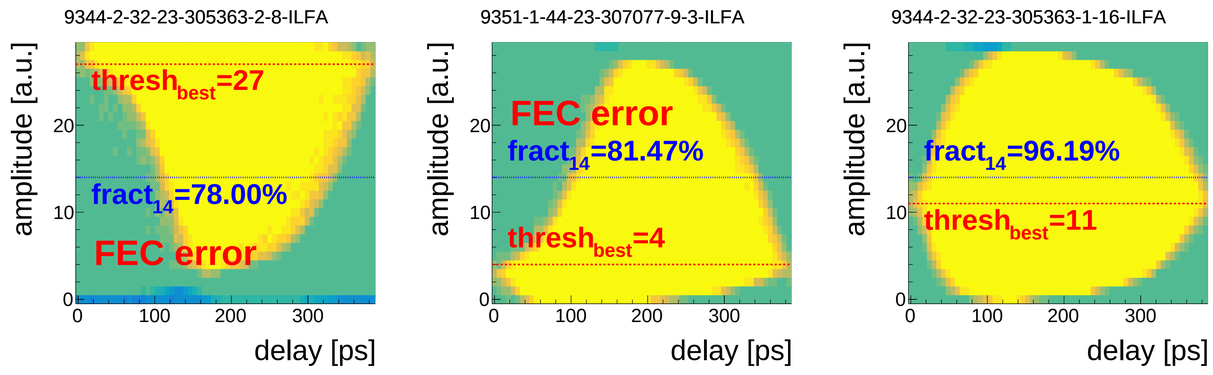
Production and QC Statistics:



lpGBT: FEC-errors within lpGBT:

- FPGA counts 64 bit-frames with erroneous checksum (CRC) *on* 10 Gbit s^{-1} *up-links*
- lpGBT has **forward-error correction** (FEC) counter *on* 2.5 Gbit s^{-1} *down-links* (256 bit-frames)
- 1.5 × 10^{12} frames tested
- Some EoS have **non-zero** FEC counter during BERT (TB4): $\mathcal{O}(10^0) - \mathcal{O}(10^4)$ **frames**
- Boards with FEC errors also have **asymmetric eye diagrams**





lpGBT: Cold failure: Reset of lpGBT:
- During cold tests (TB2): some lpGBTs not responding to reset command or any other signal

CERN-ASIC Group has confirmed both issues
EoS production is stopped, QC of already produced cards continues

Lessons learned

- Carefully designed QC essential to catch problems during production

References

[1] ATLAS Collaboration. *ATLAS Inner Tracker Strip Detector: Technical Design Report*. ATLAS-TDR-025; CERN-LHCC-2017-005. 2017.