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Status and Challenges of the ATLAS ITk Strip Tracker Powerboard Production for the End-Cap

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In preparation for the High-Luminosity-Upgrade of the Large Hadron Collider, new silicon strip detector modules need to be built for the ATLAS ITk strip tracker. The powerboard flexes in ITk strip modules are responsible for powering all readout electronics as well as controlling and monitoring module voltages, currents and temperatures. In total, about 6000 end-cap powerboards need to be assembled into functional modules. This contribution summarizes the latest status of the powerboard mass production performed at the University of Freiburg including developed setups, latest results from quality control measurements and the challenges encountered with varying flex quality in single batches.

Summary (500 words)

In preparation for the High-Luminosity-Upgrade of the Large Hadron Collider (LHC), new silicon strip detector modules need to be built for the ATLAS ITk strip tracker. For efficient detector operation, the strip modules need to achieve a noise occupancy of < 0.1% and a detection efficiency of at least 99% at a signal-to-noise ration of at least 10:1 throughout the full runtime of the High-Luminosity LHC. In the ITk end-cap, six different module geometries are used to achieve an optimal coverage for tracking. As the silicon strip sensors are manufactured on 6“wafers, the end-cap modules on the innermost three positions comprise one silicon sensor while the outermost three module positions use two. Due to the high costs of prototyping components in all six geometries, only the innermost geometry was properly exercised during the R&D phase. All other module geometries could only be prototyped as approximate versions using available sensor geometries and early versions of flexes.

Besides the silicon sensors, the ITk strip modules comprise flexes to hold the readout ASICs called „hybrids “and a dedicated „powerboard“flex used to power the whole module as well as to control and monitor voltages, currents and temperatures. With the first prototypes of all module geometries becoming available in 2022, an excessive noise beyond the design specifications was discovered for the outermost radii module geometries. The issue was traced back to a design weakness in all powerboard geometries and was succesfully fixed. To validate the new design [1], the first powerboard flexes were SMD populated by hand and assembled into modules in 2023. These modules showed noise levels within the specifications. Currently, an increasing number of industrially SMD populated powerboard flexes become available for module assembly as powerboard production is ramping up.

In parallel to these noise investigations, test setups and procedures needed to be developed at the University of Freiburg to perform the electrical quality control of fully assembled powerboards. In total, about 6000 end-cap powerboards need to be assembled and characterized at Freiburg during production. In one recent batch of powerboard production, voltage oscillations leading to high noise in modules were observed at the output of the bPOL chip. Detailed investigations are currently performed to understand this feature which is identified to be related to a low flex quality for one specific batch. The quality control procedures have been expanded by suitable tests to detect this behaviour further during production.

This contribution summarizes the latest status and challenges observed with the test setups and the test procedures at the University of Freiburg.

[1] https://indico.cern.ch/event/1255624/contributions/5443877/

Authors: SPERLICH, Dennis (Albert Ludwigs Universitaet Freiburg (DE)); KOPPENHÖFER, Roland (Albert Ludwigs Universitaet Freiburg (DE))

Presenter: KOPPENHÖFER, Roland (Albert Ludwigs Universitaet Freiburg (DE))

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