



Rad-Hard Readout System for Timepix3 Hybrid Pixel Detectors

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TWEPP 2024 Topical Workshop on Electronics for Particle Physics

The Beam Instrumentation PiXel (BIPXL) readout system allows the data acquisition and slow control of Timepix3 hybrid pixel detectors in high radiation environments.

It is employed in the Beam Gas Ionization (BGI) profile monitors at CERN for non-invasive, continuous measurement of the beam profile.

Content

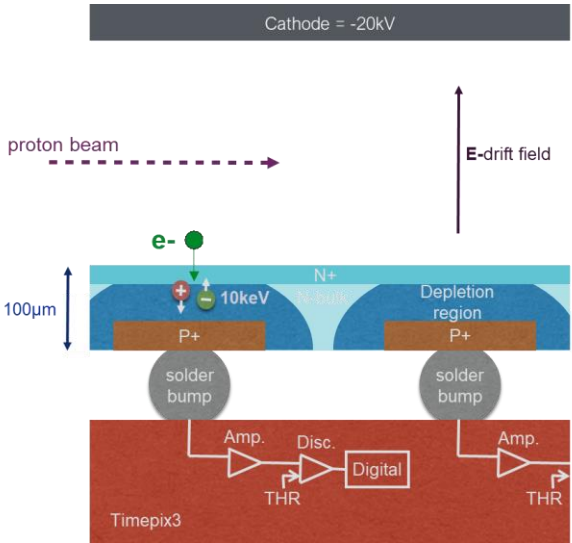
- **BGI overview**
 - Ionisation electron detection with Timepix3
- **BIPXL readout overview**
 - BIPXL Front-end and BGI connections
- **BIPXL front-end**
 - Front-end constraints
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- **Conclusions and future projects**

BGI Overview

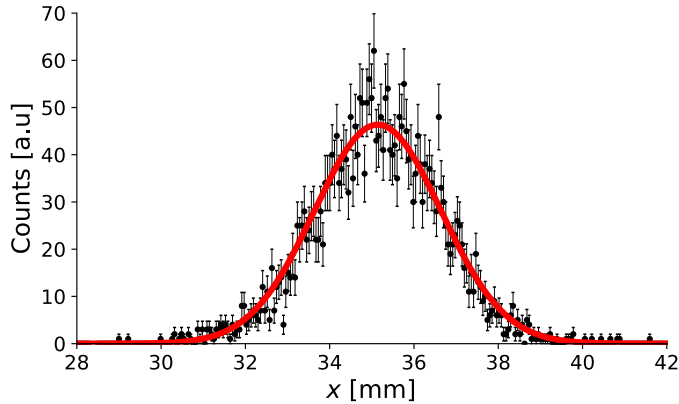
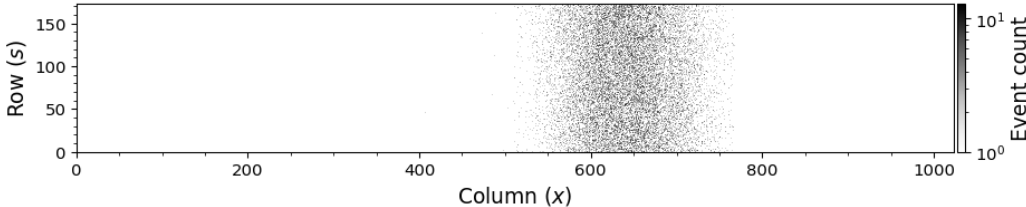
Instrument description and ionisation electron detection principle

Ionisation electron detection with Timepix3

- **Timepix3 Hybrid Pixel Detector:** 256 x 256 array of 55 μm x 55 μm pixels.
- **Signal > Threshold \rightarrow Event:**
 - Pixel position \rightarrow Where ($\sigma_{\text{position}} < 16 \mu\text{m}$)
 - Time of Arrival (ToA) \rightarrow When ($\sigma_{\text{time}} = 1.6 \text{ ns}$)
 - Time-Over-Threshold (ToT) \rightarrow \sim Energy



- **Create the beam profile by counting ionisation electrons detected in each column.**



BIPXL Readout Overview

Front-end and Back-end concepts and connections overview.

BIPXL readout: F-E and B-E

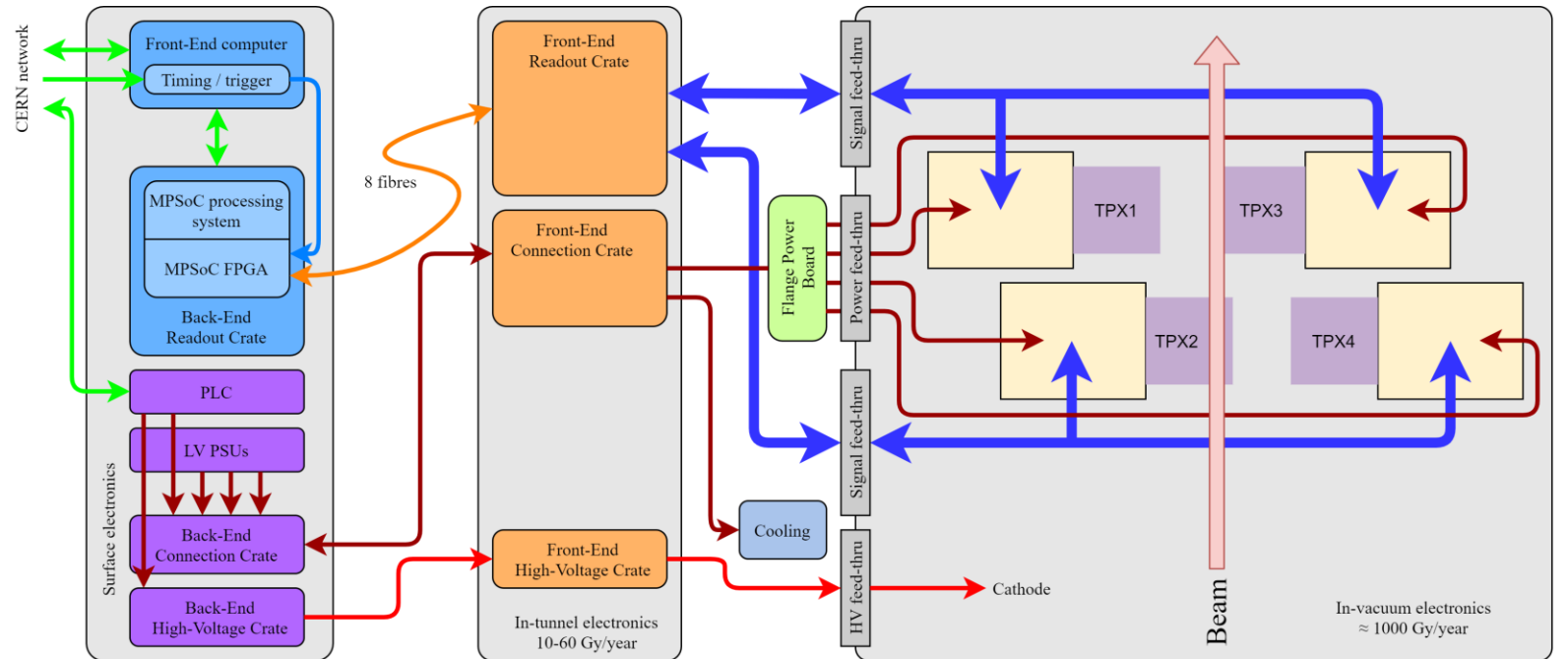
- **The BIPXL readout system handles:**
 - 4 x 8 Timepix3 output signals at 320/640 Mbit/s (10.24/20.48 Gbit/s upstream).
 - 4 x 6 Timepix3 control signals at 80 Mbit/s (1.92 Gbit/s downstream).
- **Since the BGI instruments are integrated into the accelerators with the Timepix3 detectors inside the beam pipe (exposed to radiation):**
 - The selected COTS processing systems must be located far from radiation areas.



- **The BIPXL readout is divided into “**Readout Front-end**” (electronics under radiation) and “**Readout Back-end**” (electronics outside the radiation area).**
 - Communicated by optical signals (SM).

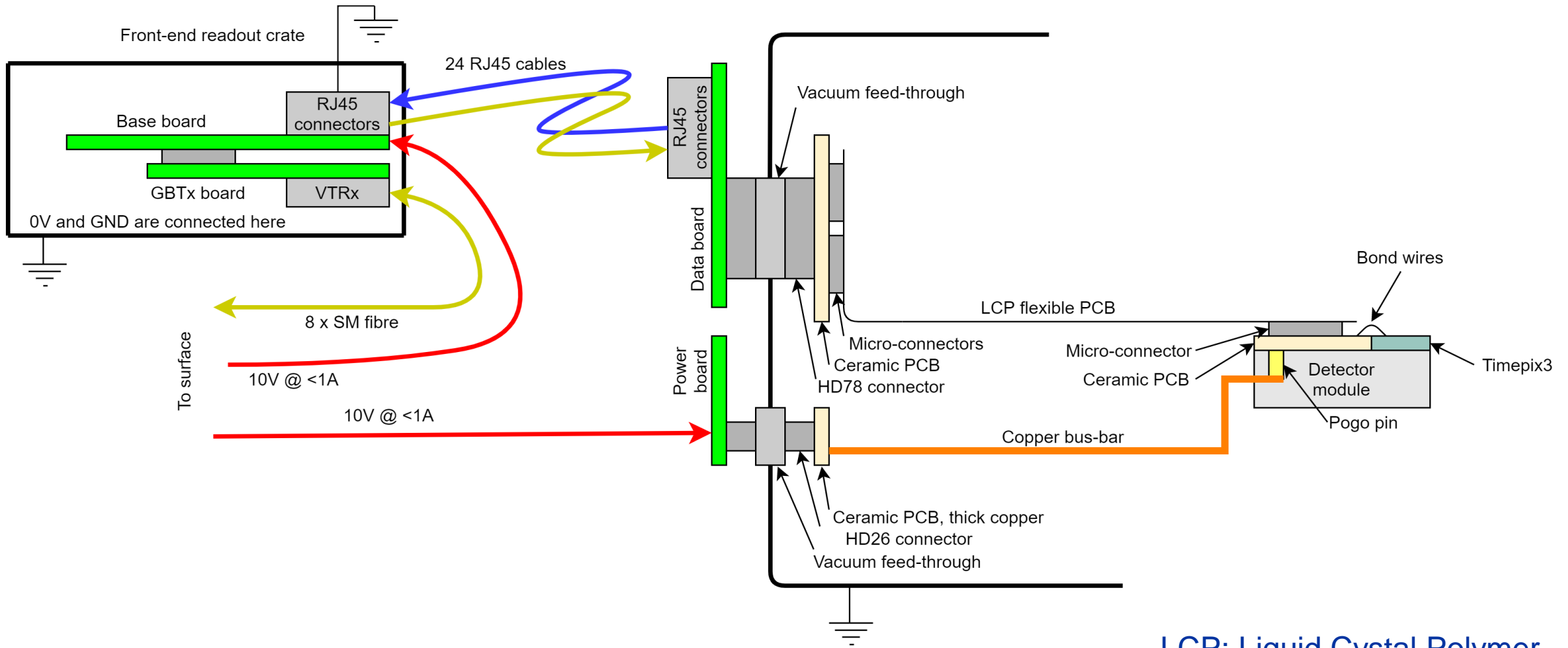
BIPXL readout overview

- **Detectors – front-end** → 32 Cat6A cables (RJ45 terminations).
- **Front-end – back-end** → 8 Optical fibres (SM).
- **Back-end** → Xilinx MPSoC (Zynq Ultrascale+, ZCU102)
 - Programmable Logic: more-time critical and data intensive tasks such as bit manipulation and trigger handling.
 - Processing System: running Petalinux with applications for the processing of the coming data.



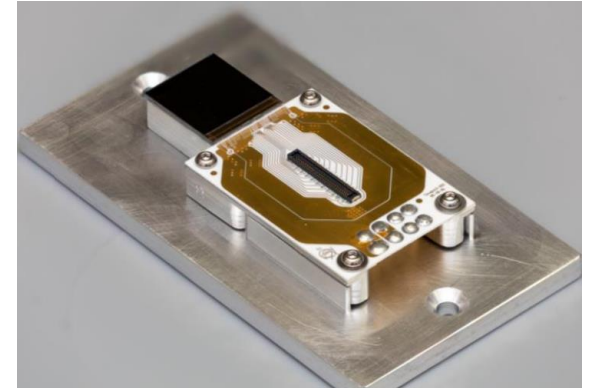
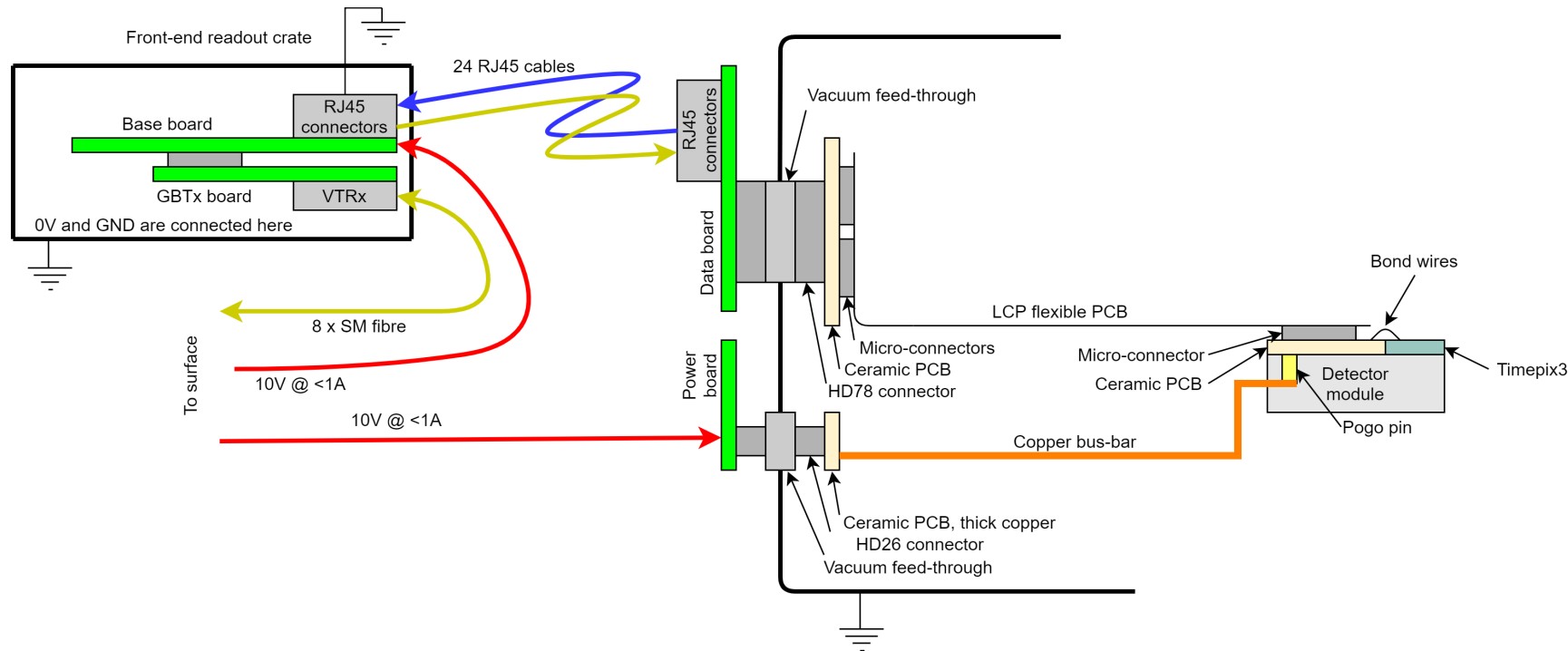
Non-destructive beam profile measurements with an Ionisation Profile Monitor (IPM) based on Timepix3&4 Hybrid Pixel Detectors (HPDs) - IBIC 2024 - Mark McLean

BIPXL Front-end and BGI connections



LCP: Liquid Crystal Polymer

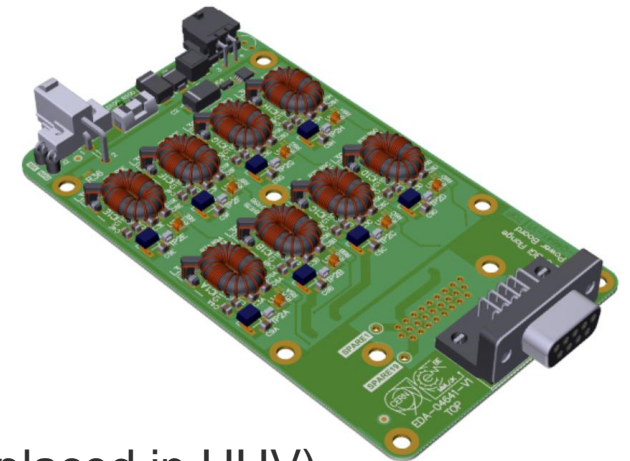
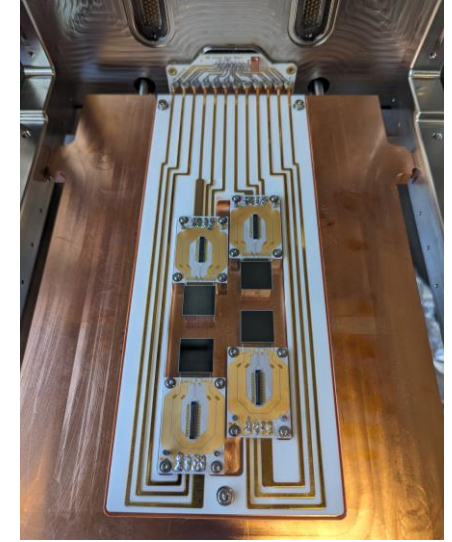
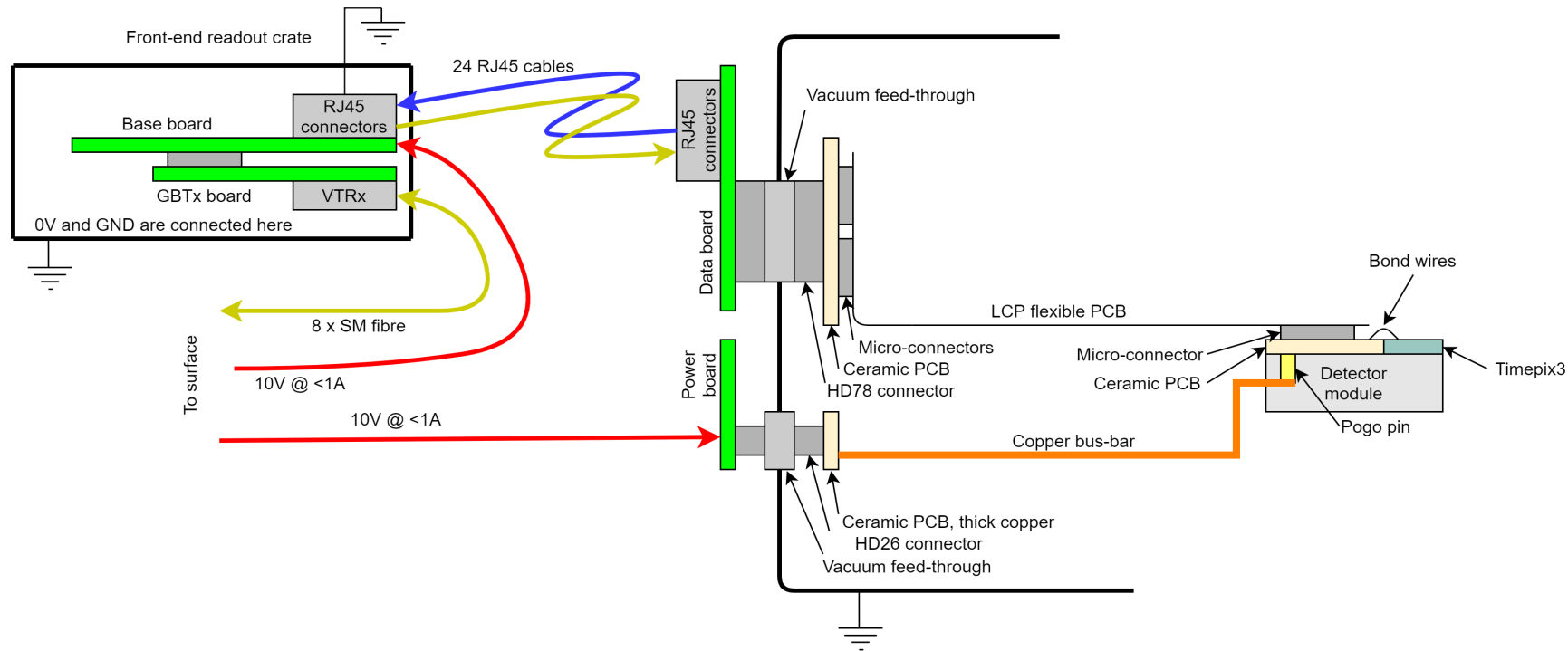
BIPXL Front-end and BGI connections



Timepix3 UHV modules

- Timepix3 attached to an aluminium base with Staystick (672).
- Ceramic thin-film PCB to fan out TPX3 control & data signals to Panasonic narrow pitch connector.
- Connect to DC power (mini-Cu busbars) via pogo-pins.

BIPXL Front-end and BGI connections



Timepix3 DC power:

- bPOL DC/DC converters on the air side of the vacuum flange (they cannot be placed in UHV).

BIPXL Readout Front-end

Constraints, prototypes and current design

Front-end design constraints

The design requirements for the Front-end have been:

- Proximity to the beam → radiation hard design.

4 RPL Dosimeters (CR-136545) measured in March 2023

	Dose (Gy)
PS-BGIH Flange electronics	696
PS-BGIH Front-end electronics	10,5
PS-BGIV Flange electronics	427
PS-BGIV Front-end electronics	53

- Low access to the system (only during technical stops) → reliable design + diagnostics.
- High speed signals → signal integrity for optimal system performance.

BIPXL Front-end prototypes

GBTx: Gigabit Transceiver
VTRx: Versatile Transceiver
GEFE: The Giga Bit Transceiver based Expandable F-E

GEFE Board (2016)

- No radiation-tolerant board met TPX3 data rate needs.
- **Designed at CERN: ProASIC3E FPGA and GBTx chip (3.2 Gbit/s).**
- Initial TPX3 tests despite data rate constraints.

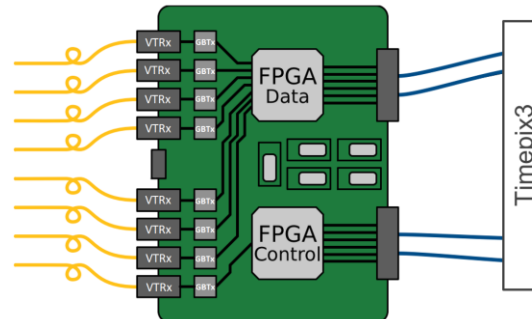


BIPXL Front-end prototypes

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GEFE: The Giga Bit Transceiver based Expandable F-E

GEFE Board (2016) → FPGA based Front-end (2018)

- No radiation-tolerant board met TPX3 data rate needs.
- **Designed at CERN: ProASIC3E FPGA and GBTx chip (3.2 Gbit/s).**
- Initial TPX3 tests despite data rate constraints.
- Custom F-E board to achieve 20.48 Gbit/s data rate:
 - 8 GBTx + 8 VTRx transceivers
 - ProASIC3 and Kintex-7 SRAM-based
- **After two operational years, the FPGAs, mostly the Kintex-7 became unreliable.**



BIPXL Front-end prototypes

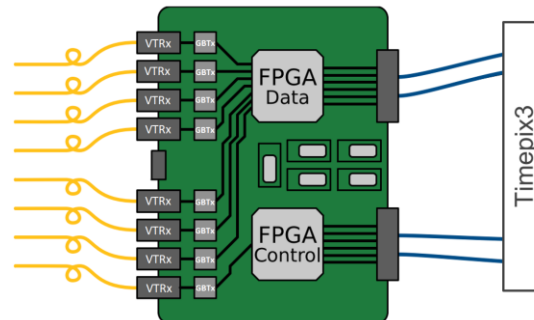
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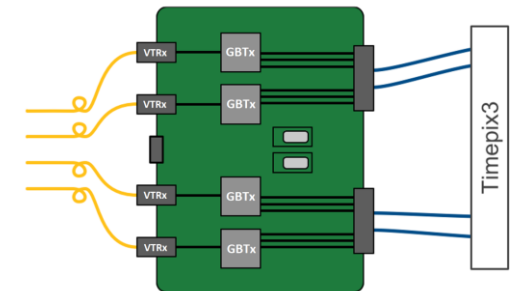
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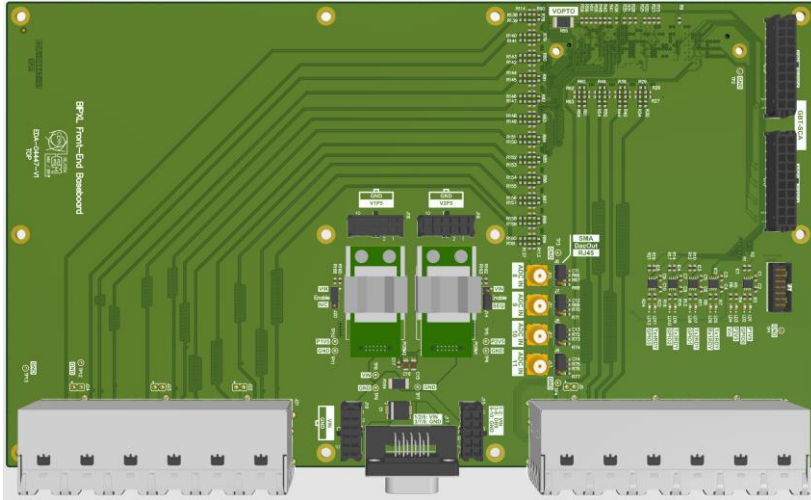
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- **Radiation hard design:**
 - The two FPGA were removed.
 - Data rate reduced from 640 Mbit/s to 320 Mbit/s.
 - Direct connection of the Timepix3 signals to the GBTx e-Links.
 - Kintex-7 and ProASIC3 HDL logic moved to the Back-end MPSoC.



Current front-end design



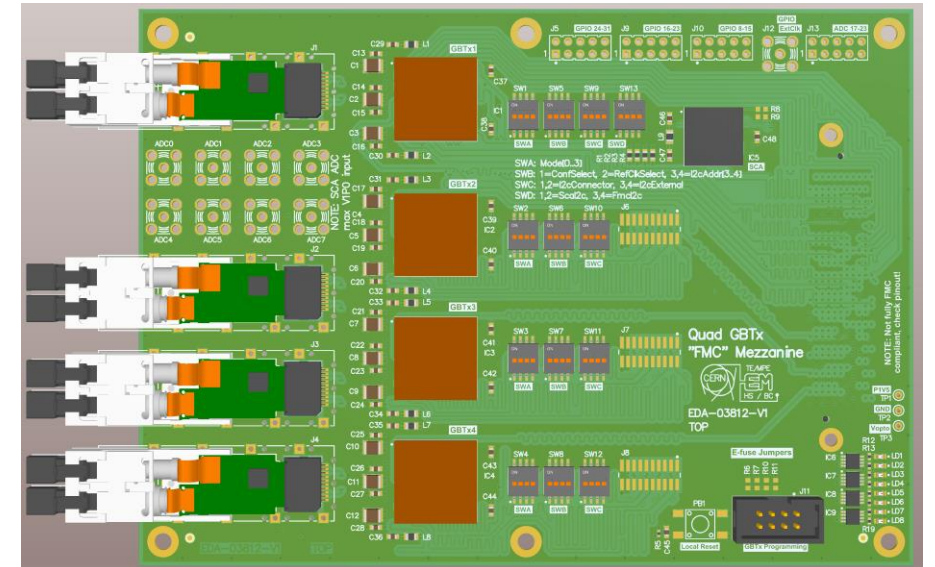
Two boards connected via an FMC HPC connector

Front-end baseboard:

- 24 RJ45 connectors
- Four SMA as ADC inputs
- Two FEASTMP DC/DC modules (1.5V for the GBTx chips, 2.5V for the VTRx transceivers).

Quad GBTx Mezzanine board

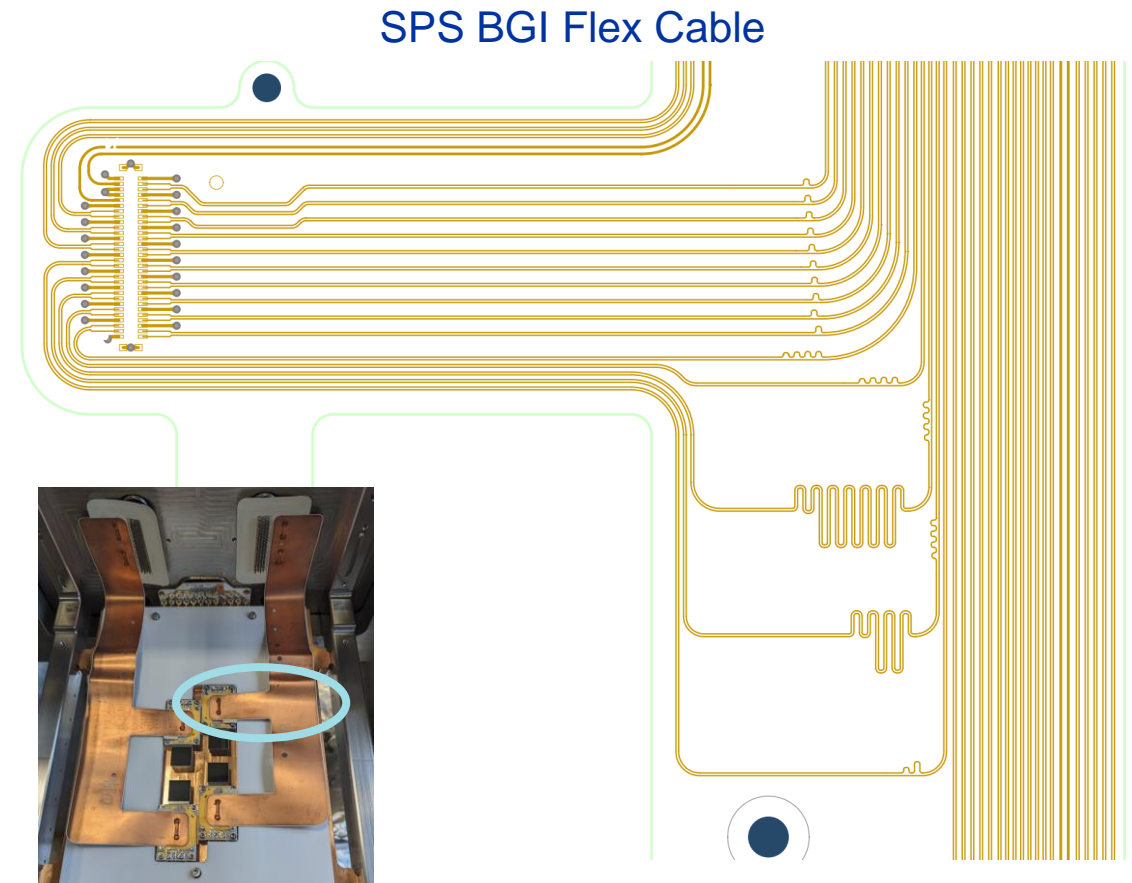
- Four GBTx chips for the data serialize-deserialize (one main chip) with four VTRx transceivers.
- 32 e-links at 320 Mbit/s as uplinks and 24 e-links at 80 Mbit/s at downlinks.
- Adjustable phase alignment of the input e-links.
- 40 MHz reference clock received from the Back-end.
- GBT-SCA (digitization of the bias currents).



Current front-end design

- **Custom-designed components at CERN for radiation-hard environments** using RHBD techniques like Triple Modular Redundancy and latch-up protection.
- **Length Matching:** differential signals are precisely length-matched to ensure signal integrity within each pair.
- **Adjustable Phase Aligners:** GBTx eLink inputs compensate for signal cable length variations.
- **Uniform Lengths:** Shutter and T0_Sync signals must be uniform across all Timepix3 devices for consistent operation and synchronized time stamping.

Maximum radiation levels of the BIPXL front-end components	
VTRx (SM)	Up to 50 Mrad (0,5 MGy)
GBTx	Up to 100 Mrad (1 MGy)
FEASTMP	150- 200 Mrad (1,5 – 2 MGy)



Horizontal PS-BGI and Front-end



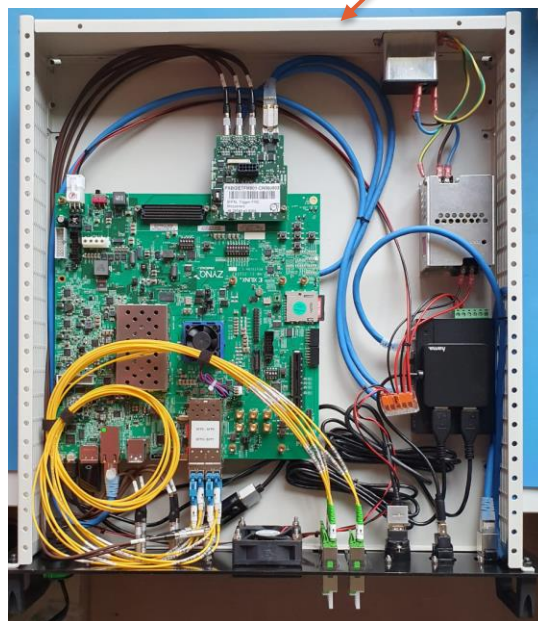
Front-end 2U crate



Back-end, PLC and power supplies



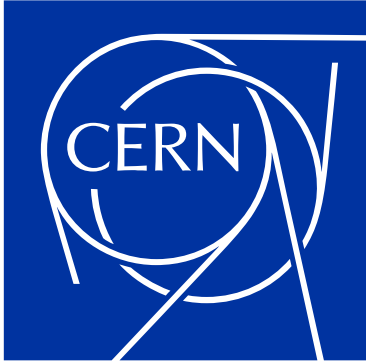
Back-end 2U crate



Conclusions and future projects

- **The BIPXL readout characteristics make it suitable for future application of Timepix3 for beam instrumentation in high radiation areas like**
 - HL-LHC BGI profile monitor.
 - North Area telescope for bent crystals characterization.
 - Beam Loss Monitor (BLM) for rapid deployment in the LHC.
- **They might imply the use of the Timepix4: 16 outputs at 10.24 Gbit/s**
 - Readout modifications:
 - High-speed PCB material
 - Low power GBT (IpGBT)
 - VTRx+ (SM)
 - bPOL12V

Maximum radiation levels	
Component	Max. Radiation Levels
IpGBT	Up to 200 Mrad (2 MGy)
bPOL12V	150 Mrad (1,5 MGy)



home.cern

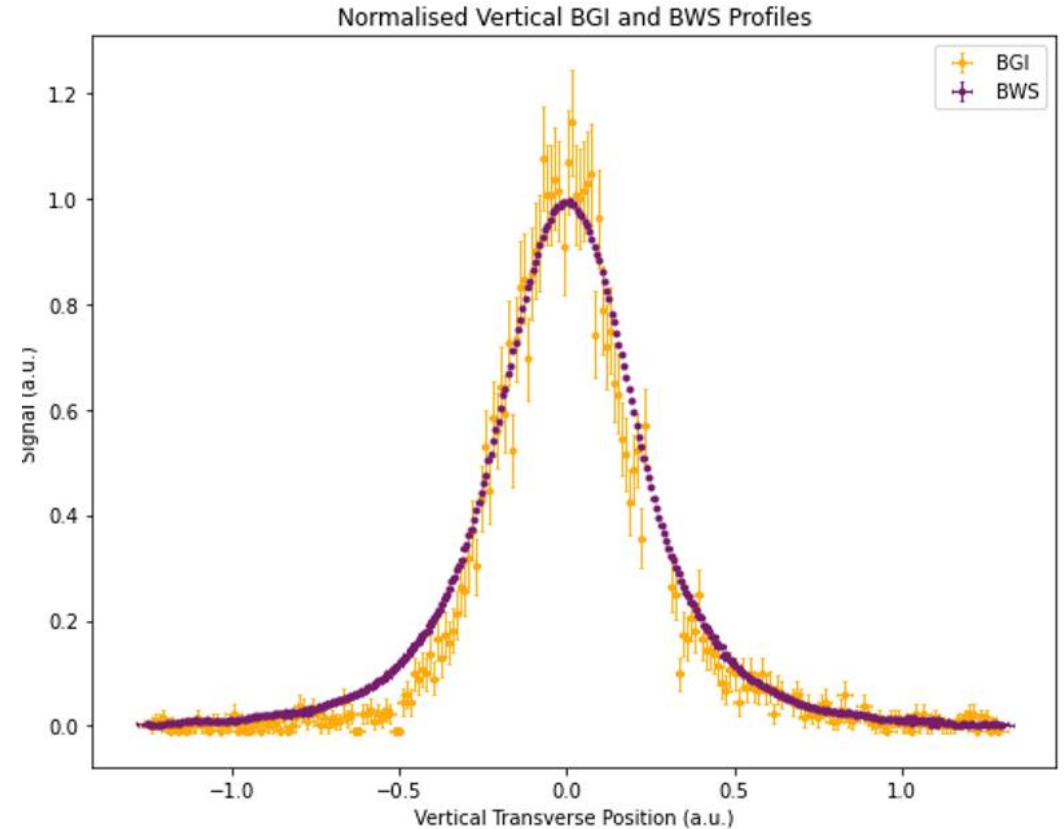
Spares

Acronyms

- **BGI:** Beam Gas Ionization profile monitor
- **BIPXL:** Beam Instrumentation PiXel
- **GBTx:** Gigabit Transceiver (electronic part)
- **VTRx:** Versatile Transceiver (optical part)
- **GBT-SCA:** GBT- Slow Control Adapter
- **MPSoC:** Multiprocessor System-on-Chip
- **MPSoC PS:** Processing System
- **MPSoC PL:** Programmable Logic
- **APU:** Accelerated Processing Unit
- **RPU:** Real-time Processing Unit
- **GEFE:** Gigabit Transceiver based Expandable Front-End
- **bPOL:** Point-Of-Load DC-DC converter
- **FESA:** Front-End Software Architecture
- **FEC:** Front-End Computer
- **LCP:** Liquid Crystal Polymer

Benchmarking Results

- During 2023/4 the PS-BGIs were compared with the wire-scanners.
- Data was collected from LHC-type beams at flat top with both PS-BGIs, without gas injection.
- The agreement in terms of normalized emittance is within 1 statistical sigma.



C. Fleisig et al., “Equalisation and Benchmarking of the Beam Gas Ionisation Profile Monitor”

GBTx overview

Information from the GBTx manual

- **130 nm CMOS rad-hard ASIC for high-speed optical links designed by CERN**
 - Bidirectional high-speed link at 4.8 Gbps
- **40 bi-directional e-ports (GBT Mode)**
 - Up to 40 @ 80 Mb/s
 - Up to 20 @ 160 Mb/s
 - Up to 10 @ 320 Mb/s
- **40 e-ports clocks programmable:** 40/80/160/320 MHz with fixed phase
- **Data phase alignment (dedicated PLLs):** automatic, semi-automatic or user controlled
- **Each e-port is physically associated with a specific set of bits in the data frame**
 - No front-end module address is needed
- **Electrical characteristics: drivers with SLVS signalling and receivers with SLVS/LVDS signalling**

- **Low power version of the GBTx chip**
 - Uplink:
 - 5.12 Gbps
 - 10.24 Gbps
 - Downlink: 2.56 Gbps
 - 4 programmable deskew clocks with 50 ps resolution
- **Design specifications**
 - 65 nm CMOS technology
 - ~200 Mrad total dose / SEE robust
 - 0.75W at 10.24 Gbps / 0.5W at 5.12 Gbps

Downlinks at 2.56 Gbps with FEC12

- BW: 160/320/640 Mbps
- e-ports: 28/14/7

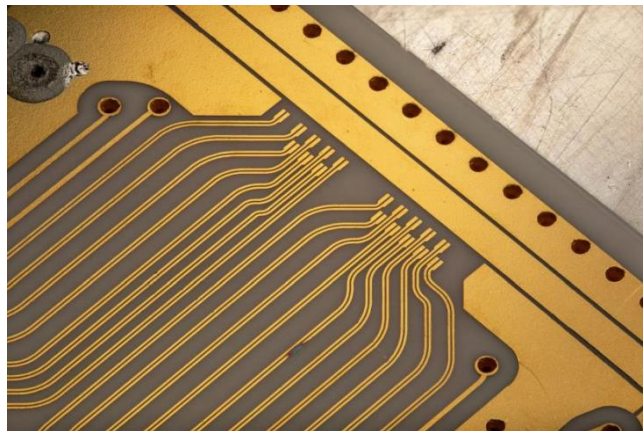
Uplinks:

- FEC5 at 5.12 Gbps
 - BW: 160/320/640 Mbps
 - e-ports : 28/14/7
- FEC5 at 10.24 Gbps
 - BW: 320/640/1280 Mbps
 - e-ports : 28/14/7
- FEC12 at 5.12 Gbps
 - BW: 160/320/640 Mbps
 - e-ports : 24/12/6
- FEC12 at 10.24 Gbps
 - BW: 320/640/1280 Mbps
 - e-ports : 24/12/6

UHV Boards

Fully-assembled Mk-II module with Timepix3 chip wire-bonded to it.

- The data signals require a very small track width and spacing (30 μm and 60 μm) to get the 100-ohm differential impedance on this 0.38 mm thick ceramic.
- The wire-bonding pads also have small features with a width of 56 μm and a spacing of 86 μm .
- The power traces need to be as large as possible with a thick copper to reduce the resistance and the voltage drop.
- The combination of these requirements increases the complexity of the ceramic board and forces the use of a complex and expensive thin-film manufacturing.



Layer Stack Legend

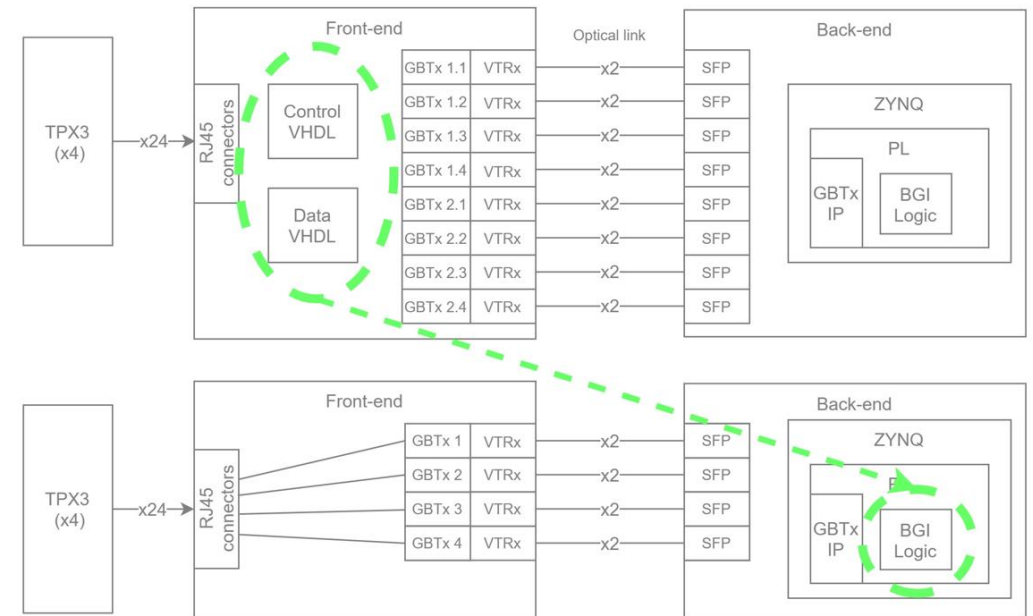
Material	Layer	Thickness	Dielectric Material	Type
Surface Material	Top Copper	0.012mm	Cu+Ni+Au	
Ti+Au+Ni+Au	Top Gold	0.003mm		Signal
Core		0.381mm	AL2O3 99%	Dielectric
Ti+Au+Ni+Au	Bottom Gold	0.003mm		Signal
Surface Material	Bottom Copper		Cu+Ni+Au	
Total thickness: 0.399mm				

FPGA based Front-end

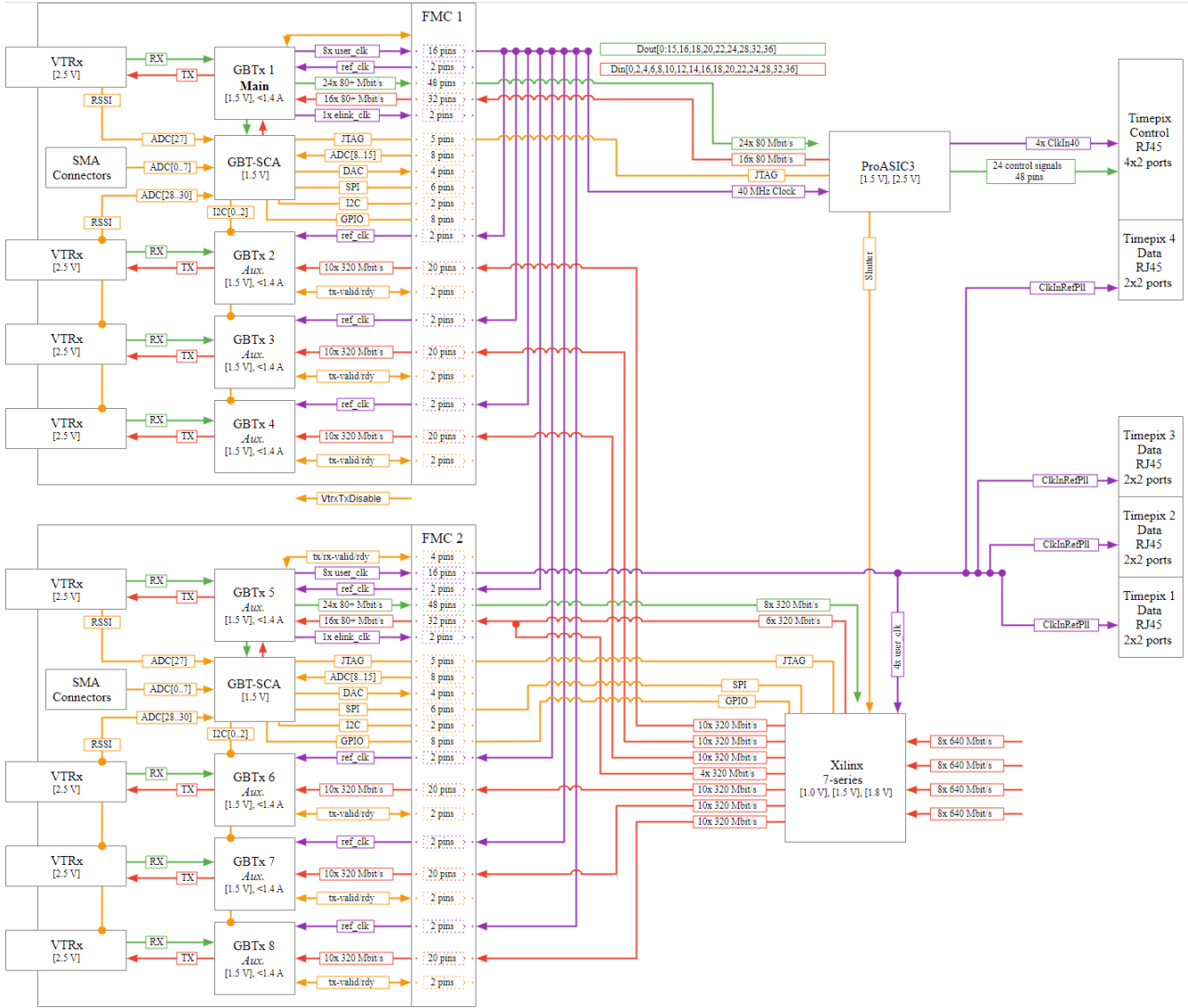
- **ProASIC3E (A3PE1500-FG484)**: it takes care of the control of the TPX3 detectors by sending commands with the correct timing and by toggling various pins.
- **SRAM-based Kintex-7 (XC7K70T1FBG676C)**: connected to the 32 data links coming from the detector and handles the synchronization and packaging of the serial data into 10-bit packets, which represent one byte of data due to the 8b10b encoding used in the TPX3.

ProASIC and the Kintex-8 logic into the B-E

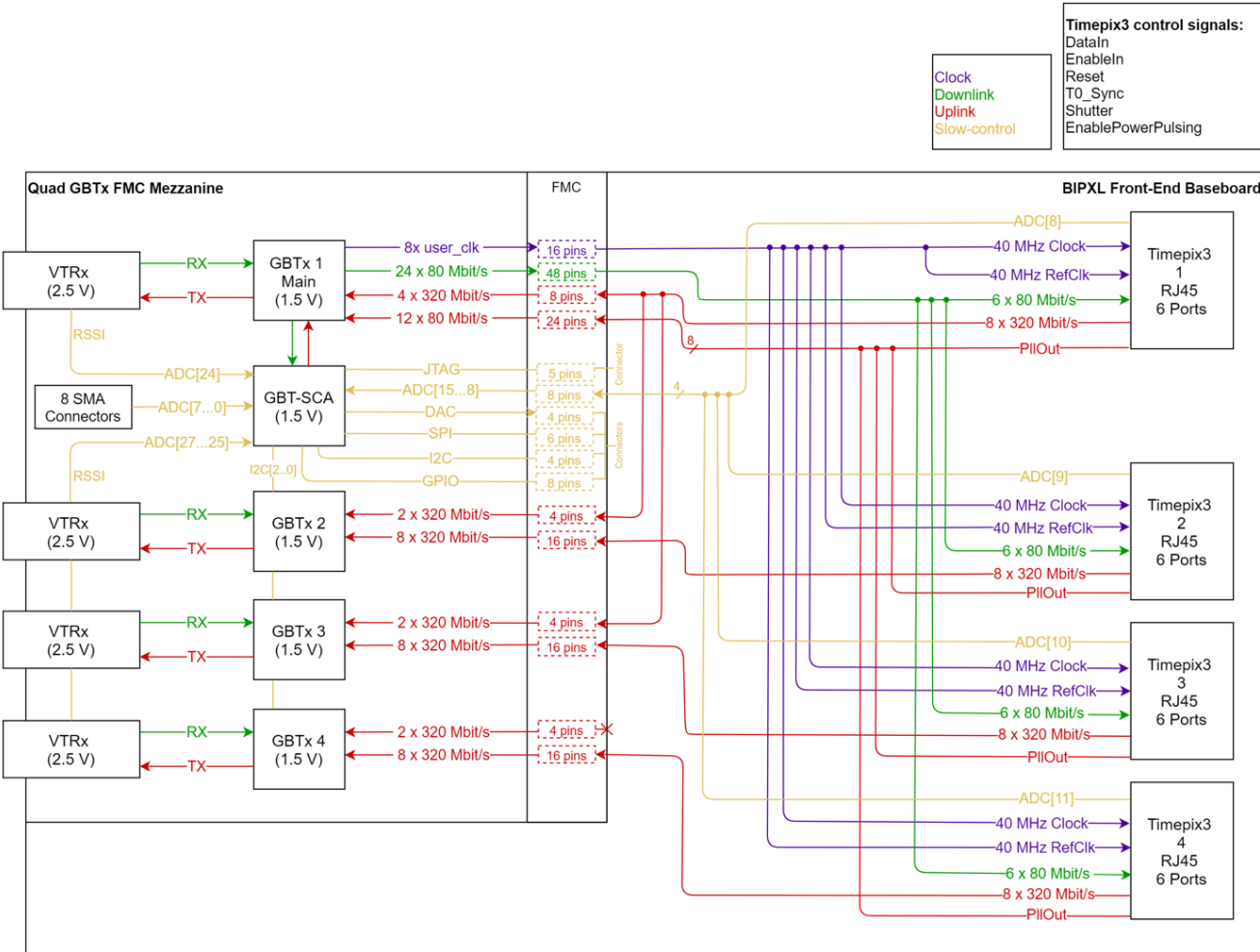
- **Control detector**: state-machine, FIFO and serializer to handle the control signals.
- **Data detector**:
 - Detecting the COMMA message in 8b10b codification.
 - Repackaging the received data for the data processing in the other PL modules.



FPGA based Front-end: Connections



GBTx based Front-end: Connections

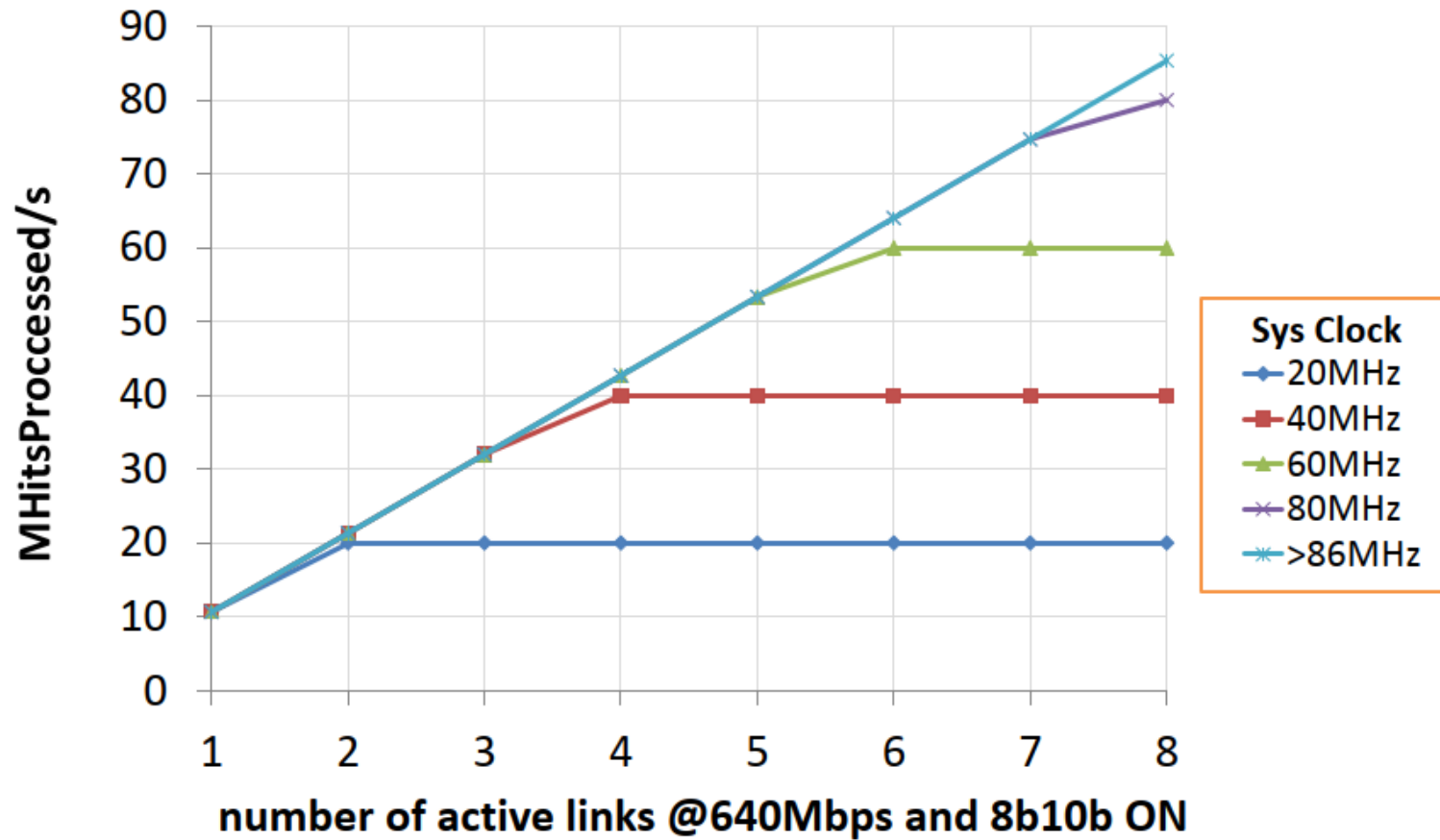


Timepix3 vs Timepix4

		Timepix3 (2013)	Timepix4 (2019)	
Technology		130nm – 8 metal	65nm – 10 metal	
Pixel Size		55 x 55 μm	55 x 55 μm	
Pixel arrangement		3-side buttable 256 x 256	4-side buttable 512 x 448	
Sensitive area		1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	0.43x10 ⁶ hits/mm ² /s	3.58x10⁶ hits/mm²/s
	Frame based (Imaging)	Max Pix rate	1.3 KHz/pixel	10.8 KHz/pixel
		Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)
	Max count rate	~0.82 x 10 ⁹ hits/mm ² /s	~5 x 10 ⁹ hits/mm ² /s	
TOT energy resolution		< 2KeV	< 1Kev	
TOA binning resolution		1.56ns	195ps	
TOA dynamic range		409.6 μs (14-bits @ 40MHz)	1.6384 ms (16-bits @ 40MHz)	
Readout bandwidth		$\leq 5.12\text{Gb}$ (8x SLVS@640 Mbps)	$\leq 163.84\text{Gbps}$ (16x @10.24 Gbps)	
Target global minimum threshold		<500 e ⁻	<500 e ⁻	

Timepix4 manual

Chip data output bandwidth



Timepix3 v1.9 manual

GBT-SCA

- **It was used to program the Kintex-7 in the FPGA based Front-end.**
- **It digitizes Timepix3 DACOut signals:**
 - Four analog signals arrive from the instruments to be digitalized for the GBT-SCA and to be sent to the main GBTx.
 - The JTAG pins are connected to a Xilinx-style header connector.
 - The DAC, SPI, I2C and GPIO pins, as well as 4 of the ADC pins finish in connectors in the baseboard.
 - The “Received Signal Strength Indication” signals from the VTRx devices are monitored using the GBT-SCA for the conversion.

Intrinsic Binary Resolution

- **Intrinsic binary resolution** refers to the theoretical or fundamental resolution limit of a detection system, based on the uncertainty in measuring a signal within a pixel.

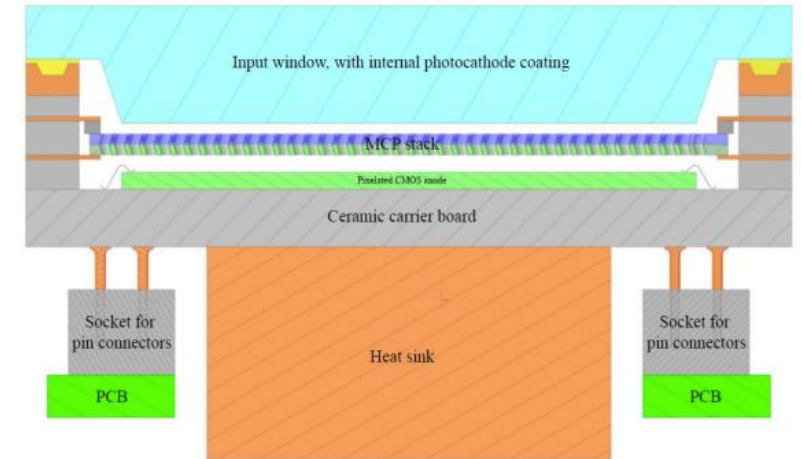
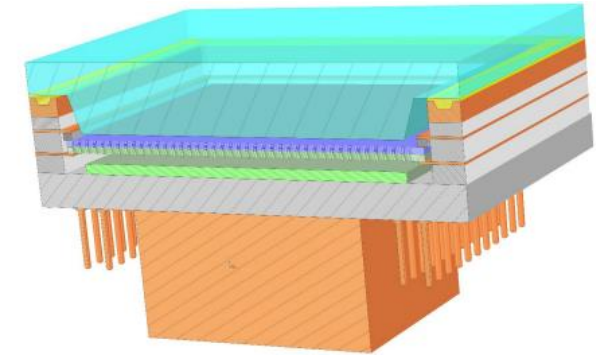
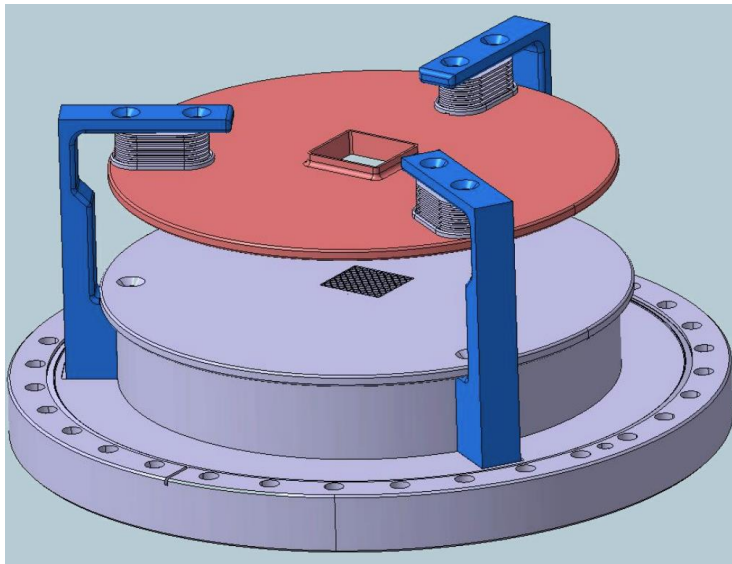
$$\text{Intrinsic Resolution} = \frac{\text{Pitch}}{\sqrt{12}} \approx 15,88\mu\text{m}$$

- The reason for dividing by $\sqrt{12}$ comes from a statistical analysis of the uncertainty in position measurements. It assumes that when an event occurs in the detector, it can happen anywhere within the pixel with equal probability. **Thus, the position within a pixel can be modelled as a uniform distribution.**
- **This standard deviation is interpreted as the intrinsic spatial resolution of the system, as it represents the statistical uncertainty in the true position of a particle that lands somewhere within a pixel.** In other words, it quantifies the uncertainty in knowing where exactly the event occurred inside the pixel area.

For more information: [Particle Detectors: Fundamentals and Applications](#). Hermann Kolanoski, Norbert Wermes (Appendix D)

Future for the BGI design

- Horizontal and Vertical BGIs are planned for the LHC. Several options for the design are being explored, using either Timepix3 or Timepix4. **One elegant solution uses parts from the 4D Photon project for the vacuum feedthrough and Timepix4 support.** → [IBIC 2024](#)



[Update on Timepix4 characterisation and integration on ceramic carrier](#)
[Dr Nicolo Vladi Biesuz](#)