Readout Electronics for Neutron Detectors at CSNS and CSNS-II: Challenges, Solutions, and Progress

Abstract

The China Spallation Neutron Source (CSNS) is undergoing an upgrade to CSNS-II, increasing its power to 500 kW. This talk summarizes the readout electronics for the 10 neutron instruments currently in operation or commissioning at CSNS, discussing challenges, solutions, and glitches encountered. We also present the development and testing of low-power readout electronics for 3He PSD arrays and high-density neutron scintillators, which are the main detector types for CSNS-II. The progress on prototypes, including ASIC-based preamplifiers, ultra-low power FPGA-based channel reduction circuitry, and low-power FPGA-based processing modules, will be discussed.

Summary

The China Spallation Neutron Source (CSNS) is a spallation neutron source operating at 150 kW power and 25 Hz repetition rate, with 20 planned neutron test beamlines. CSNS has been in operation since 2018, and the upgrade to CSNS-II began in early 2024, aiming to increase the target power to 500 kW within 5 years. CSNS-II will include 7 additional neutron instruments, primarily using 3He PSD tube arrays and large-area neutron-sensitive scintillators as detector solutions.

This talk will first summarize the readout electronics for the 10 neutron instruments currently in operation or commissioning at CSNS, discussing the challenges, solutions, and glitches encountered during development, production, commissioning, and operation.

We will then describe the main challenges, development progress, and beam test results for two major detector types planned for CSNS-II:

1. Low-power readout electronics for 3He PSD arrays: Vacuum operation is crucial to eliminate air influence in neutron scattering experiments, making thermal conduction of the electronics challenging. The higher counting rate requirement of 100 kHz at 500 kW power necessitates high-performance, low-power readout electronics. We are developing and evaluating both discrete and ASIC versions of pre-amps for charge-to-amplitude conversion, consuming around 10 mW/Ch. A digitization board with 16 ADC channels will digitize the pre-amp outputs and calculate the hit position and energy of neutron events. Both the preamplifier and digitization board will operate in vacuum, with a power consumption of 3 - 4W for a set of electronics responsible for 8 PSD tube readouts. A ZYNQ MPSOC-based data accumulation board will collect data from 8 digitization modules and perform real-time counting rate, TOF, charge spectrum monitoring, and histogramming for real-time diagnostics and initial analysis data.
2. High-density neutron scintillator readout electronics: Scintillator-based neutron detectors are promising replacements for rare 3He. Current scintillator-based large-area detectors at CSNS have a spatial resolution of 3mm x 50mm, with channel numbers in the tens of thousands. CSNS-II plans to achieve 1mm x 1mm spatial resolution with a 1 square

meter detection area, requiring 1 million electronic channels for pixelized readout due to counting rate requirements. We will present the development and testing progress of a prototype with 3.5mm x 7mm spatial resolution, 20cm x 20cm area, and ~1600 readout channels. The main components of this system include ASIC-based preamplifiers, ultra-low power FPGA-based 32:1 channel reduction circuitry, and low-power FPGA-based processing modules. Low power consumption is a key requirement as the system will also operate in vacuum.

This talk will provide valuable insights into the challenges and solutions related to readout electronics for neutron detectors at CSNS and CSNS-II, highlighting the importance of low-power, high-performance systems for advanced neutron scattering experiments.