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Readout Electronics for dN/dx Measurement of the Drift Chamber for CEPC R&D

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The Circular Electron Positron Collider (CEPC) drift chamber requires high-performance readout electronics for accurate dN/dx measurement and particle identification (PID) using cluster counting techniques. The prototype readout electronics consists of high-speed op-amp based fast current amplifiers, 1.3 Gsps ADCs, and FPGAs for data acquisition and buffering. The system aims to acquire accurate current signals and send them for machine learning-based cluster counting algorithms. Systematic simulations, tests of high-bandwidth pre-amplifiers, and the development of multi-channel high-speed sampling electronics will be presented. The prototype, with more than 10 channels, will be evaluated in testbeam experiments to assess PID capability.

Summary (500 words)

The Circular Electron Positron Collider (CEPC) is a proposed Chinese electron-positron collider designed to study the Higgs boson. With a circumference of 100 kilometers, it would be the world's largest particle accelerator. The drift chamber, a proposed subdetector for the main CEPC experiment, is optimized for particle identification (PID) using cluster counting techniques. A key requirement is to achieve 3 sigma separation power for K/pi with momentum up to 20 GeV/c.

dN/dx measurement is the process of measuring the number of clusters over the track, where the number of clusters corresponds to the number of primary ionizations. The yield of primary ionization follows a Poisson distribution. To eliminate the effects of secondary ionization, dN/dx is based on peak finding and clusterization.

The total cell/channel number for the detector design in the CDR is 27,623. The signal to be measured is a fast induced current signal on the wires, typically a pulsed current signal with multiple peaks, a rise time in the nanosecond scale, and a pulse width of around a microsecond.

To perform accurate dN/dx measurements, fast and low-noise electronics are crucial. The readout electronics consist of two main parts: radiation-hardened, high-bandwidth current preamplifiers located within the detector, and off-detector digitization electronics connected via several-meter-long cables.

The pre-amplifiers will eventually be radiation-hardened for operation within the detector. However, the prototype will use commercial op-amps to verify the effectiveness of the circuit. The off-detector digitization electronics, consisting of 1.3 Gsps ADCs and FPGAs for data acquisition and buffering, do not require radiation hardening due to their location.

Demonstrator electronics have been developed and tested with electron beams. Currently, a prototype is being developed, consisting of high-speed op-amp based fast current amplifiers, high-speed 1.3 Gsps ADCs, and FPGAs for AD conversion and buffering. The data is then sent to a DAQ server via fast Ethernet links. The prototype will have more than 10 channels and is planned to be tested in testbeam experiments to evaluate the performance of PID capability. Each time the digitization electronics receives a trigger, it will buffer 2,000 data points for channels with amplitudes above the threshold.

This talk will present the scheme of the prototype electronics, providing a systematic description of the readout electronics scheme. It will also discuss the simulation and testing of high-bandwidth pre-amplifiers and the development of multi-channel high-speed sampling electronics, as well as the firmware for data buffering and packaging.

The development of high-performance readout electronics is essential for accurate dN/dx measurements and particle identification in the CEPC drift chamber. The prototype system, with its fast current amplifiers, high-speed ADCs, and data acquisition capabilities, will be a significant step forward in achieving the required performance for the CEPC experiment.

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