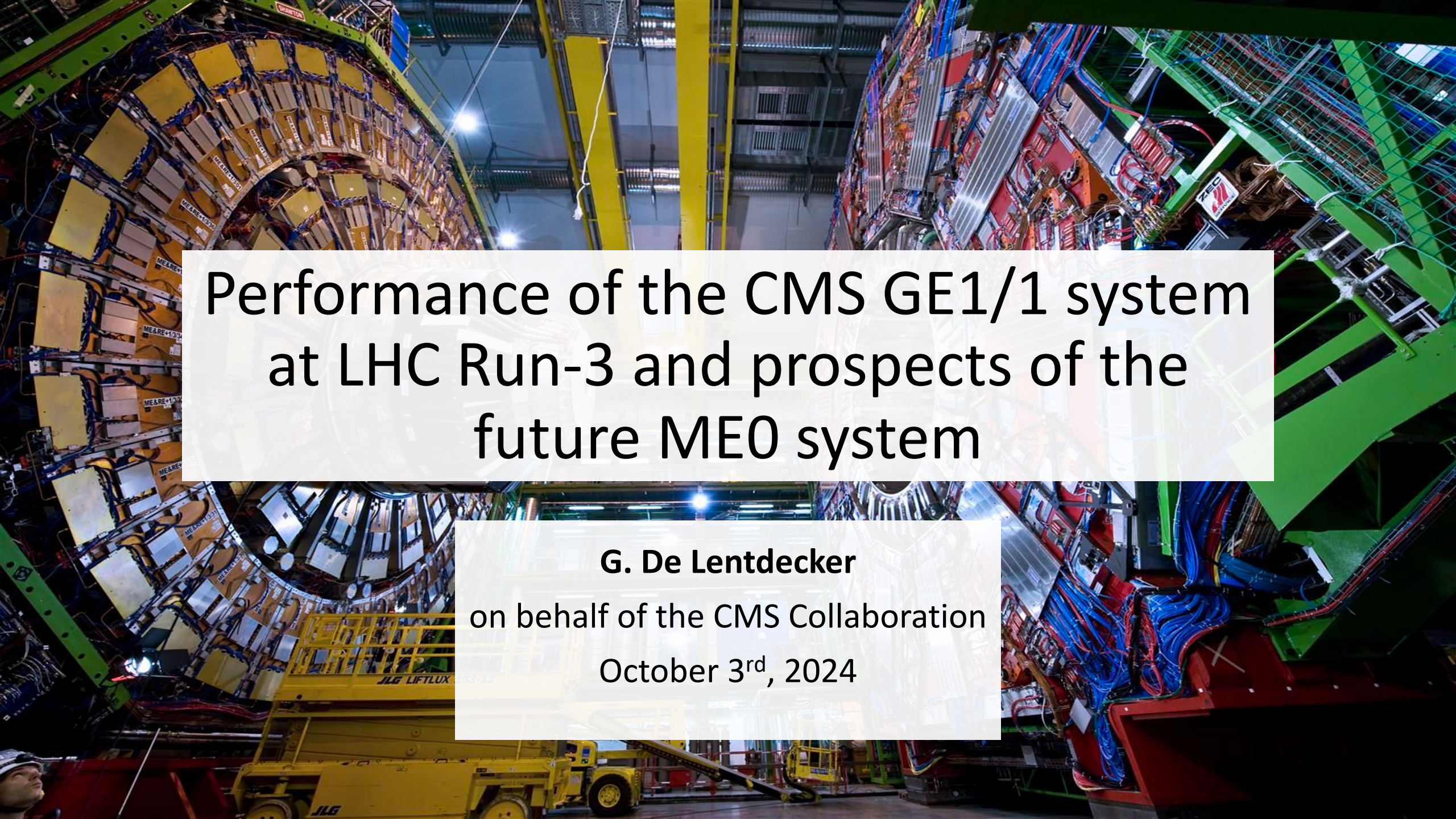


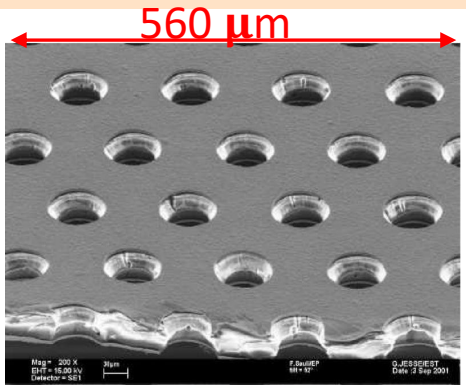
Performance of the CMS GE1/1 system at LHC Run-3 and prospects of the future ME0 system

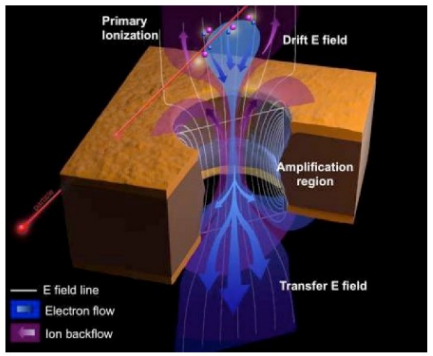
G. De Lentdecker

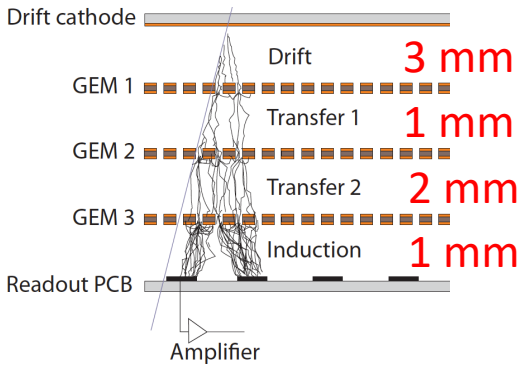
on behalf of the CMS Collaboration

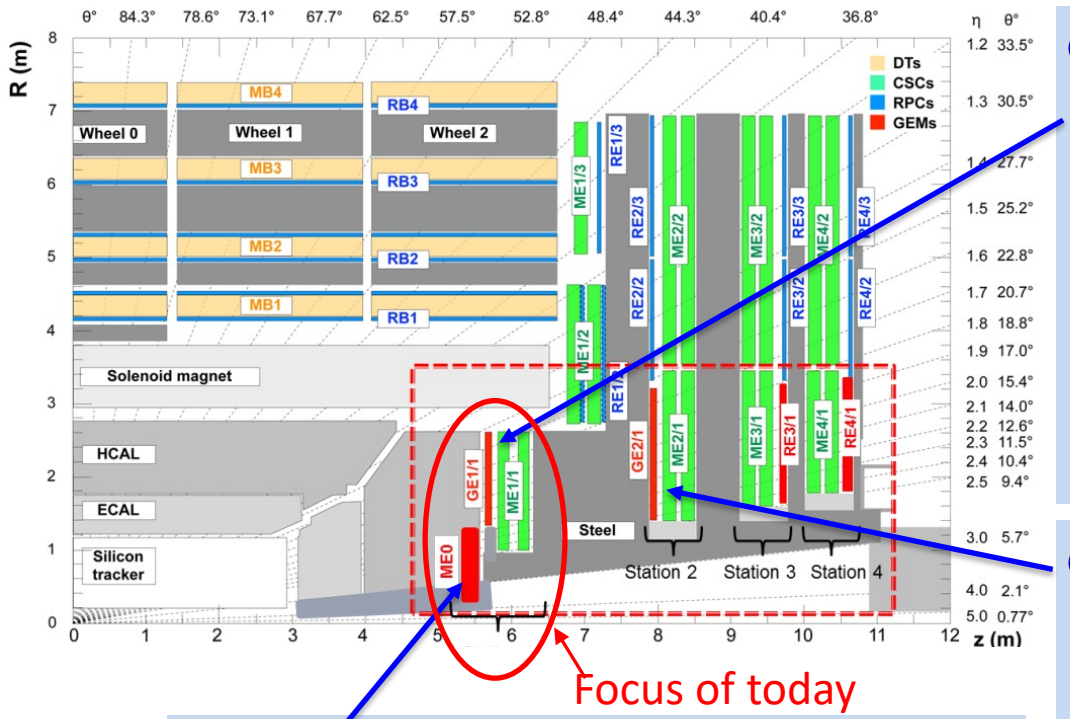
October 3rd, 2024

The CMS GEM project









Focus of today

ME0:

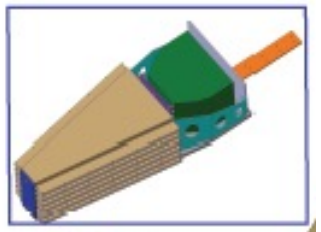
The only Muon station at the highest η

$2.0 < |\eta| < 2.8$

6 layers of Triple-GEM

each chamber spans 20°

Installation: LS3 (2027)



GE1/1:

$1.55 < |\eta| < 2.18$

baseline detector for GEM project

36 staggered chambers per endcap, each chamber spans 10°

One chamber is made of 2 back-to-back Triple-GEM detector

Installed in 2019-20

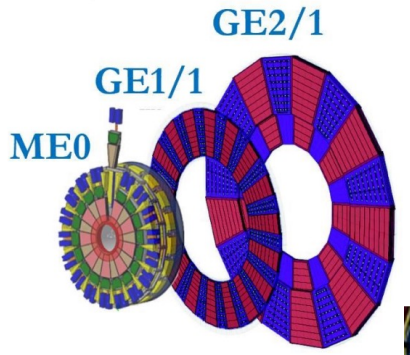
Recording LHC Run-3 data since 2022

GE2/1:

$1.55 < |\eta| < 2.45$

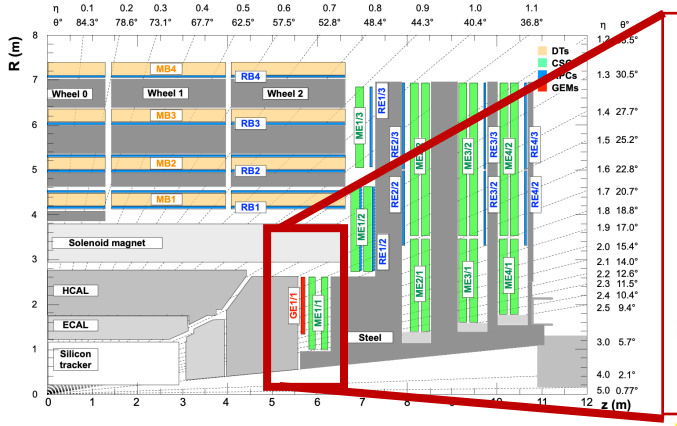
18 staggered chambers per endcap, each chamber spans 20°

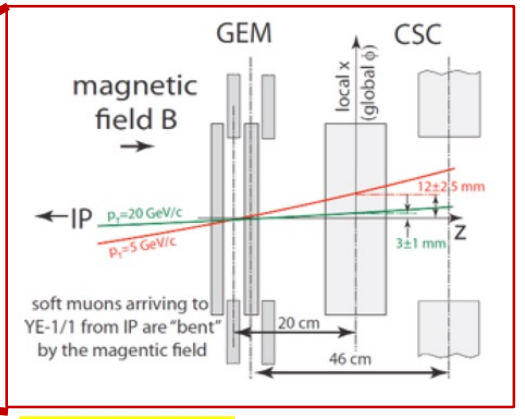
Installation: After LS3



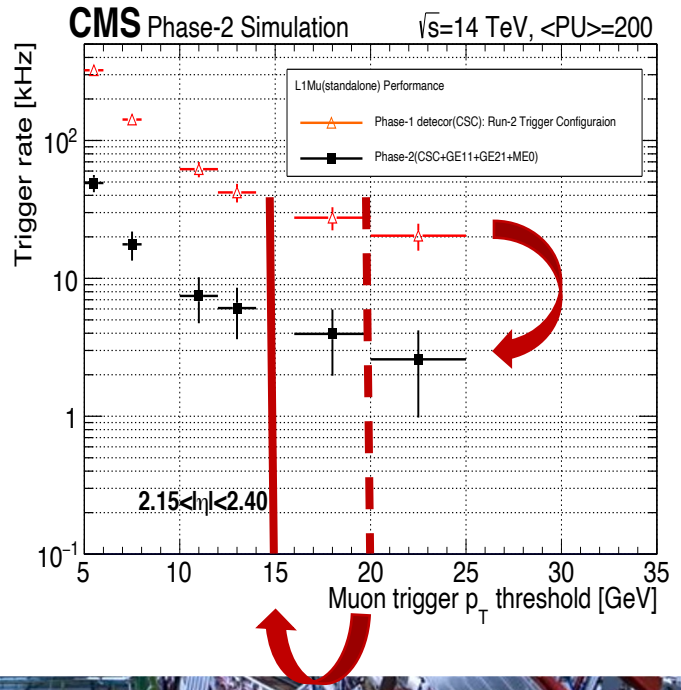
Objectives & specifications

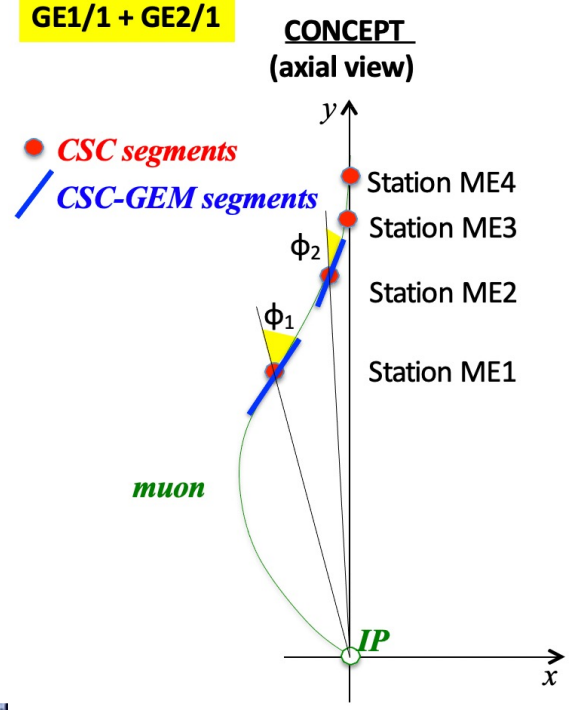
- To improve muon tracking and triggering performance in the most forward region of the CMS muon spectrometer
- With ME0: extend the muon coverage beyond $\eta = 2.4$
- GE1/1 specifications
  - Particle rate: a few kHz/cm^2
  - TID: a few krad
  - Spatial resolution: better than 300 μradian
  - Time resolution per chamber: 8-10 ns





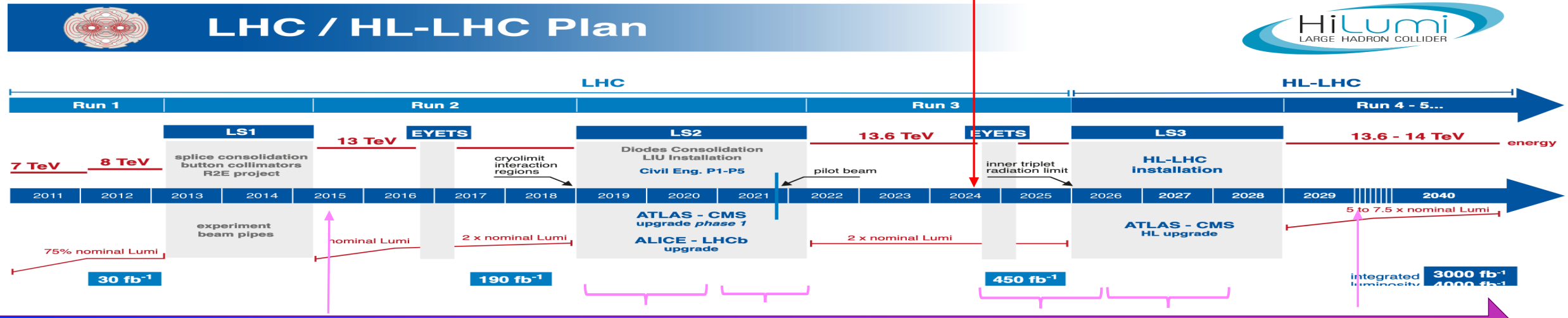
GE1/1 + GE2/1



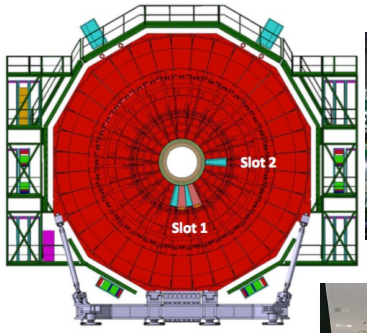


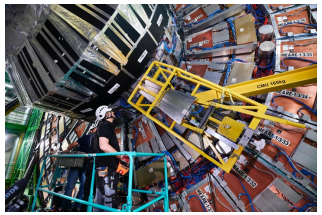
GEM project timeline

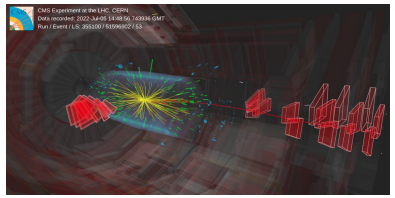
You are here

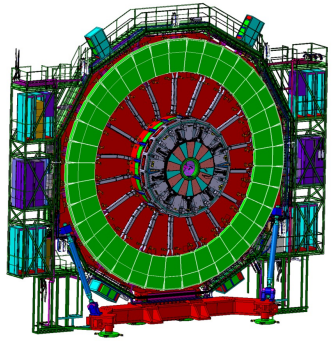


prototypes | GE11 TDR | Slice Test | GE1/1 Instal. & comm. | ME0 Prod. | ME0 Instal. & GE1/1 refurbishment | GE2/1 Instal.





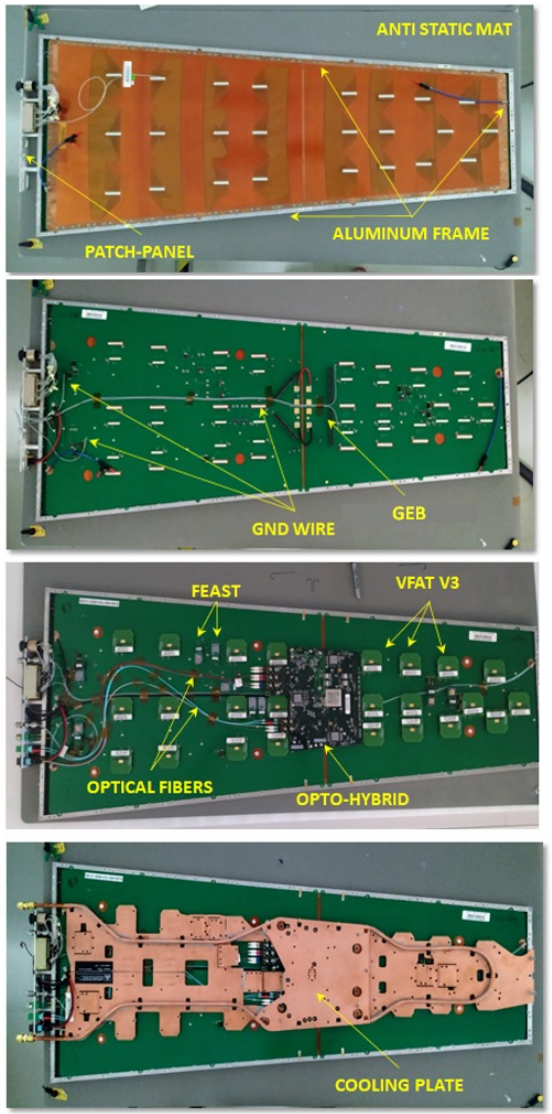


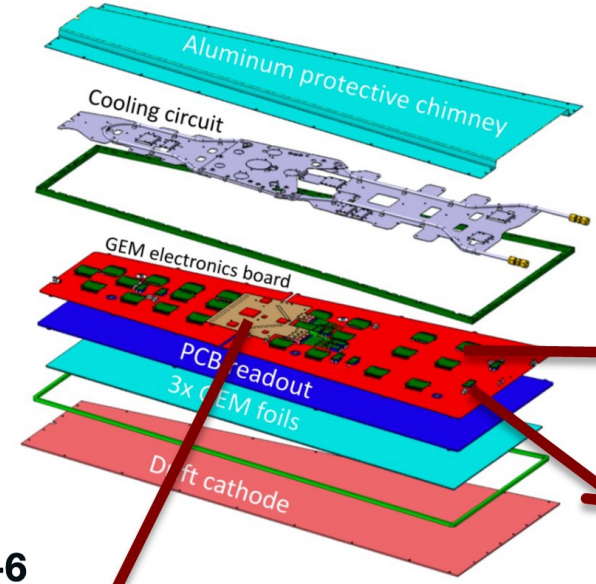


Outline

- GE1/1 electronics system
  - Performance & Issues
- ME0 status & prospects

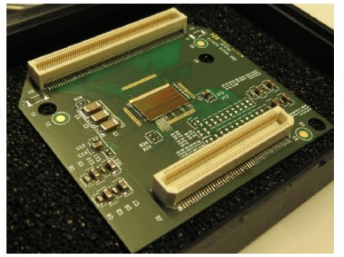
GE1/1 Electronics system overview





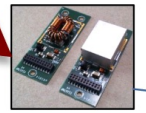
GE1/1 system:

- 72 Super-Chambers (SC)
- 3456 VFAT3 chips
- 432 GBT + VTRx optical link (DAQ path)



FE chip: VFAT3

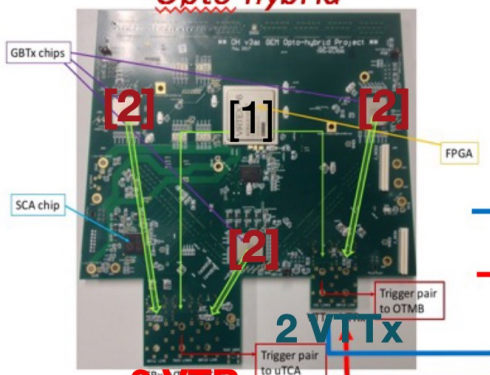
- 24 VFAT3 / chamber
- 128 channels / chip
- Binary readout
- Tracking + Trigger data



[1] Virtex-6
[2] GBTx

GE1/1 Electronics

Opto-hybrid

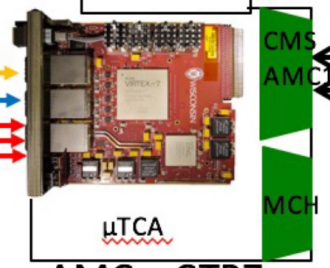


Trigger data
(3.2 Gbps – 10b/8b)
GBT links: Traking data
(4.8 Gbps)

CSC Trigger Mother Board (TMB)

EMTF

FEAST (DC DC converter, LV VFAT3 & OH)

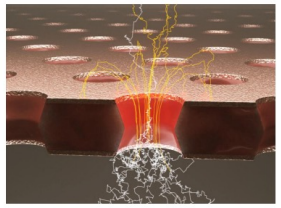


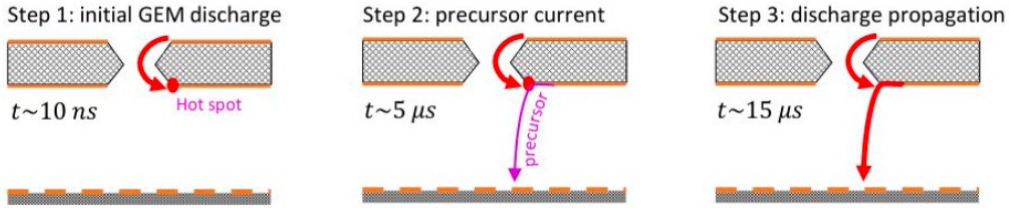
DAQ
TTC

AMC = CTP7

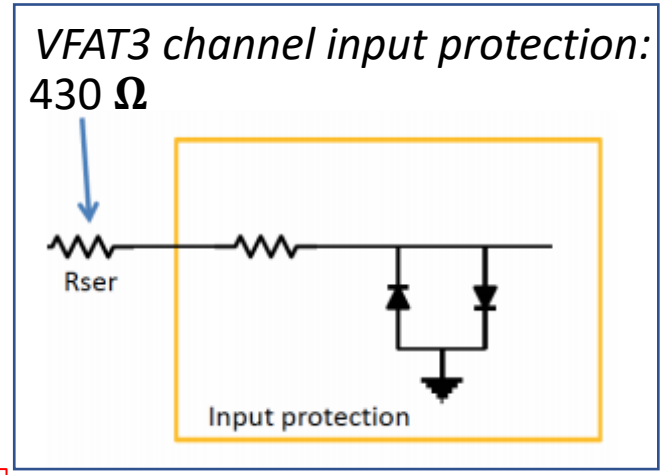
Damages on electronics due to discharges

- GEMs, like any other Micro Pattern Gaseous Detector, can suffer from discharges between its electrodes
  - Today discharge rate <2/h/chamber





- Despite input protection some VFAT3 channels may be destroyed
  - Today we count ~0.3% of damaged channels
- <1.5% of VFAT3 channels are masked due to
  - High noise
  - Damaged VFAT3 biasing circuit



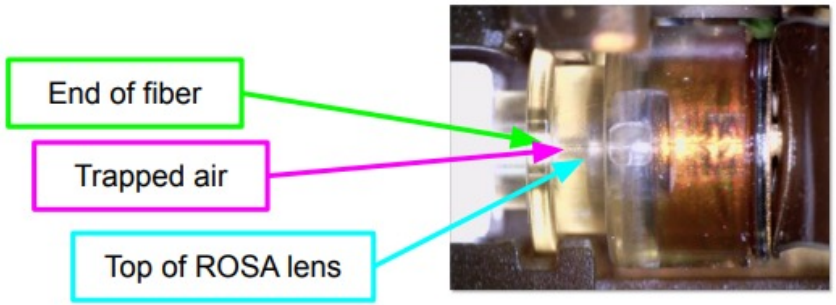
All damaged VFAT3's will be replaced during LS3

VTRx outgassing

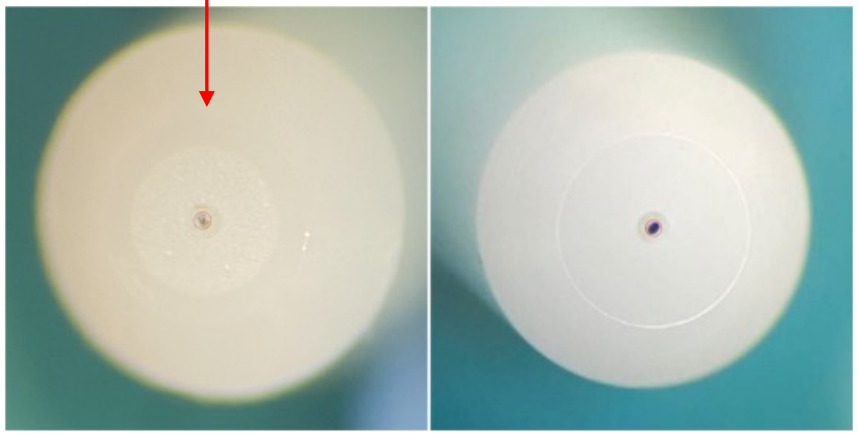
- Not a new issue: known since 2021

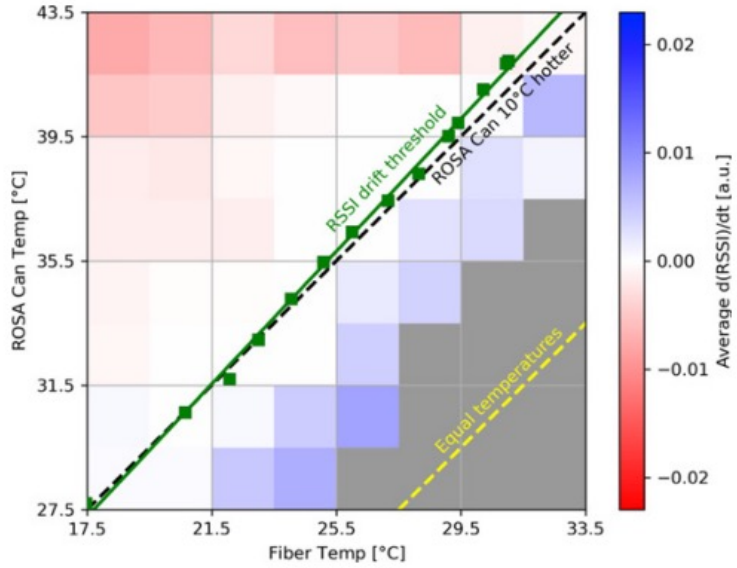
https://indico.cern.ch/event/1019078/contributions/4444259/attachments/2312222/3935142/GECummings_TWEPP2021_CMSHCALVTRx.pdf

- Today: how we operate GE1/1 with this issue
- Tomorrow: how to improve the situation
- Recap:
  - Outgassing of ROSA* -> condensation of material on fiber face
  - Mitigation: keep **Δ**T° (ROSA-Fiber) < 10°C



From 2022 JINST 17 C05020

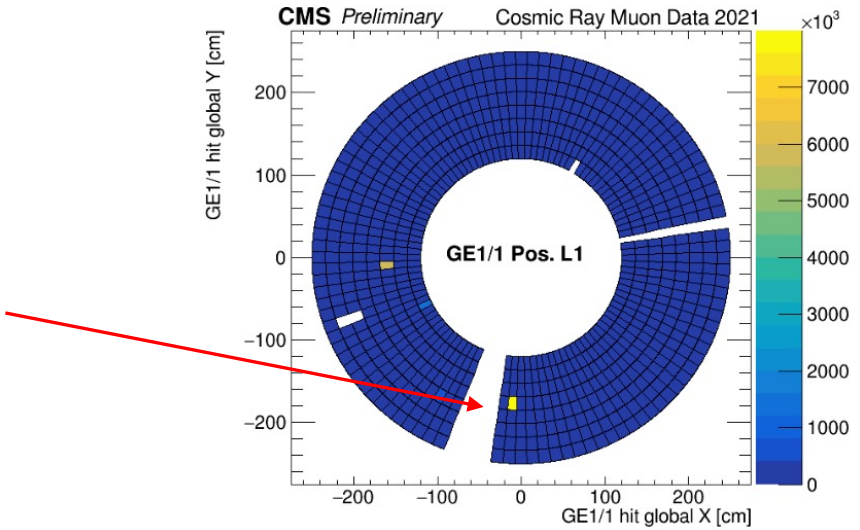


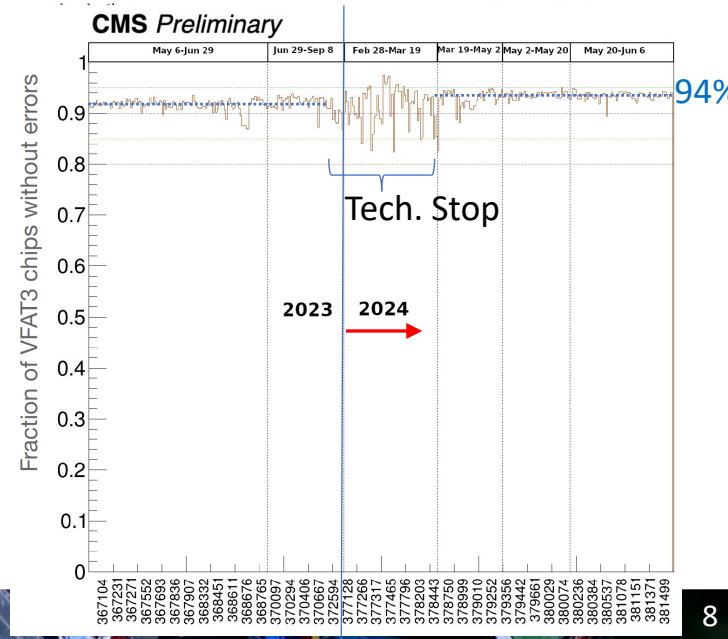


*ROSA= Receiver Optical Sub-Assembly

VTRx outgassing - today

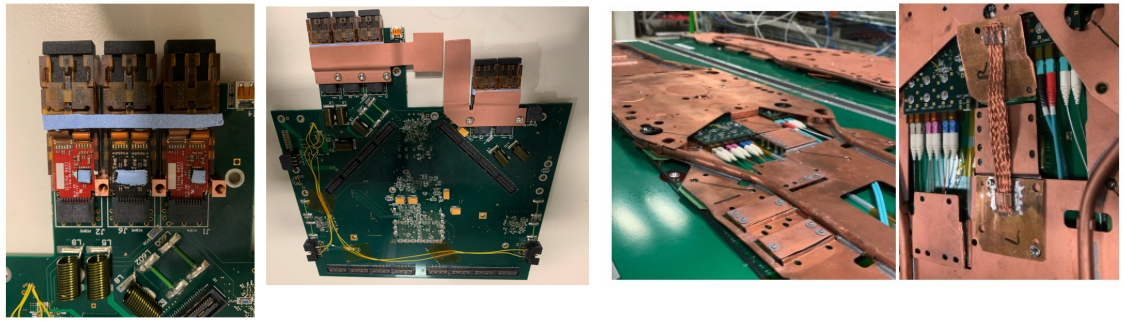
- GE1/1 was installed in 2021 and CMS had to be closed by end of March 2022
  - Not enough time to rework the 144 Opto-hybrids
- Consequence: ~6-7% of the 432 VTRx are not properly communicating at any time
  - Rather stable now
- Mitigation:
  - interplay between DAQ and DCS (Detector Control System) to automatically power cycle the affected Opto-Hybrid when we configure the system

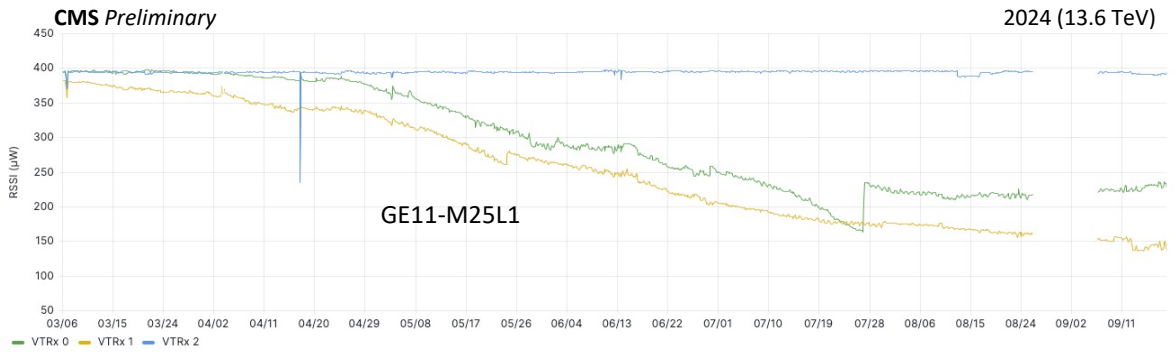


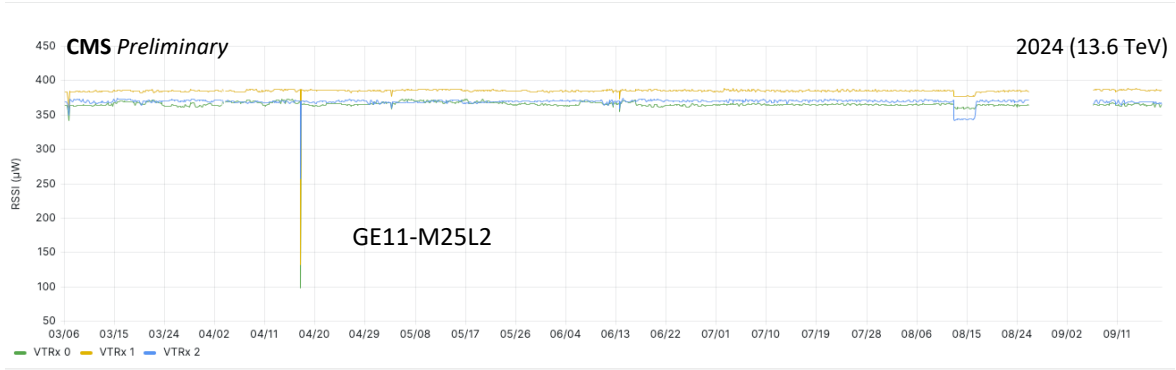


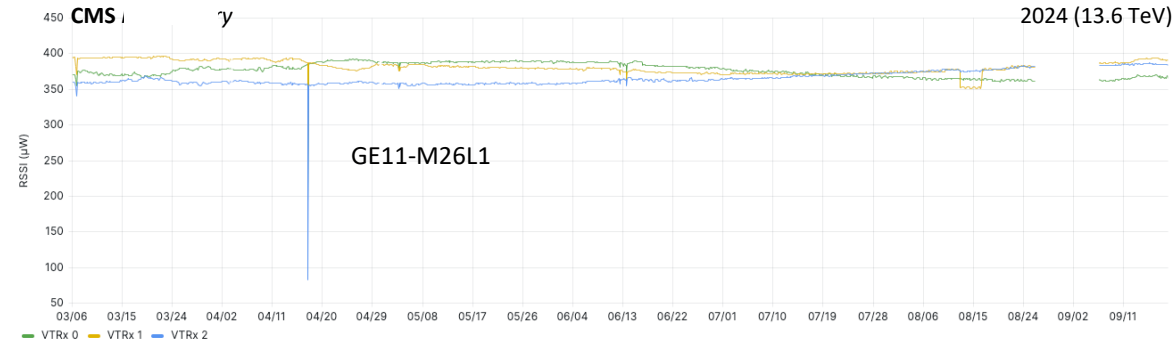
VTRx outgassing - future

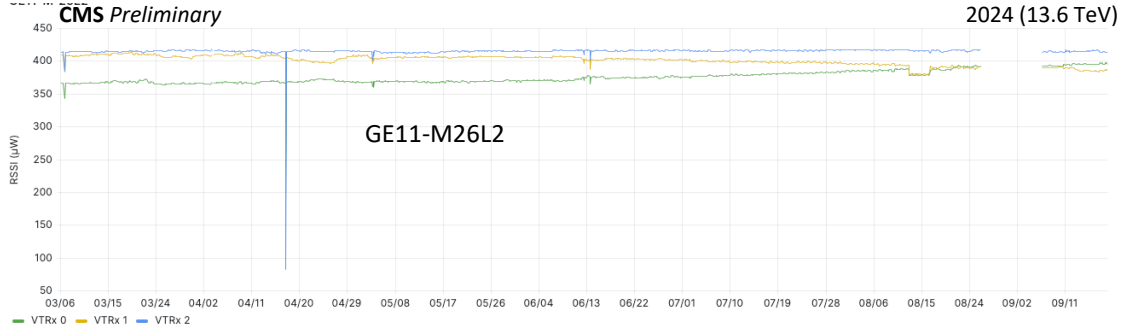
- All GE1/1 chambers will be extracted from CMS during LS3
- The OH cooling will be improved
- In January 2024, 4 GE1/1 chambers have been replaced and equipped with the improved cooling as well as the VTRx RSSI (Receiver Signal Strength Indicator) monitoring:











VTRx outgassing - future

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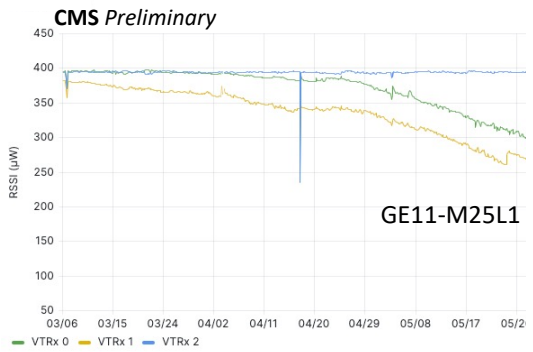
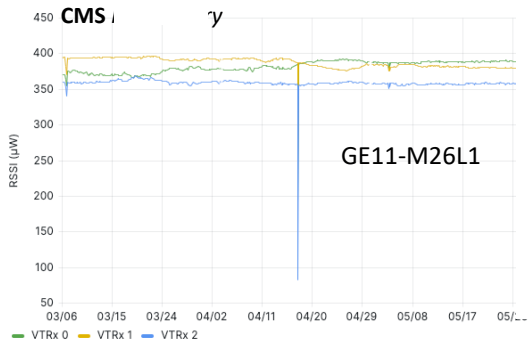
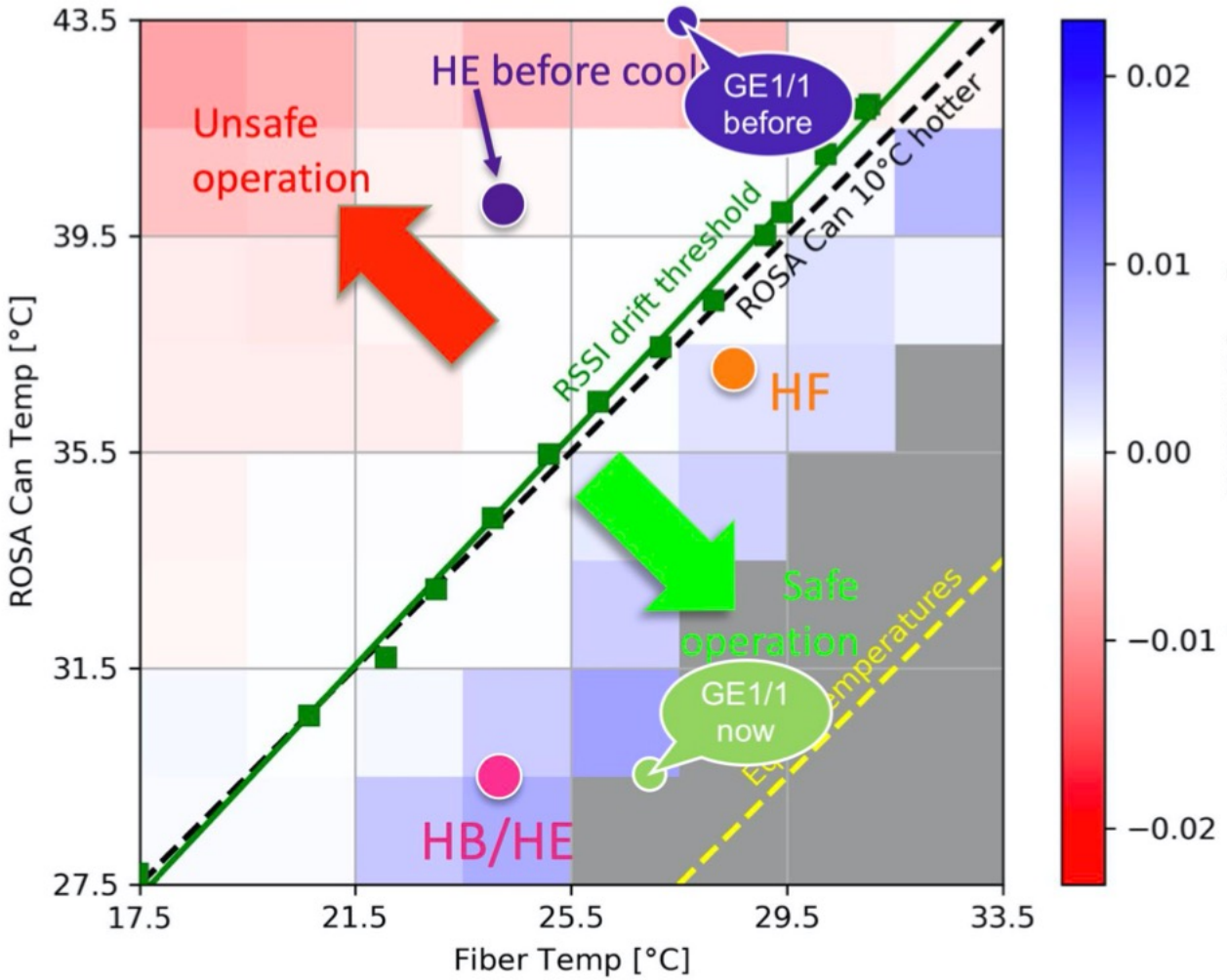
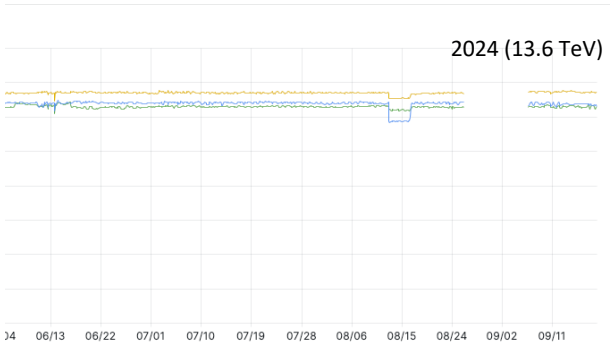
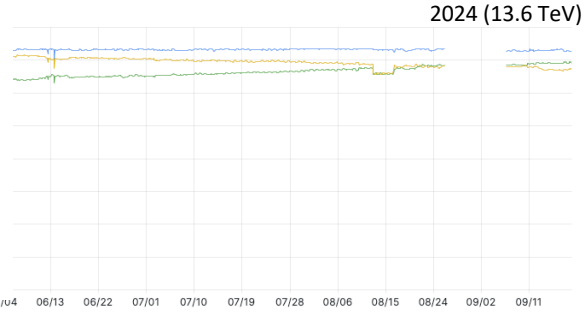
- In January 2024, 4 GE1/1 and equipped with the i VTRx RSSI (Receiver Sign







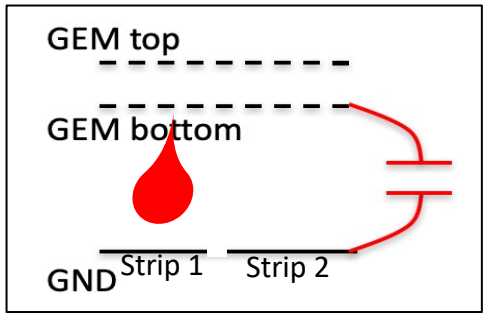


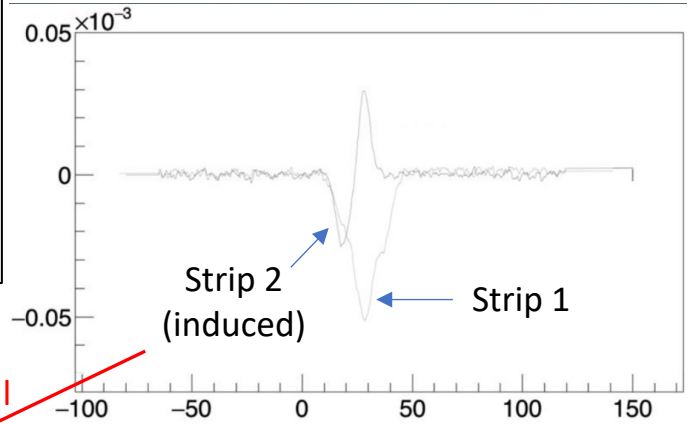


L1 Trigger: angle and time resolution

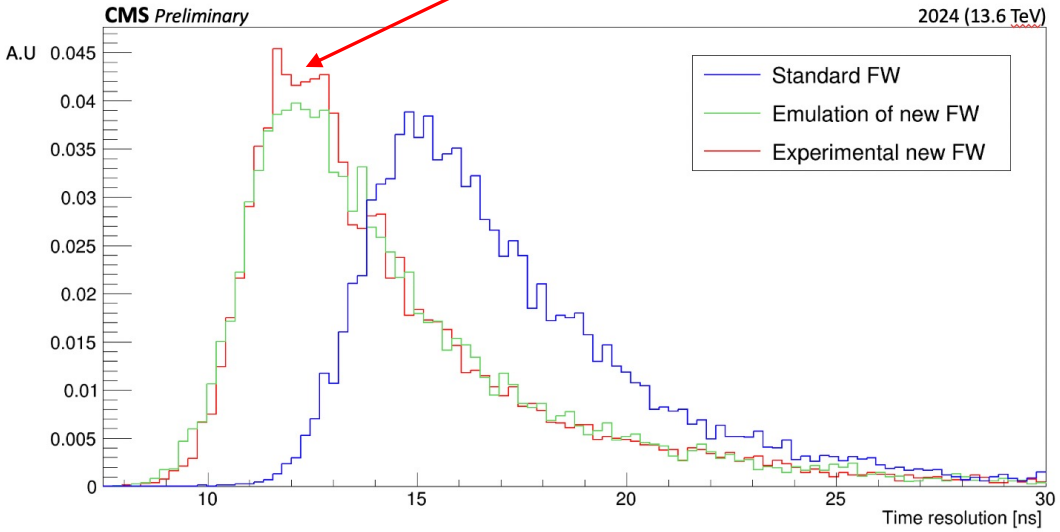
In 2024, major progresses on the trigger side:

New GE1/1 Firmware to improve time resolution

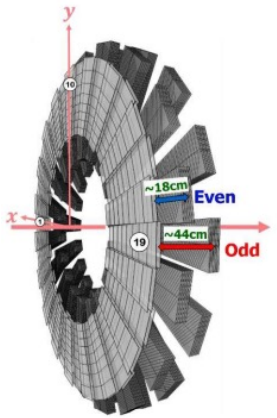


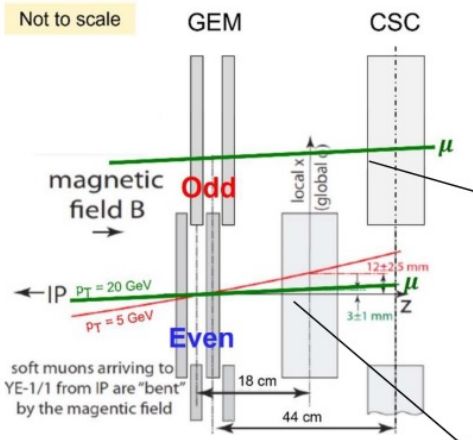


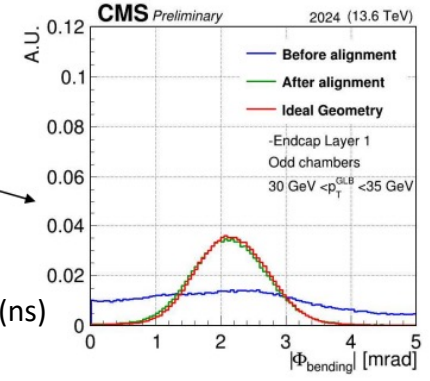
By masking the out of time signal



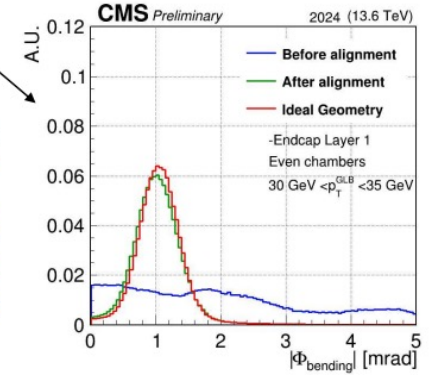
GE1/1-ME1/1 alignment included in CSC local trigger







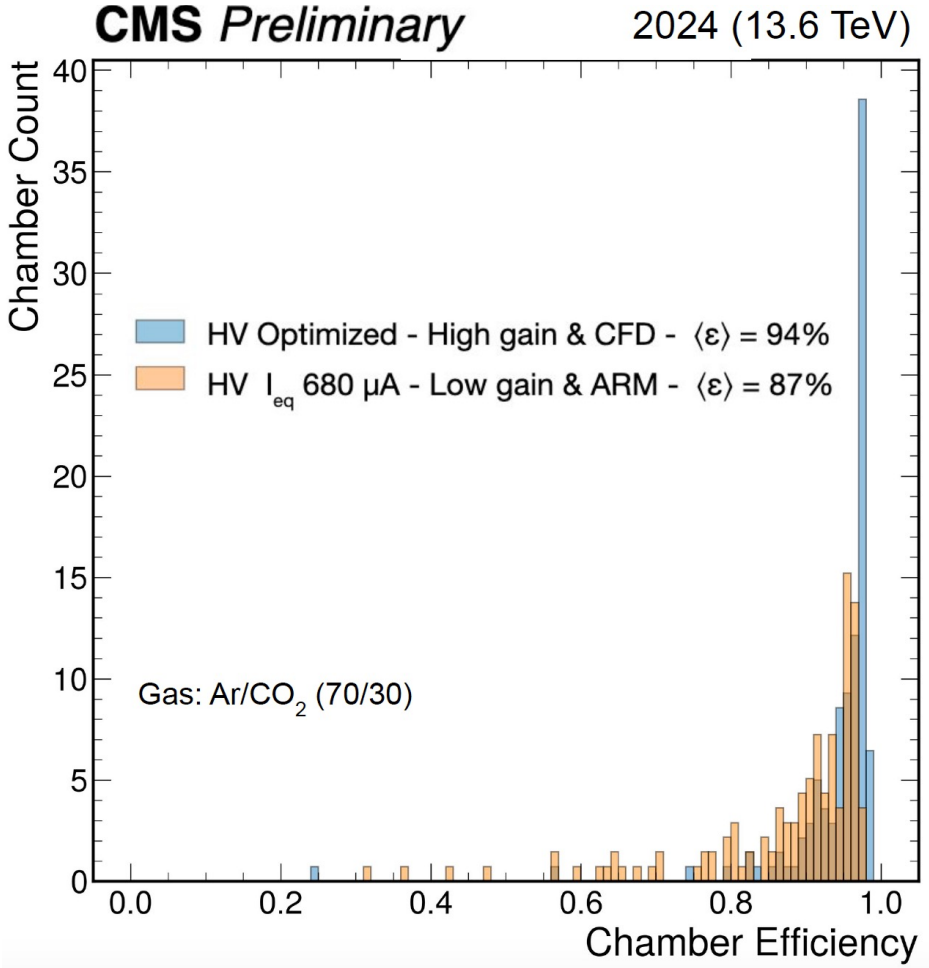
t (ns)



Measurements of GE1/1-ME1/1 bending angles (BA), ϕ_{bending}, for $\mu^{\pm}$ $(30\ \text{GeV} < p_T^{\text{GLB}} < 35\ \text{GeV})$,

GE1/1 is ready for inclusion in the CMS Level-1 Trigger

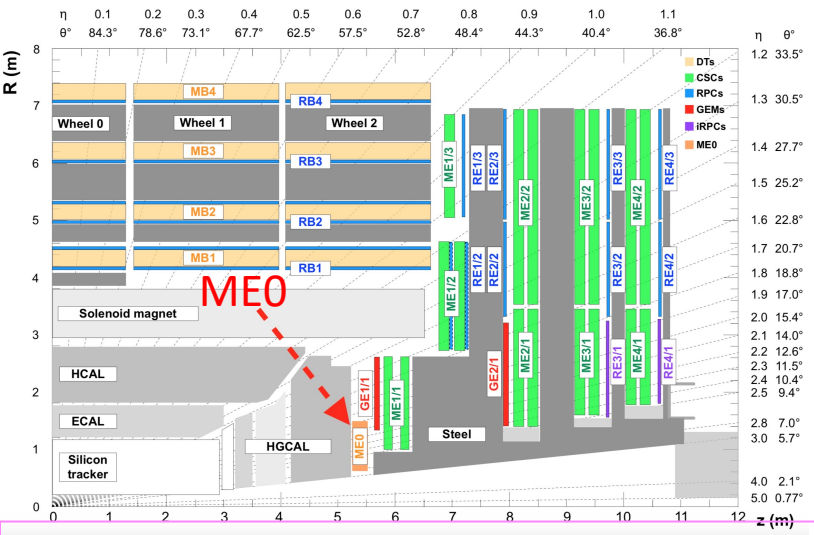
GE1/1 overall efficiency

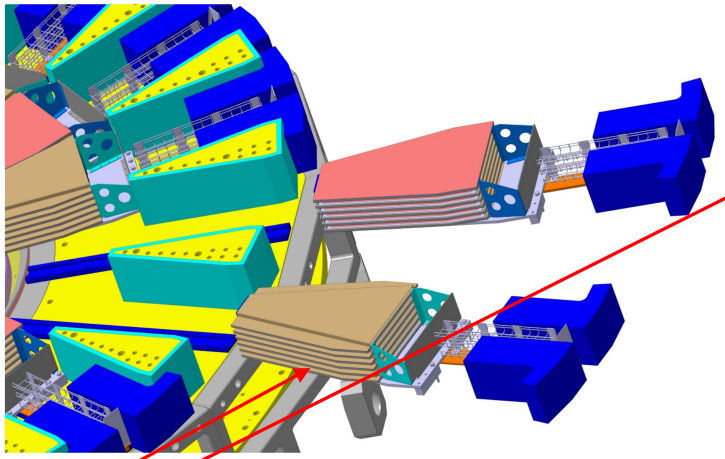


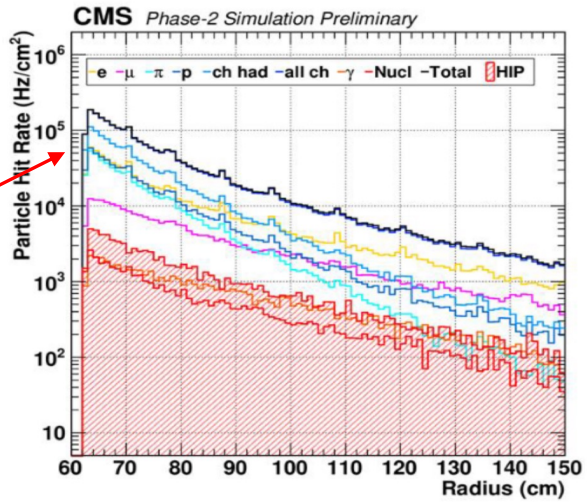
- After optimizing HV for each chamber
- After optimizing VFAT3 configuration

* Plot excludes chambers with VTRx issue

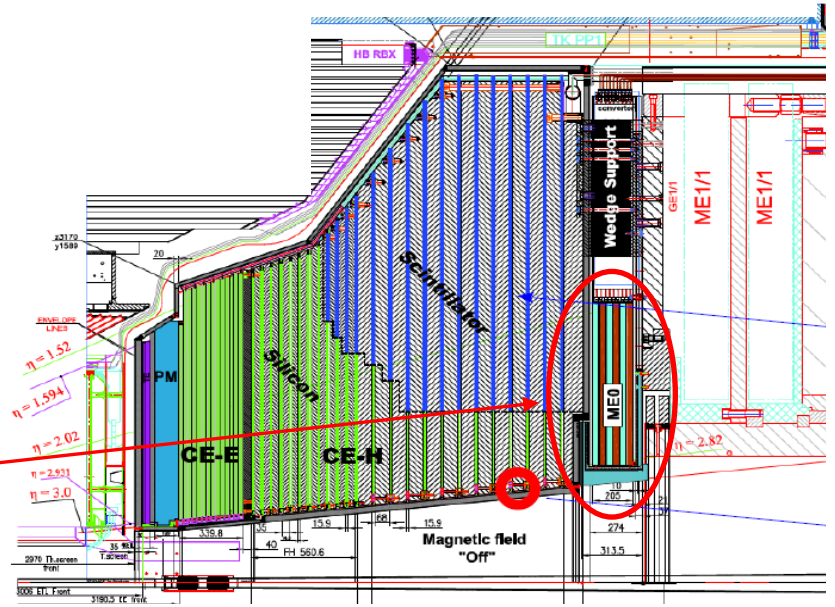
ME0



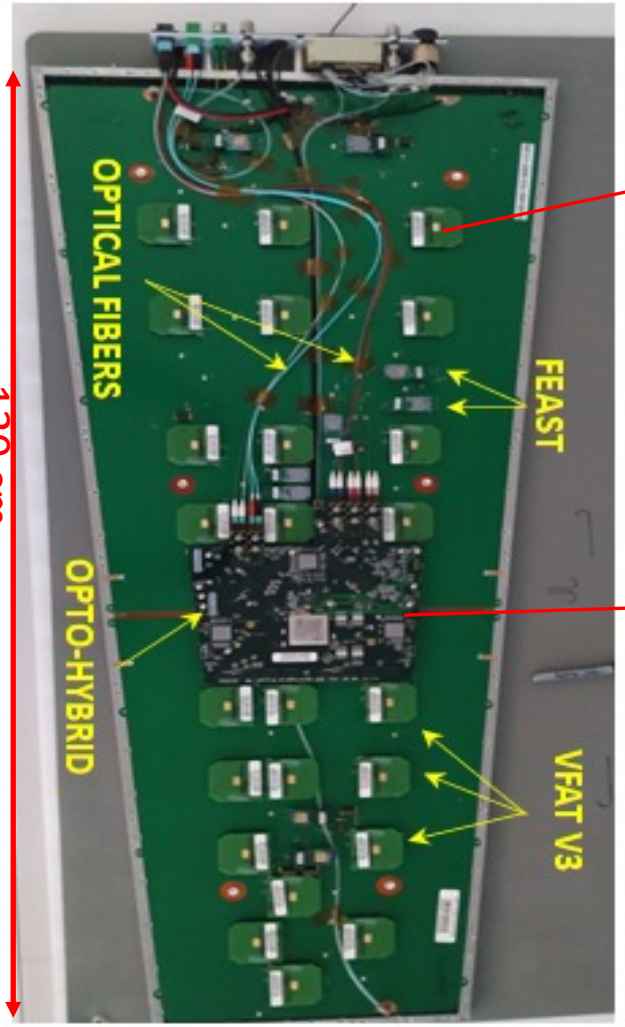




- ME0 increases CMS muon coverage to: 2.0 < |η| < 2.8
- 18 stacks per endcap, each made of 6 layers of Triple-GEM detectors
- Rate capability > 150 kHz/cm^2
- Accumulated charge (at the end of HL-LHC) ~ 8 C/cm^2
- TID up to 250 kRad (neutron fluence up to 4 x 10^{14} n/cm^2)
- Time resolution (per chamber): 8-10 ns
- Located behind new CMS HGCAL and covered by HGCAL services
  -> no access after installation during all HL-LHC

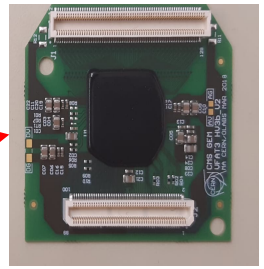


From GE1/1 to ME0

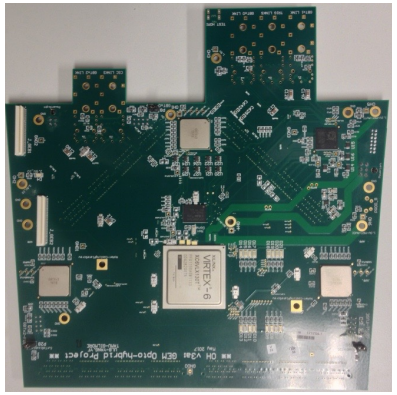


120 cm

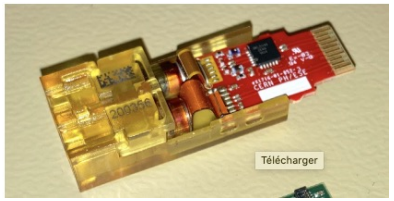
24 VFAT3s



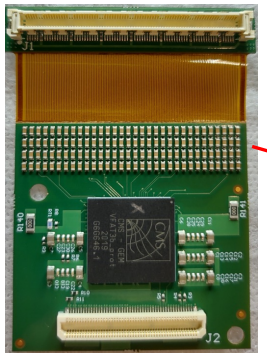
VFAT3 Hybrid (rigid)



Opto-Hybrid incl. FPGA

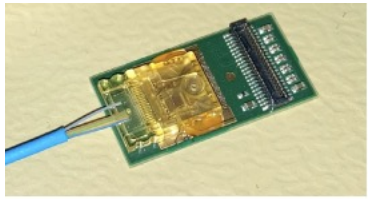


VTRx

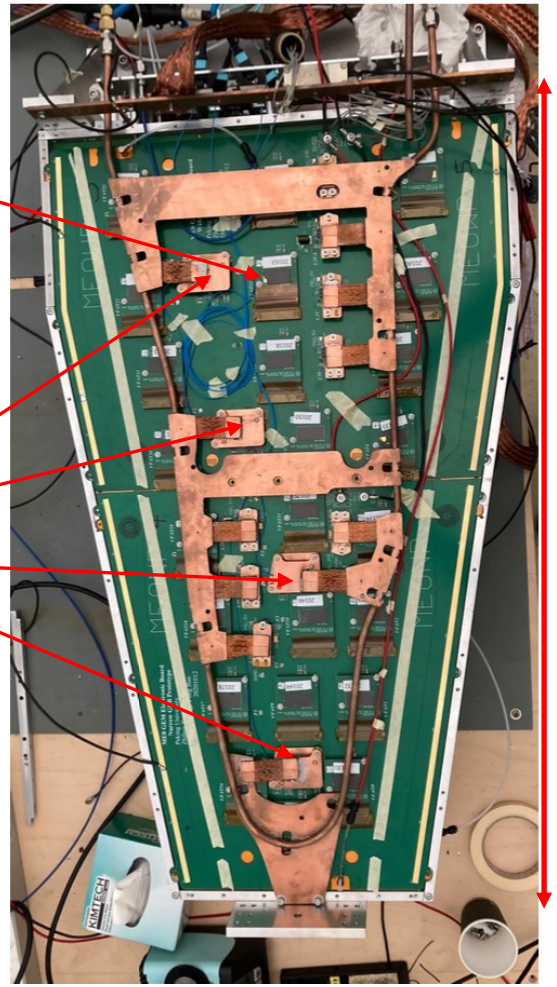


VFAT3 Plug-in card
(incl. flex part)

FPGA-less Opto-Hybrid
with 2 LpGBTs



VTRx+

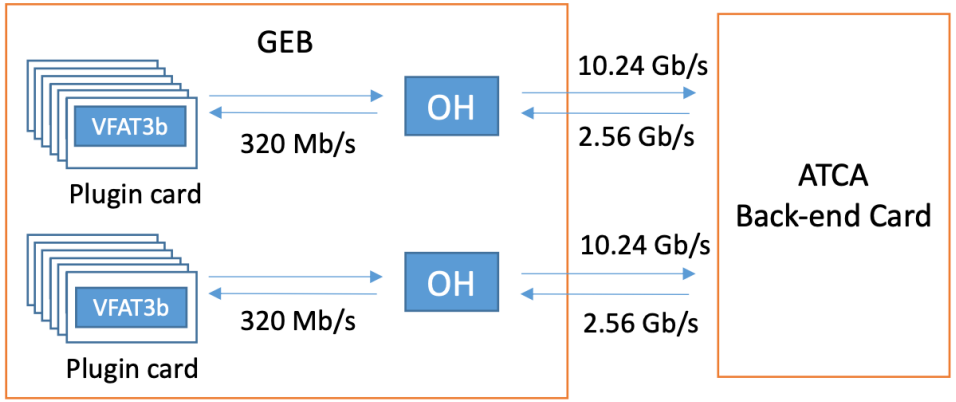


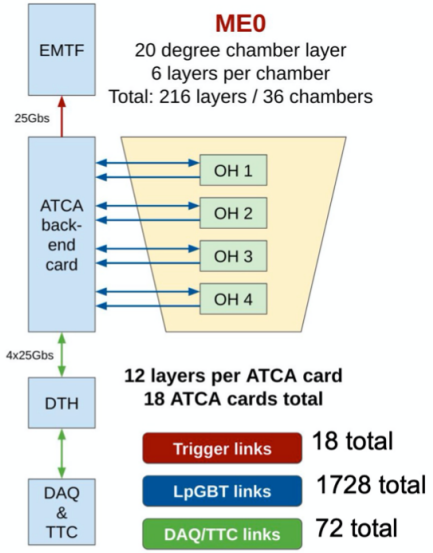
80 cm

24 VFAT3s

ME0 Electronics

- The FE should be able to readout data from strips every BX and have sufficient bandwidth to send both DAQ (for every L1A) and trigger data (every BX) to back-end
- The back-end should have enough bandwidth to accept L1A rate up to 1 MHz and sustain DAQ data rates up to 1.39 Tb/s; and also send 6-layers segments (trigger data) per BX to EMTF





- 128 strips per VFAT3b
- 1 VFAT3b per Plugin card
- 6 Plugin cards per OH

- 2 OHs per GEB
- 2 GEBs per layer

- 6 layers per stack
- 18 stacks per endcap
- 2 endcaps

X2O ATCA based back-end card (by UCLA, UF and Vinca)

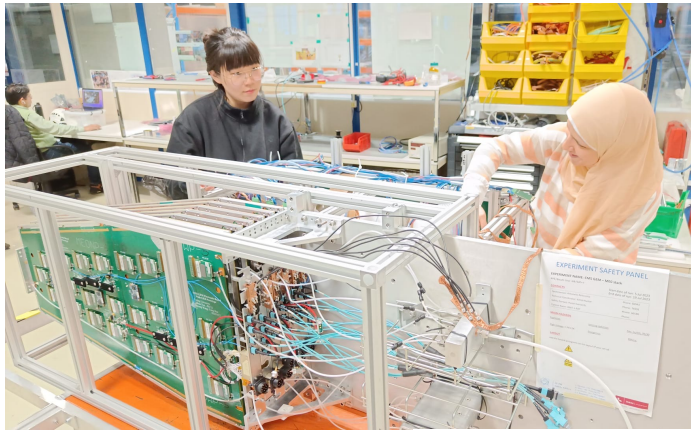
Back-end Firmware developed by TAMU and BU

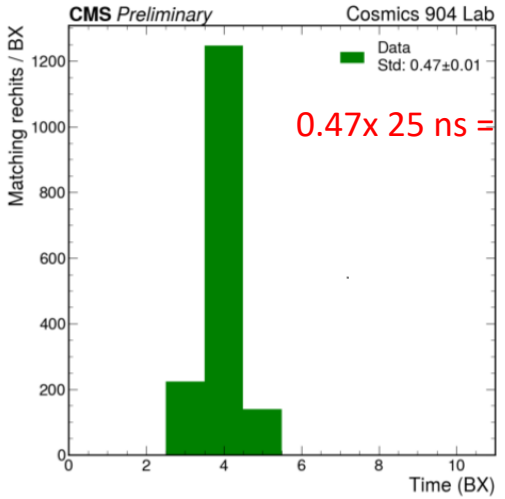
GEB: GEM Electronic Board
OH: Optohybrid

Note: GE1/1 & GE2/1 will also use X20 board & ATCA

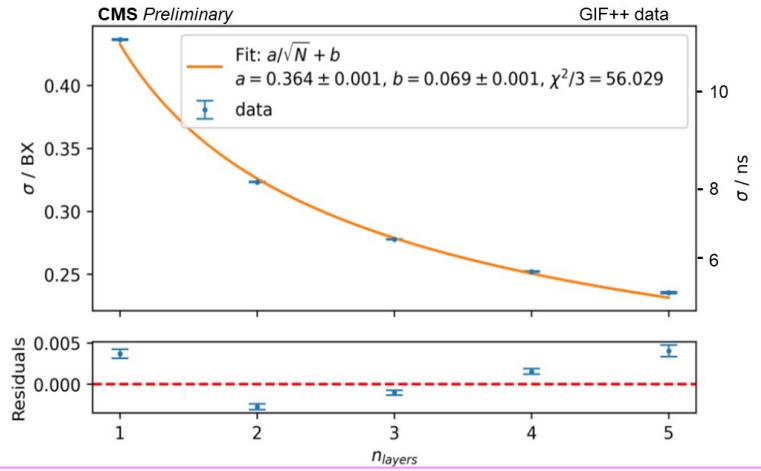
Latest results before production

Stack prototype in high intensity beam (GIF++):

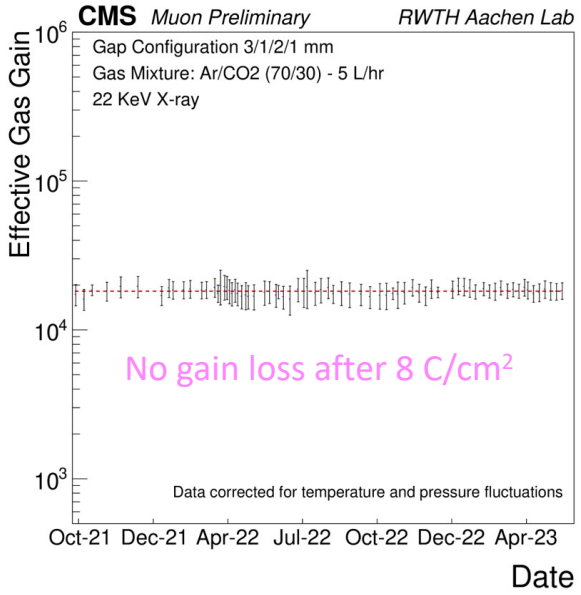




0.47x 25 ns = 11.7 ns



Ageing studies:



- Time line
  - Production starting in 2024
    - More than 30 detectors already assembled
    - All (255) GEBs produced
    - All (994) OHs produced
      - Note: 330 boards reproduced by the manufacturer after QC issue observed, mainly due to over-etching
    - 150 pre-series plug-in cards received
  - Next milestones
    - Assembly of 1 endcap (18 stacks) by Oct. 25

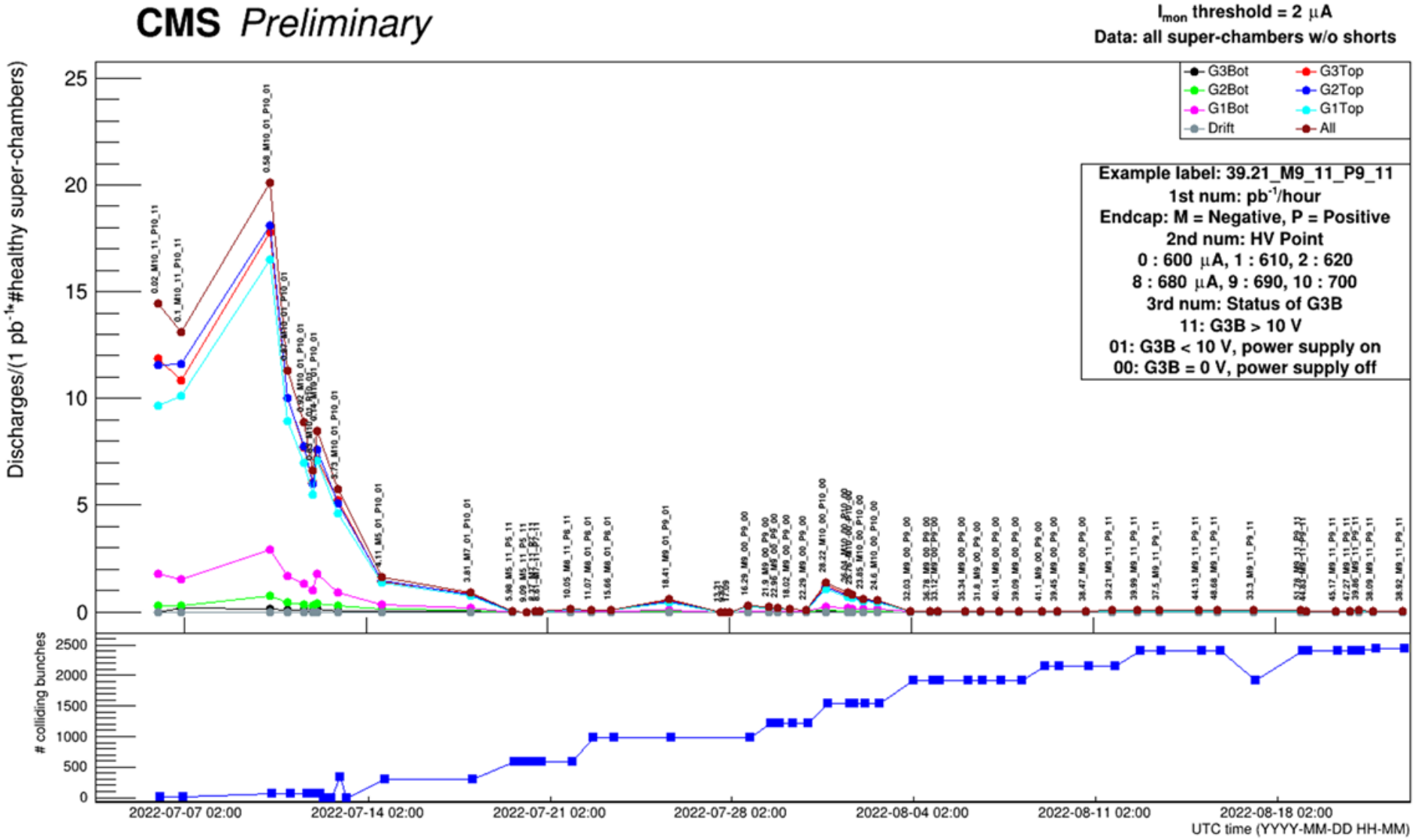
Conclusion

- CMS GE1/1 is performing very well
  - Overall efficiency: 94%
  - Main source (~7%) of inefficiency: due to VTRx outgassing
  - Plan for rework during LHC LS3
    - + replace the damaged VFAT3s
  - alignment & time resolution now allows to enable GE1/1-CSC ME1/1 combined trigger

- ME0 is now gearing to full production
  - Latest results from test beam show that we meet all the specs.

Back-up

Discharge rate



Impact of lpGBT Issues on ME0 Optohybrid (OH)

1. **Stuck at power up:**
   - lpGBT can get completely stuck, no communication possible, can recover with a powercycle
   - Probability of occurring ~1%. May depend on environmental conditions like temperature, power supply rise time, and TID
   - For ME0, this issue was observed and reported in Jan 2024. With a slower power up, the issue was resolved, at least at room temperature and 0 TID. All production electronics fabricated with this improved powering scheme
     - Out of 765 production OHs (1530 lpGBTs) tested so far with the slow power up, only 1 chip showed the issue (~0.06%)
   - Operating temperature (~15 C) not far from testing temperature (~30 C at chip)
     - All boards will still be tested with many power cycles with final system cooling during integration at CERN
   - Need to understand the effect of TID:
     - The CERN lpGBT team is performing radiation tests. Expected TID in ME0 (< 1 Mrad) much lower than specs for the chip
     - We are also considering radiation testing of 200 boards (rejected during production testing due to unrelated PCB issues but with good lpGBTs) – discussing with the lpGBT team to understand feasibility of this test
   - Worst Case scenario: if the issue shows up at P5, we can still try to powercycle (even if it does not have a 100% success rate). 1 LV channel only controls 4 OHs
2. **Equalizer attenuation:**
   - ~1% boards might have non-functional optical links due to incorrect default configuration of equalizer attenuation
   - Out of 765 production OHs (1530 lpGBTs) tested so far, few boards (~2.5%) discovered to have bad optical links (all may not be the same issue); they were already rejected
   - Additional screening (using recommended procedure from the lpGBT team using the on-chip eye diagram) will be performed during integration at CERN for final acceptance

ME0 LpGBT powering

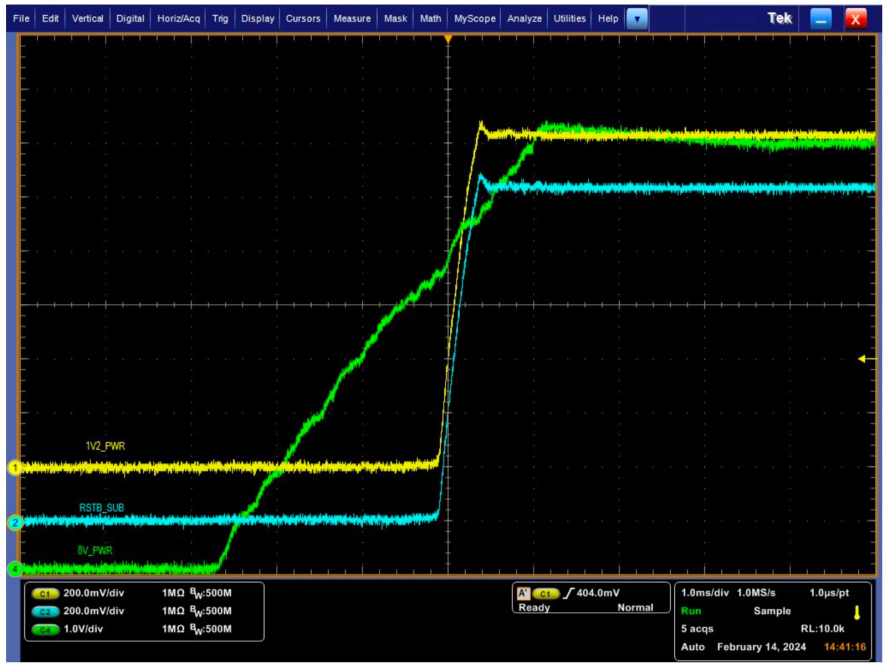
bPOL DC-DC with ~50ms Ramp Time of 8V

- bPOL DC-DC output on 1V2 has a stable shelf at 0.4 V when the 8V input ramps up slowly.
- Never see a failure appear with this power-on sequence.
- All 23 boards have passed 2-10k powercycles with this configuration

Works

bPOL DC-DC with ~5ms Ramp Time of 8V

- 0.4V shelf does not appear
- This configuration fails at a 9% for sub case, and 85% for the boss case.
- Note: Never fails when powered by QUESO. We control the 1.2 V directly with rise time ~1 ms.

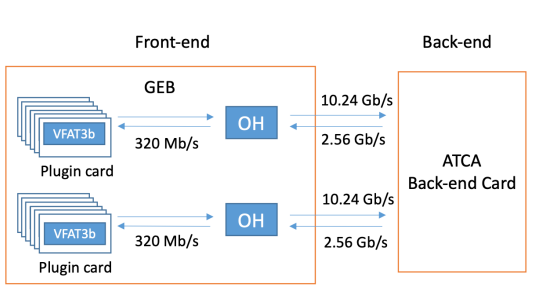


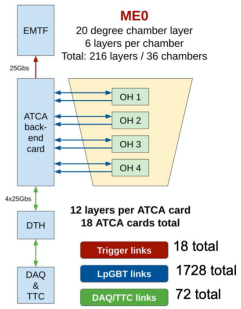
Doesn't work

ME0 bandwidth

DAQ data path:

- Same as GE2/1 (using lpGBT in ME0 instead of GBTX in GE2/1)
- VFAT sends data over 1 elink at 320 Mb/s to the lpGBT on the OH
- Data serialized & sent over optical links to backend (builds events from multiple VFATs & modules)
- Enough bandwidth to run up to 1.6 MHz of L1As without zero suppression (192 bits per packet)
- From simulation, estimated total DAQ rate of 1.39 Tb/s from ME0 at PU=200 (more details here)





- 128 strips per VFAT3b
- 1 VFAT3b per Plugin card
- 6 Plugin cards per OH

- 2 OHs per GEB
- 2 GEBs per layer

- 6 layers per stack
- 18 stacks per endcap
- 2 endcaps

GEB: GEM Electronic Board
OH: Optohybrid

Trigger (S-bit) data path:

- Different from GE2/1 - S-bits sent directly to backend without compression (no FPGA on ME0 OH)
- S-bits sent over 8 elinks from VFAT to OH at 320 Mb/s, each elink carries data for 8 S-bits (64 S-bits in total per VFAT per BX)
- S-bit rate is constant, and all the needed bandwidth is dedicated to this on the lpGBT, so it is guaranteed that all S-bits are sent to the backend every BX
- On the backend, the segment finder uses S-bits to find up to eight 6-layer segments per BX per stack (40 bits per segment) and sends to EMTF (at 12.8 Gb/s) over 25 Gb/s links (1 per stack)

Bandwidth:

	6 x VFAT3 fast control slow control DAQ packets	6 x VFAT3 sbit data	2 x LpGBT slow control	2 x LpGBT Forward Error Correction	**Total per OptoHybrid**
Backend TX	1.28Gb/s	N/A	0.16Gb/s	0.96Gb/s	**2.4Gb/s**
Backend RX	1.92Gb/s	15.36Gb/s	0.16Gb/s	1.6Gb/s	**19.04Gb/s**

Table 1: bandwidth breakdown of the OptoHybrid interface (for each OptoHybrid)

Sufficient bandwidth in both front-end and back-end to support expected data rates

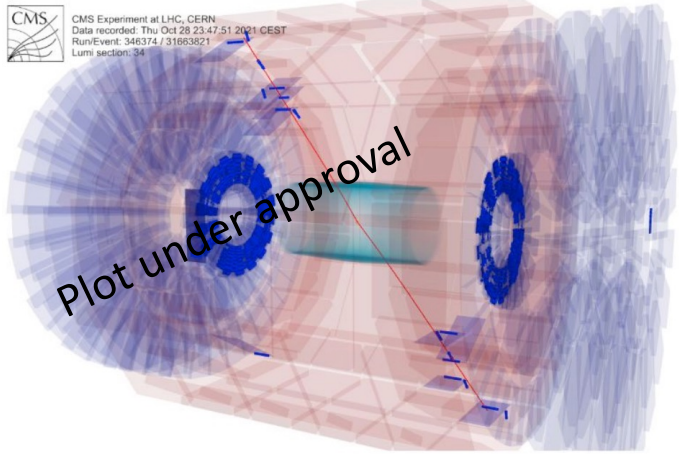
1 link per OH (only to 1 lpGBT per OH) at 2.56 Gb/s

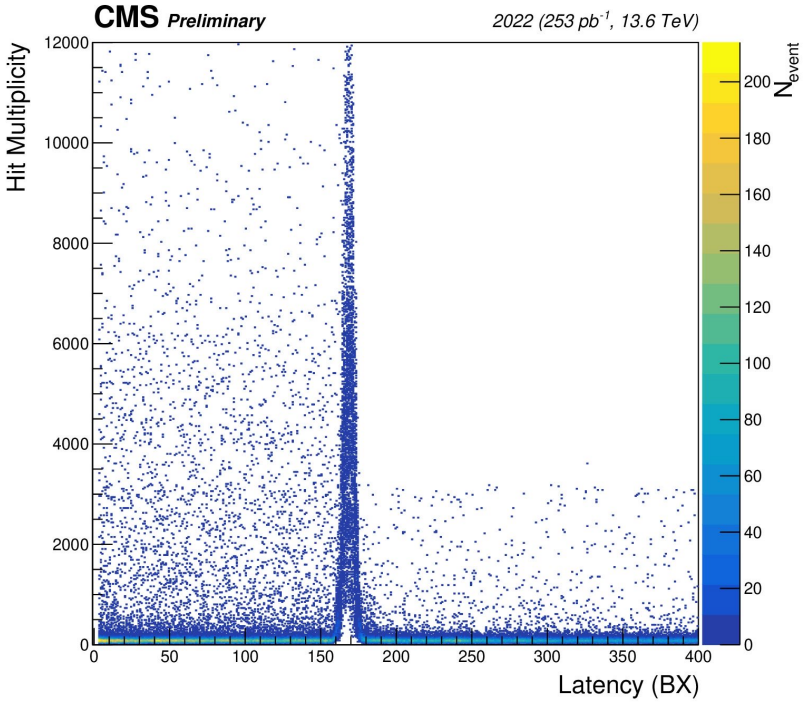
2 links per OH (1 per lpGBT) each at 10.24 Gb/s

1 S-bit = OR of 2 strips

High multiplicity events

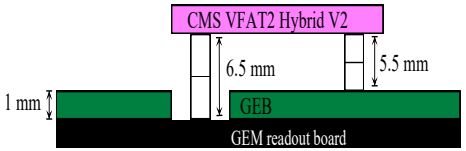
- Upon L1A, the instantaneous current drawn in the digital power domain of the VFAT3 induces a signal/noise in the analog power domain. This spurious signal happens ~160 Bunch Crossings later.
- A filter with a multi-BX (Bunch Crossing) window has been implemented to minimize the fraction of high multiplicity events. The number of high multiplicity events still passing the filter is O (5%).
- Filter is applied on trigger path; not on DAQ path





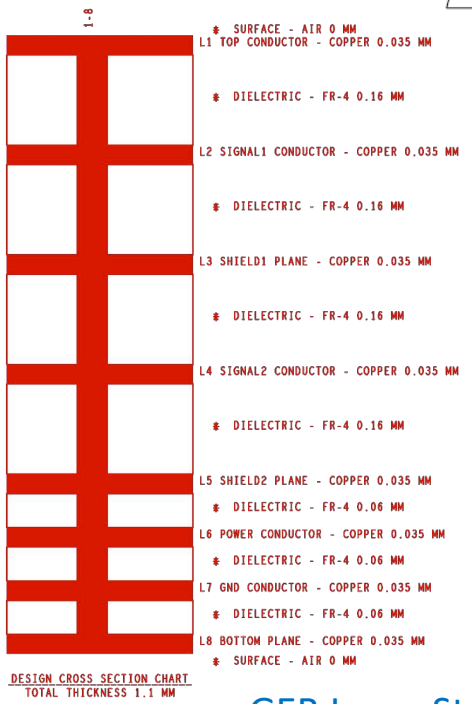
v3 Electronics - GEB

- The GEB is limited to a thickness of ~1mm
- This limits the possible layers:
  - 1 power plane
  - 1 GND plane
  - 2 signal layers
  - 1 shield layer

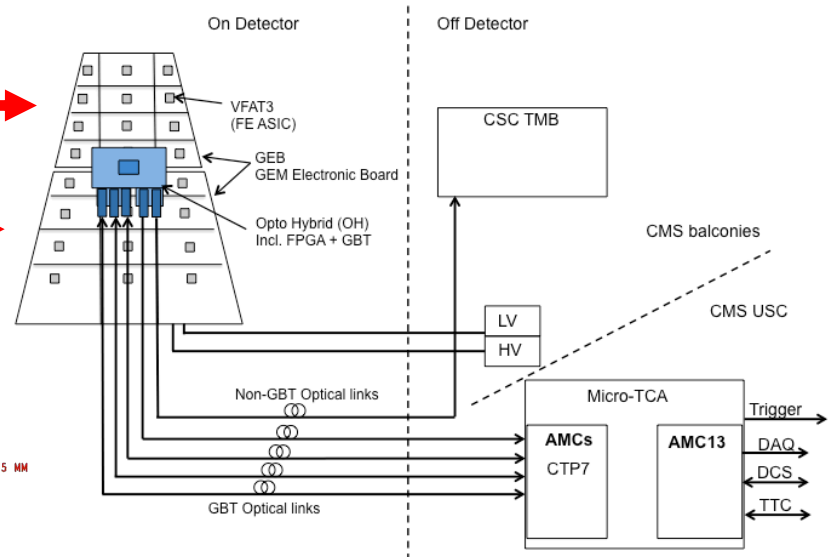


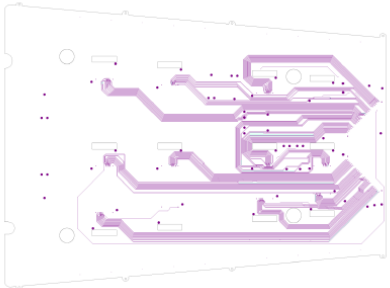
Location of the GEB in the detector

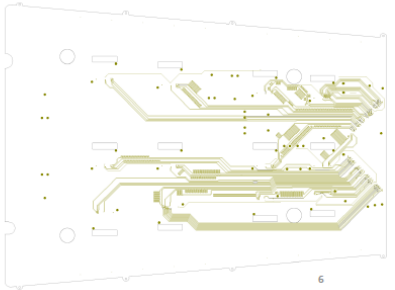
- The shield layer between the GEB signal lines and the read-out board was added after our experience from the slice test.



GEB Layer Stack



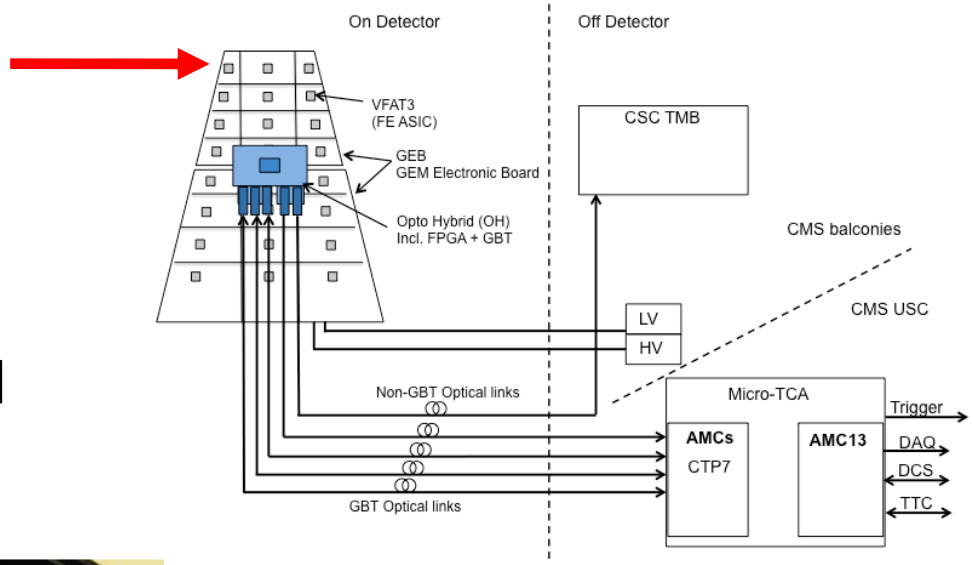


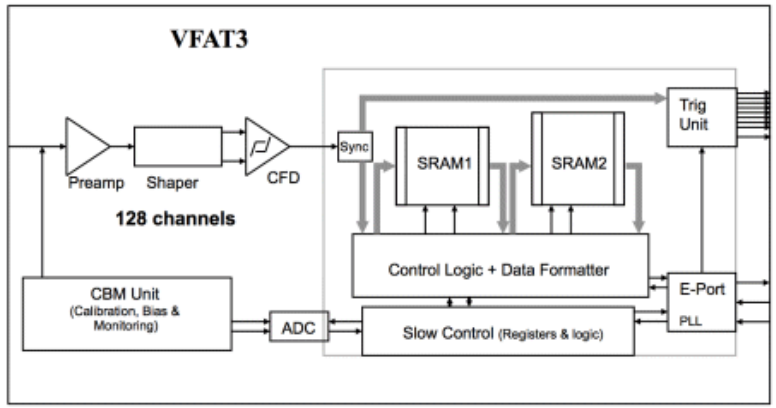


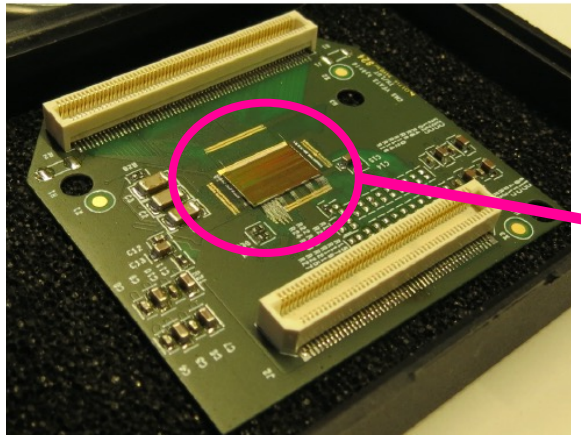
GEB Signal Layers

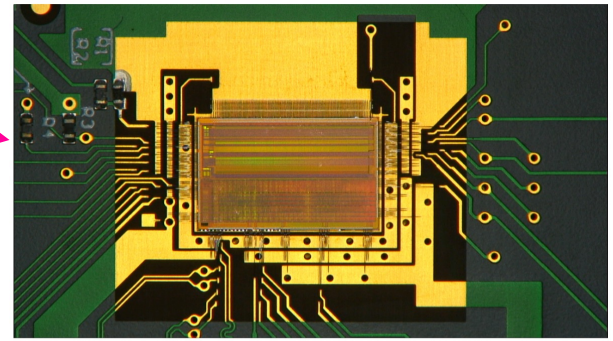
v3 Electronics – VFAT3

- 24 sectors, each routed to an ASIC-based VFAT3 hybrid chip
  - 320 MHz: 4x higher frequency than VFAT2
  - L1 latency up to 12.5 µs
  - Trigger data: 1 bit = OR of two strips (VFAT2 had 1 bit = OR of 16 strips)



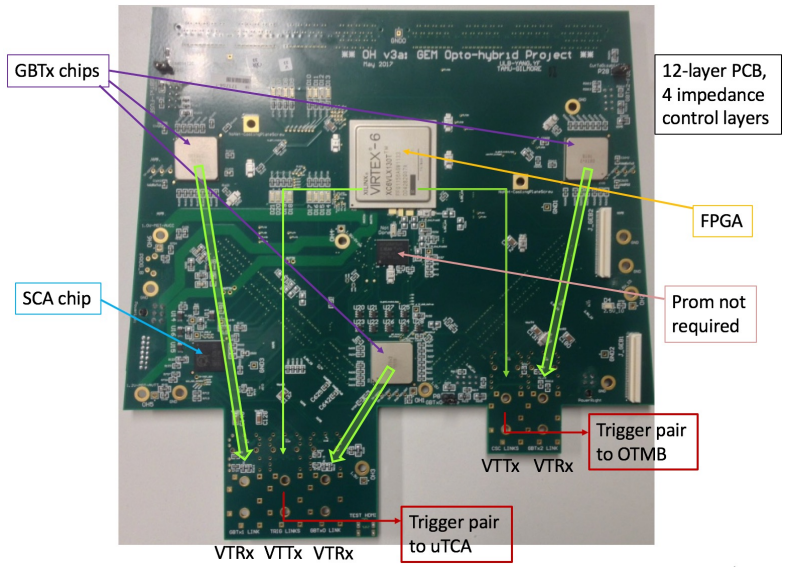




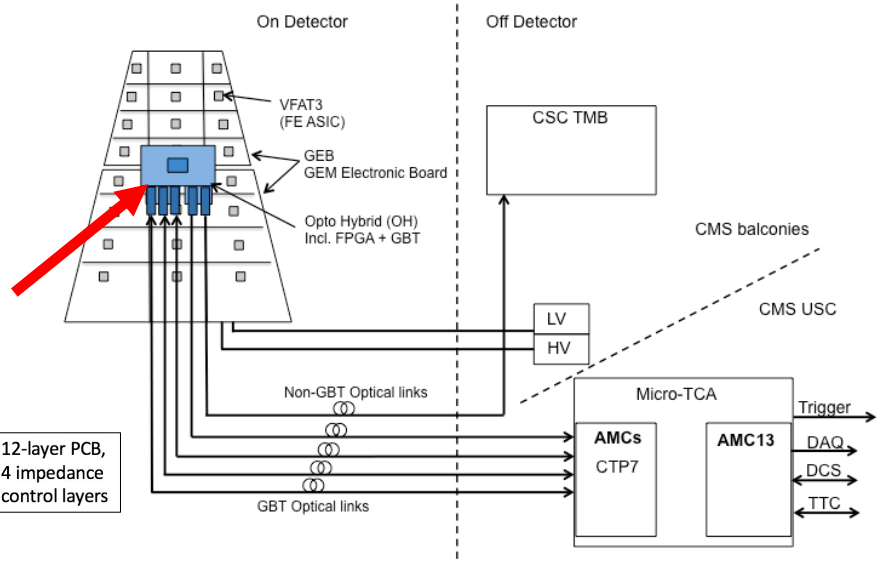


v3 Electronics – Optohybrid

- In the center, attached to both boards, is an optohybrid (OH) mezzanine card, whose main features are a Xilinx Virtex-6 FPGA and three GBTX chips.
- The v3 optohybrid is promless – fast, promless programming of the FPGA directly from the CTP7 is achieved in 70ms. This removes the need for one FEAST.

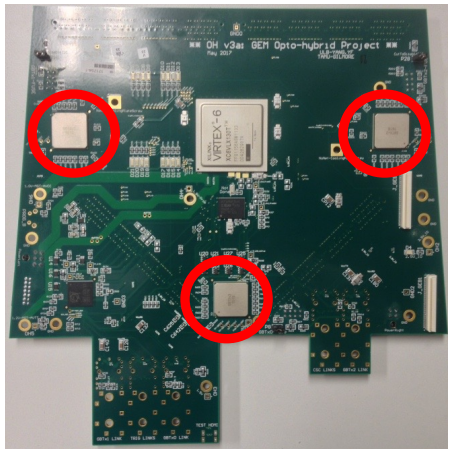


Optohybrid (OH)

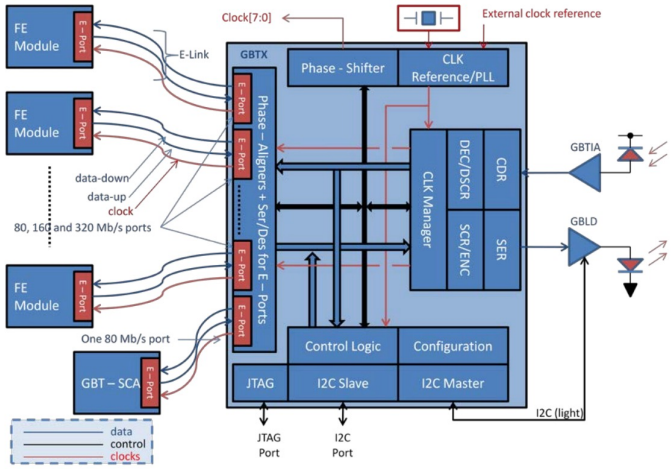


v3 Electronics - GBTXs

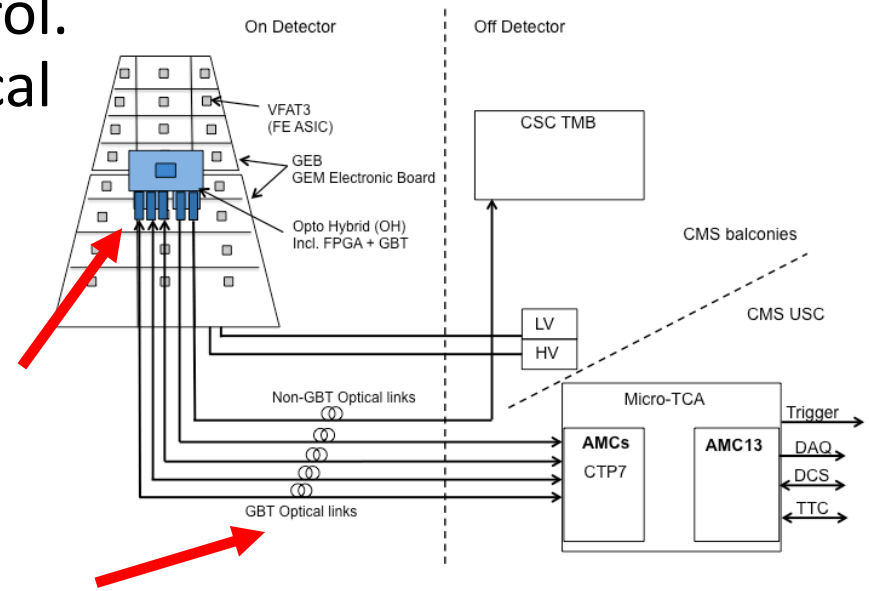
- The GBTXs are responsible for tracking and slow control. They drive communication through bidirectional optical links to/from the back-end electronics
- They can be minimally fused to lock to the fiber link, recover the clock, and keep a certain configuration even after power loss.



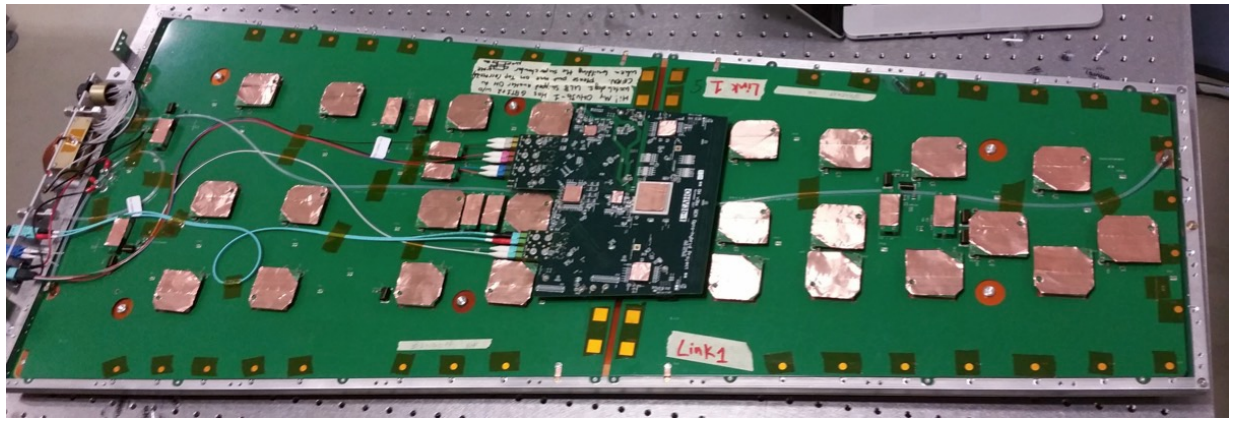
Optohybrid (OH)

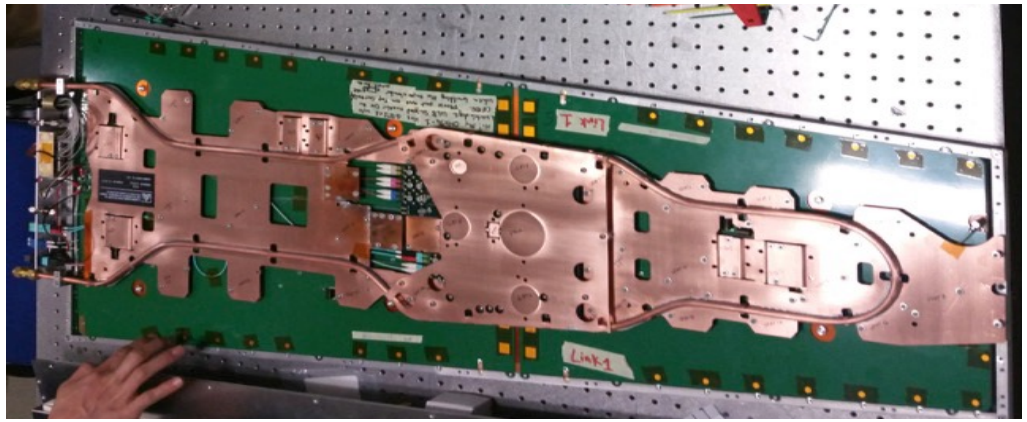


OH Architecture and Interfaces



v3 Electronics – Full Detector Assembly





Credit: Gilles De Lentdecker