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Performance of the CMS GE1/1 system at LHC Run-3 and prospects of the future ME0 system

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We present the running experience of GE1/1, a new muon tracking and triggering station made of Triple-GEM detectors installed in the most forward region of the CMS muon spectrometer. GE1/1 records data since 2022. Each of the 144 detectors has 24 VFAT3, 3 GBTx, 3 VTRx, 2 VTTx and a Virtex-6 FPGA. All powered by 10 FEAST DCDC converters. We will present the GE1/1 electronics performance over the first 2 years of running at LHC. We will also present the lessons learned and the improvements expected for the next 2 stations to be built, GE2/1 and ME0.

Summary (500 words)

GE1/1 represents the pioneering phase-2 upgrade within the CMS HL-LHC program. Comprising 144 triple-GEM detectors, each spanning 1.2 meter in length, this innovation has been integrated into the forward region of the CMS muon endcap, actively collecting data since the onset of LHC Run-3 in 2022. Serving as a precursor to two additional triple-GEM stations, GE2/1 and ME0, slated for installation within CMS in the near future.

Each GE1/1 detector is read-out by 24 VFAT3 chips, binary chips endowed with 128 channels, delivering essential trigger and tracking data. This data is subsequently relayed via a large PCB, known as the GEM Electronics Board (GEB), to a compact mezzanine, the Opto-Hybrid (OH), positioned at the heart of the GEB. The OH encompasses essential components such as 1 Virtex-6 FPGA, 3 GBTx and 1 SCA chips, complemented by 3 VTRx and 2 VTTx optical modules. The optical communication with the xTCA backend boards, notably the CTP7, is made through versatile links. Powering this intricate front-end electronics setup are 10 FEAST DCDC converters.

In this contribution we will report about the performance of this novel system over its initial two-year deployment at the LHC. Addressing challenges posed by instabilities affecting up to 10% of the bi-directional optical links, attributed to outgassing in the VTRx assembly. A predicament necessitating resolution during the upcoming Long Shutdown (LS3) of the LHC, wherein all GE1/1 chambers will be temporarily extracted from CMS for refurbishment.

Furthermore, we will delve into the insights gleaned from these operational experiences, informing enhancements in the electronics architecture of forthcoming GE2/1 and ME0 systems. These enhancements span various domains, including improvements of the VFAT3 protection circuits against discharges, introduction of mechanical flexibility between front-end PCBs, and refinement of timing resolution, among others.

Finally, we will outline the comprehensive refurbishment blueprint for GE1/1 during LS3, encompassing the transition to the ATCA standard for the backend electronics. Additionally, we will provide updates on the production status of ME0, alongside the latest findings from pre-series evaluations.

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