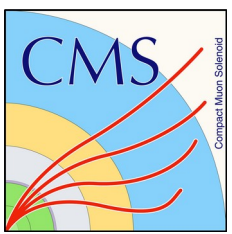
HGCAL SiPM-on-Tile Full-Stack Integration with the Serenity Phase-2 DAQ Hardware

Fabian Hummer on behalf of the CMS collaboration

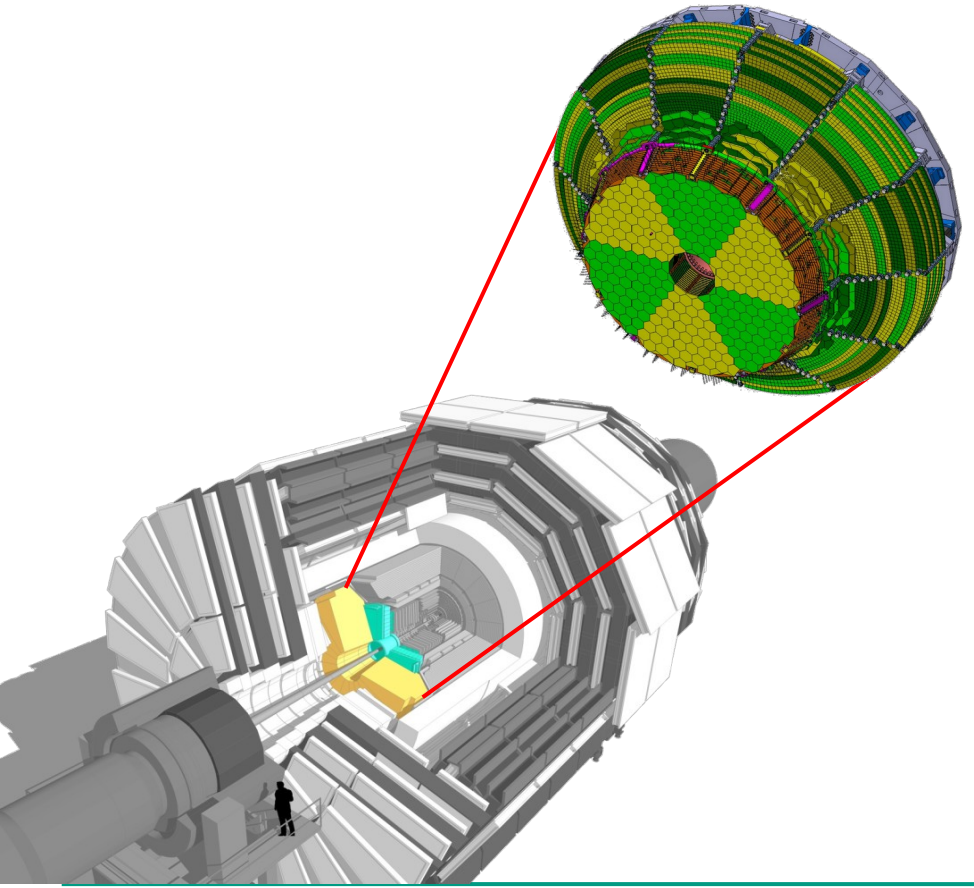
Contribution to
TWEPP 2024

3rd October 2024



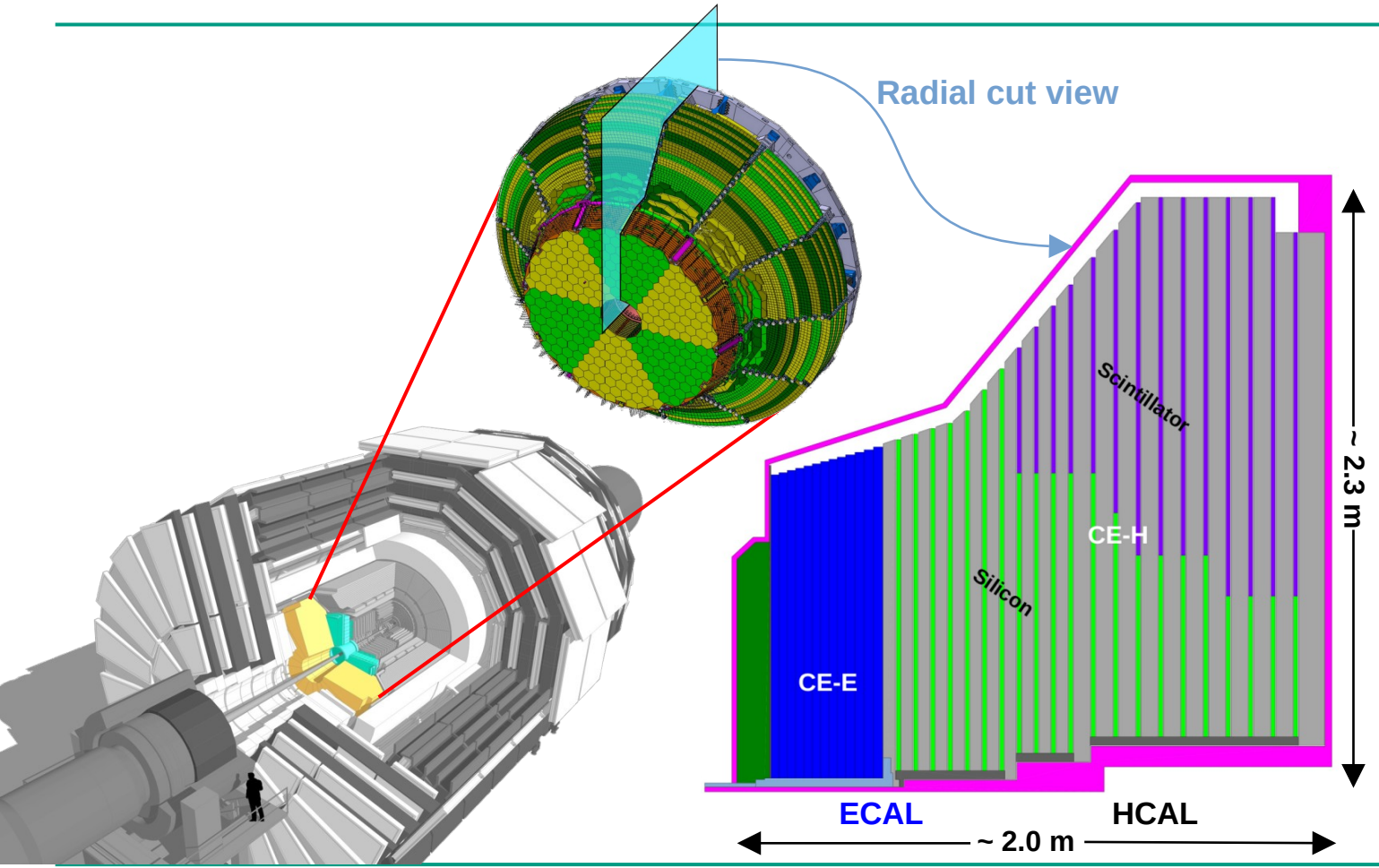
IMPERIAL

CMS needs fresh endcap calorimeters...



… and that’s how they will look like

HGCAL in a nutshell



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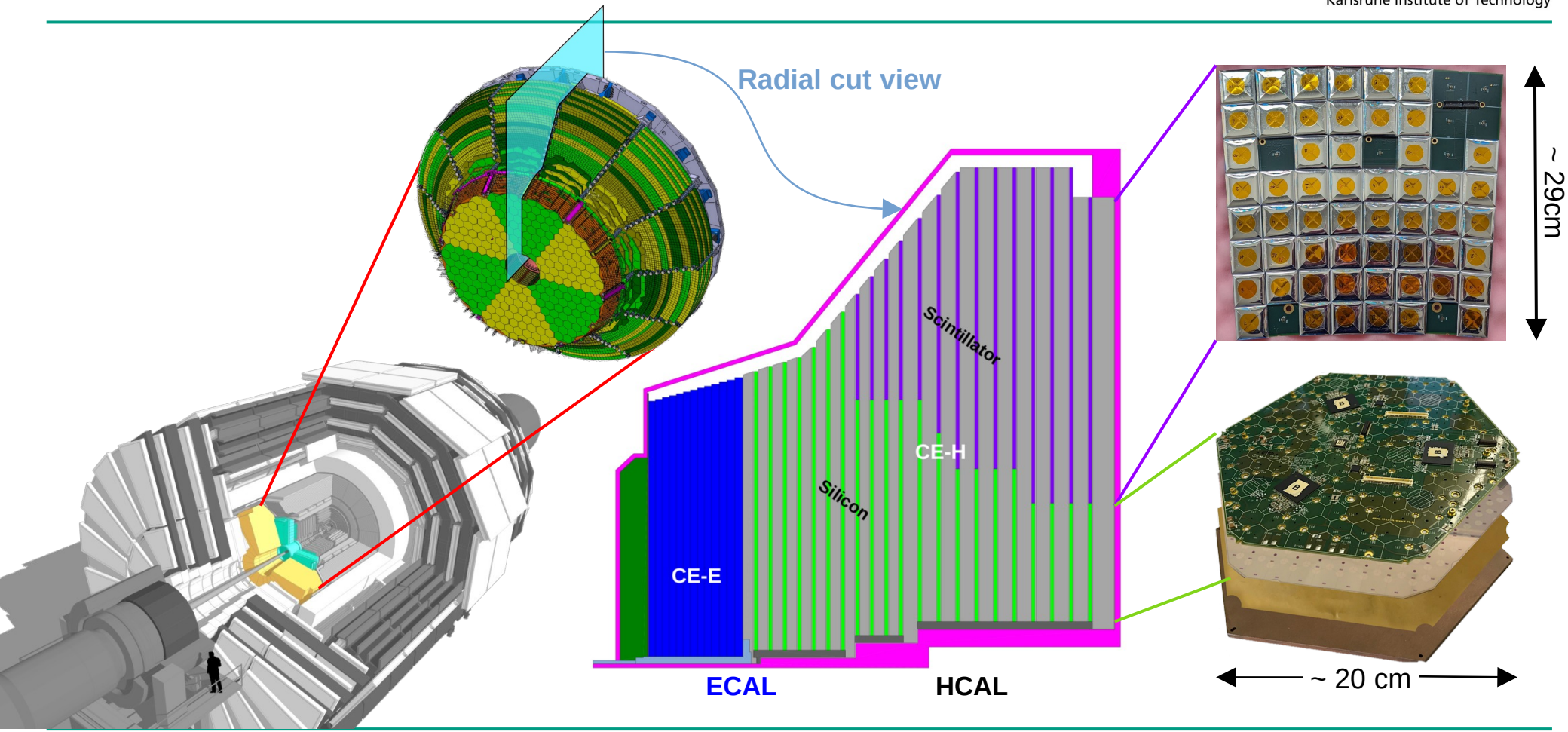
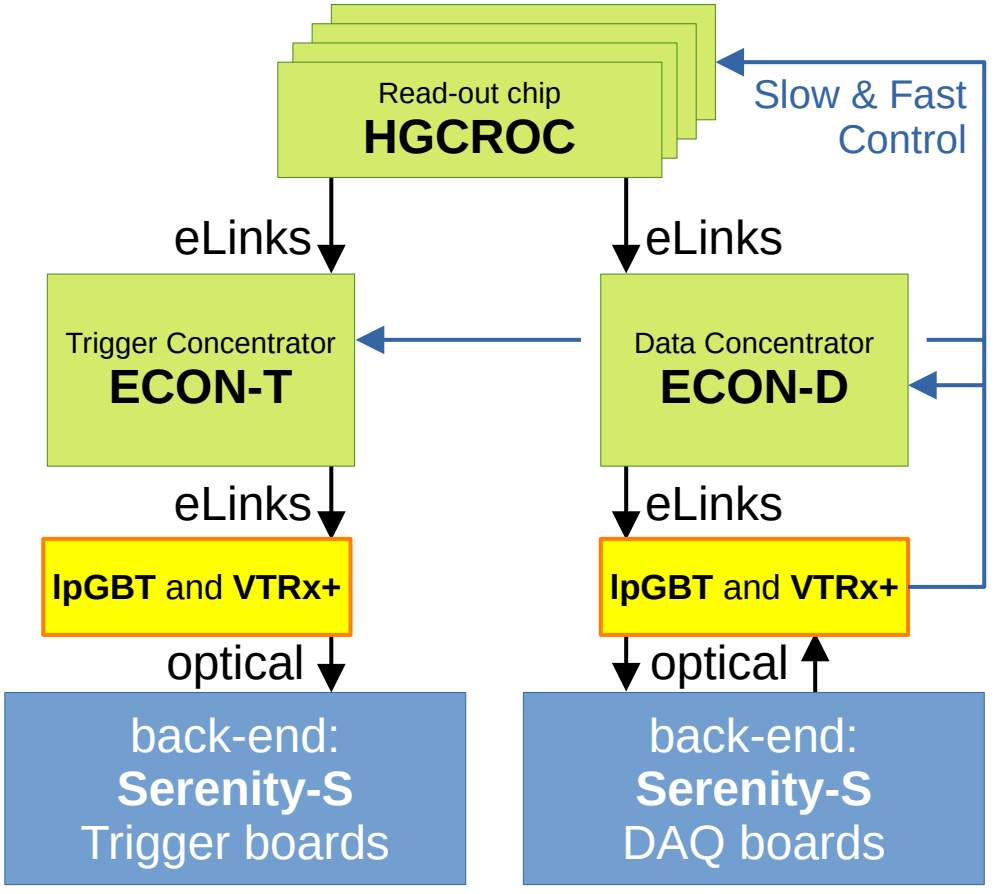


The HGCAL Readout Chain

- Trigger data:
  - Sent for each bunch crossing
  - Reduced formats, e.g. sum of multiple sensor cells
- DAQ data:
  - Full event information (ADC/ToT + ToA)
  - Only sent on demand (L1 trigger accept)



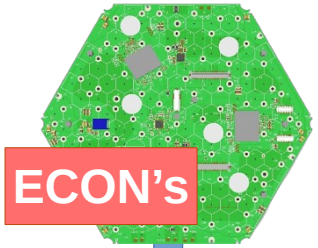
Detailed info on the data concentrators:

TWEPP 2024 ASIC Session

[Talk] J. Hoff: ECON-D and ECON-T: Design and Production Testing

[Talk] M. Lupi: Functional Verification for Endcap Concentrator ASICs in the High-Granularity Calorimeter Upgrade of CMS

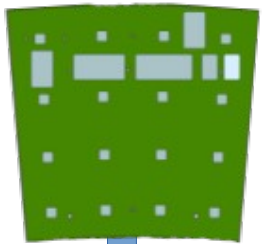
Core Feature: shared* Readout Chain



Wagon

ECON's

Engine



Wingboard

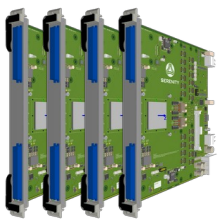
Motherboard

ECON's

Detector module
HGCROC (SiPM and Silicon version)

Passive connector board
different shapes → integration

Motherboard
Data to fiber optics (lpGBT, VTRx+)

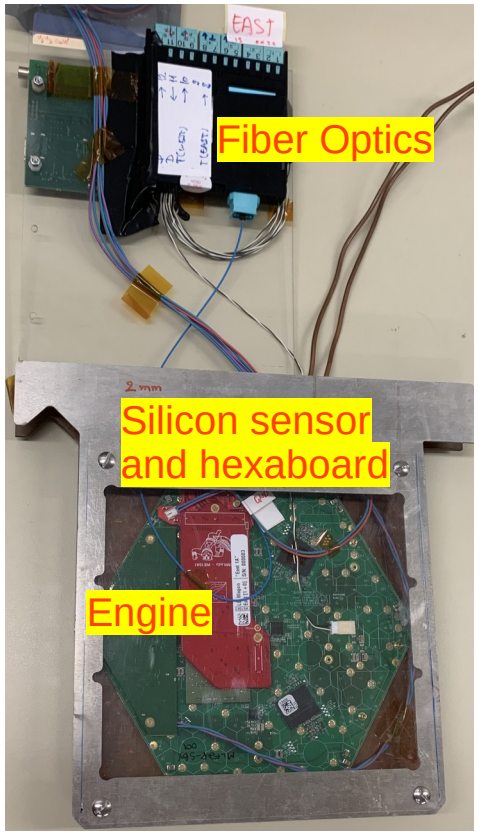


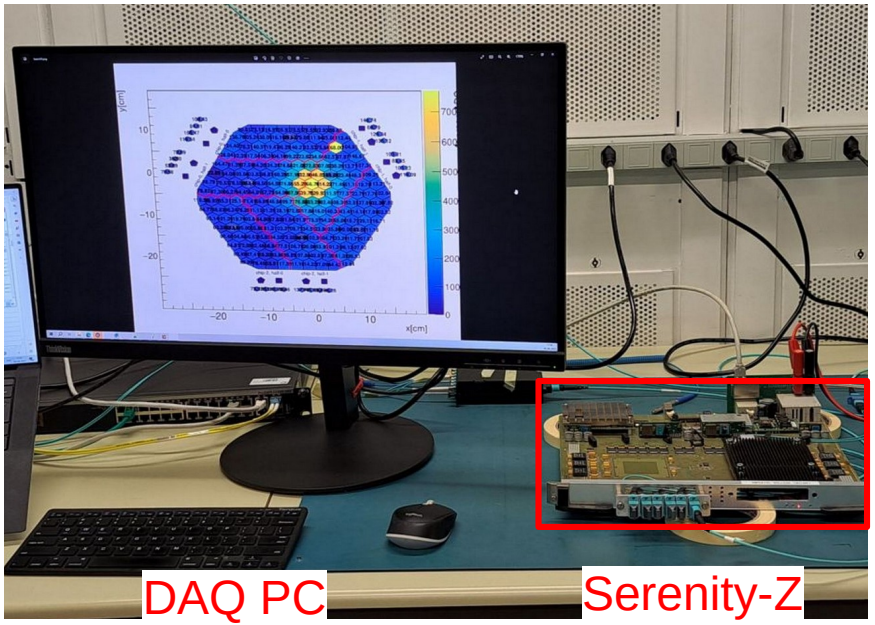
Back-end
- Serenity S1

* with some specific parts to each

1 year ago: First integration of full vertical slice

Beam Area: Front-end Control Room: Back-end





2023: beam tests at SPS:

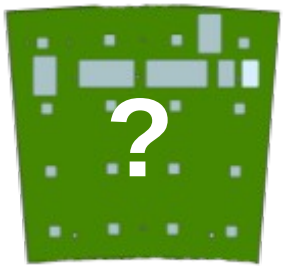
- Two sensor modules with the complete pre-series front-end
- Full readout chain until the Serenity
- First time this system was in a beam test!

→ **a huge success for HGCAL!**

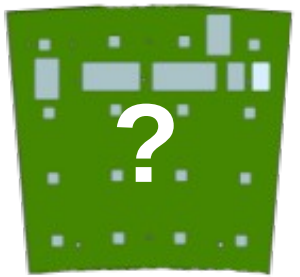
TWEPP 2023
[Talk] R. Shukla: The CMS HGCAL trigger data receiver
[Poster] M. Vojinovic: CMS HGCAL Electronics Vertical Integration System Tests

1 year ago: First integration of full vertical slice

Beam Area: Front end Control Room: Back end



But wait… what about the scintillator tile modules?



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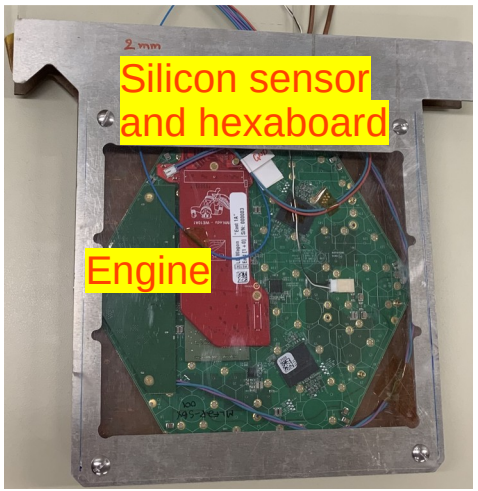

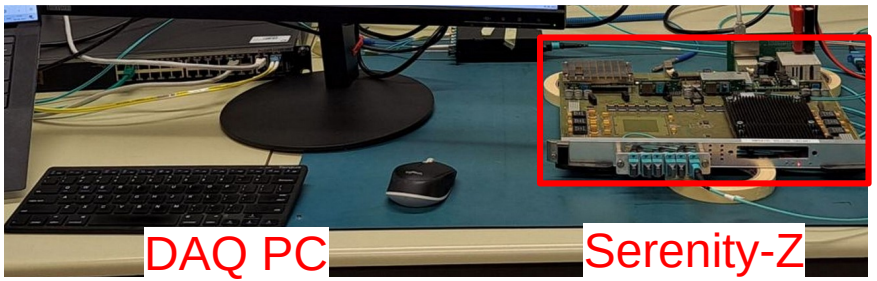

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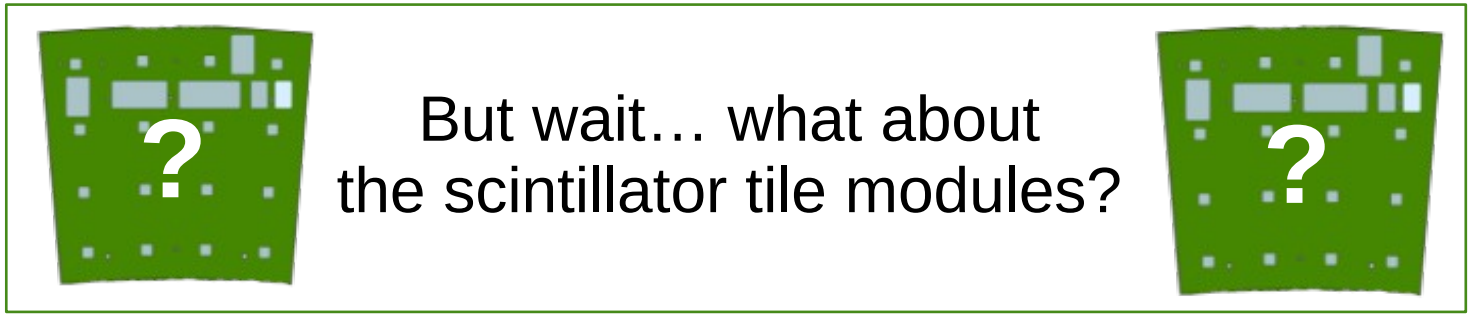
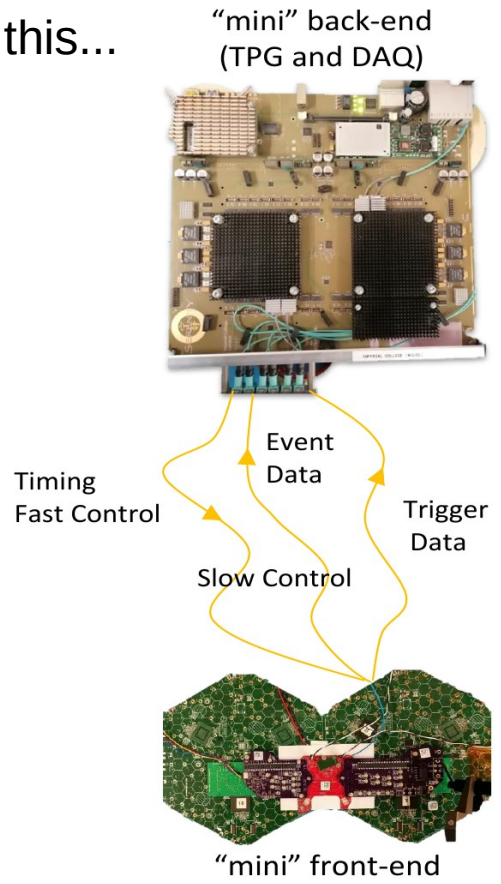


[Figure by M. Voijnovic]



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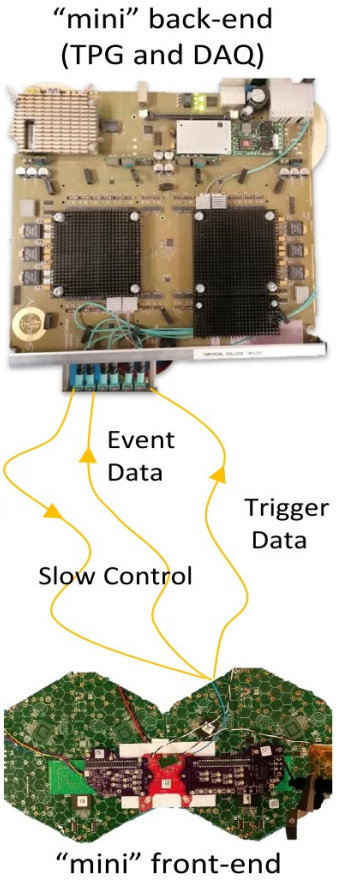

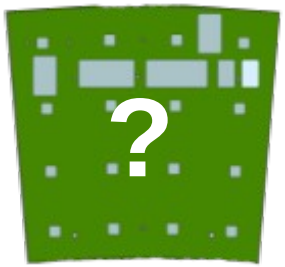

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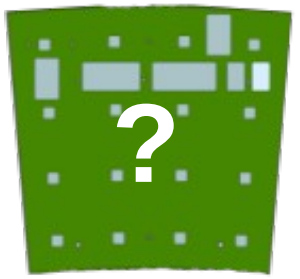
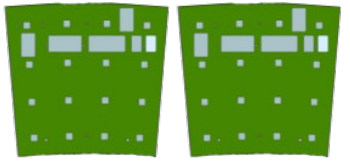


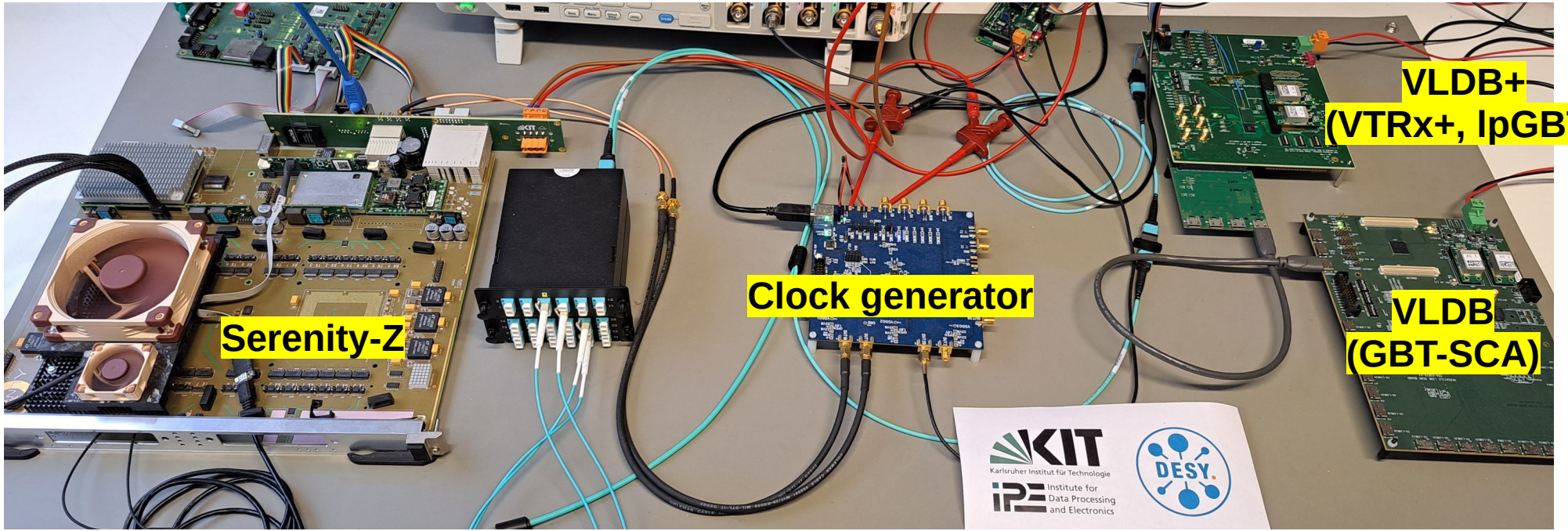
Tileboards



… can we simply REPLACE ???

Tileboard → Serenity readout: Step 1

- GBT-SCA provides I²C, GPIOs, ADCs, DACs to tileboards, *not present on silicon modules*
- GBT-SCA on Versatile Link Development Board (VLDB), lpGBT and VTRx+ on VLDB+
- Custom adapter board to test GBT-SCA connection via lpGBT eLinks



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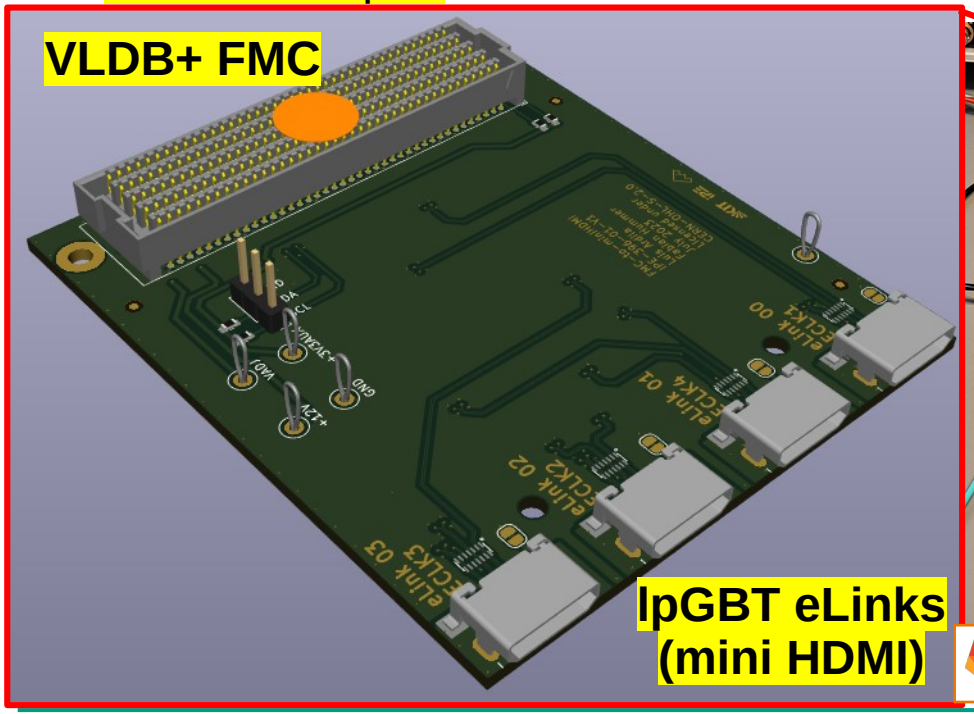
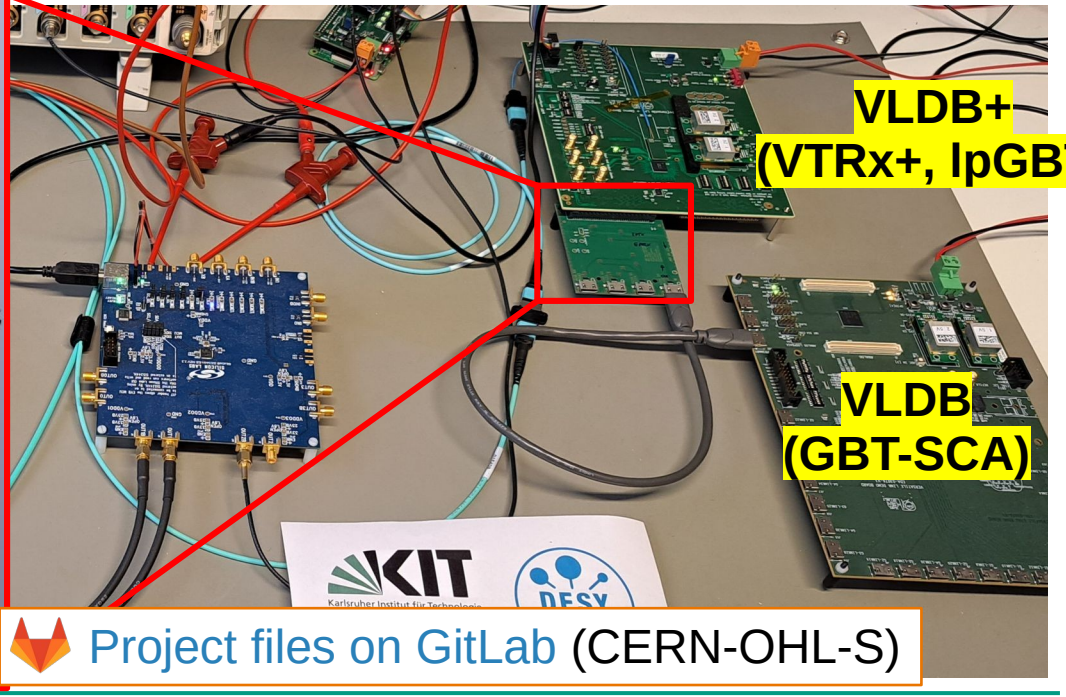
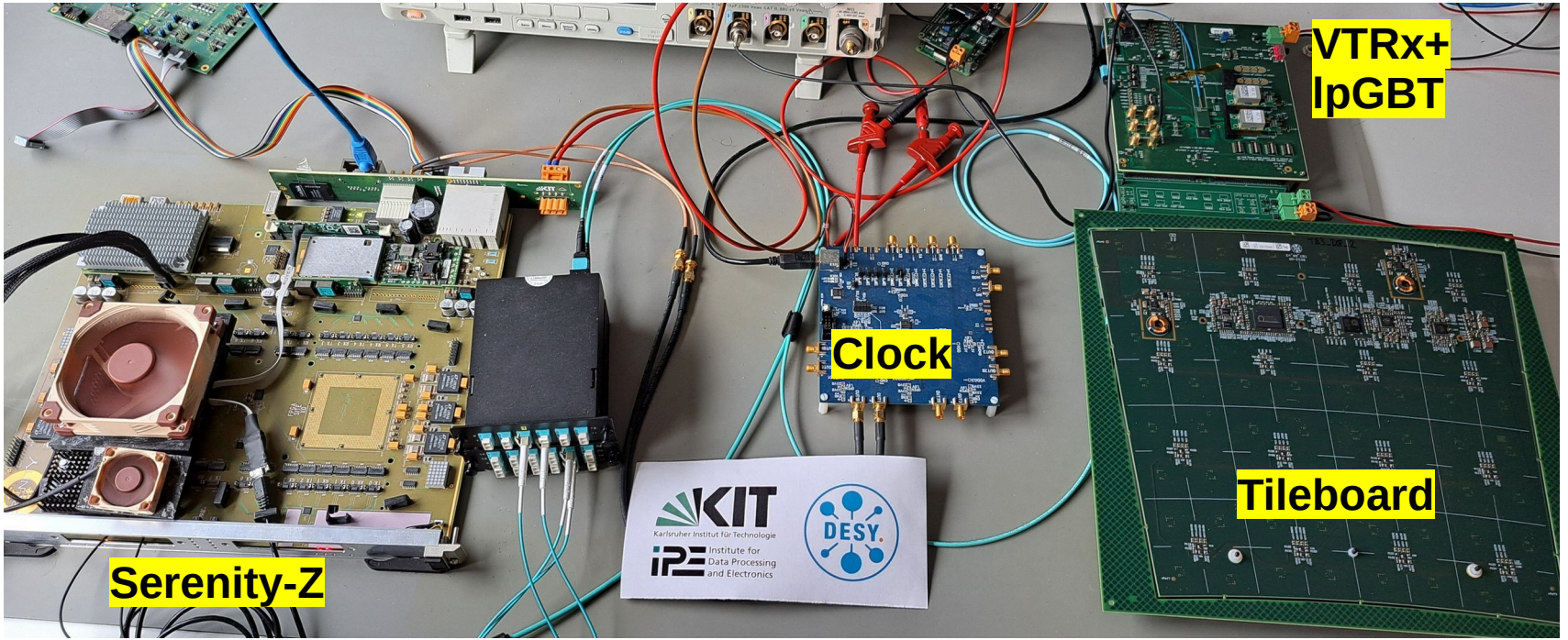




Project files on GitLab (CERN-OHL-S)

Tileboard → Serenity readout: Step 2

- Fall 2023: motherboard not yet available → **VLDB+ = „motherboard without ECON's“**
- Custom adapter board to connect tileboard to VLDB+ → develop FW and SW
- First readout of tileboard data with Serenity in January 2024



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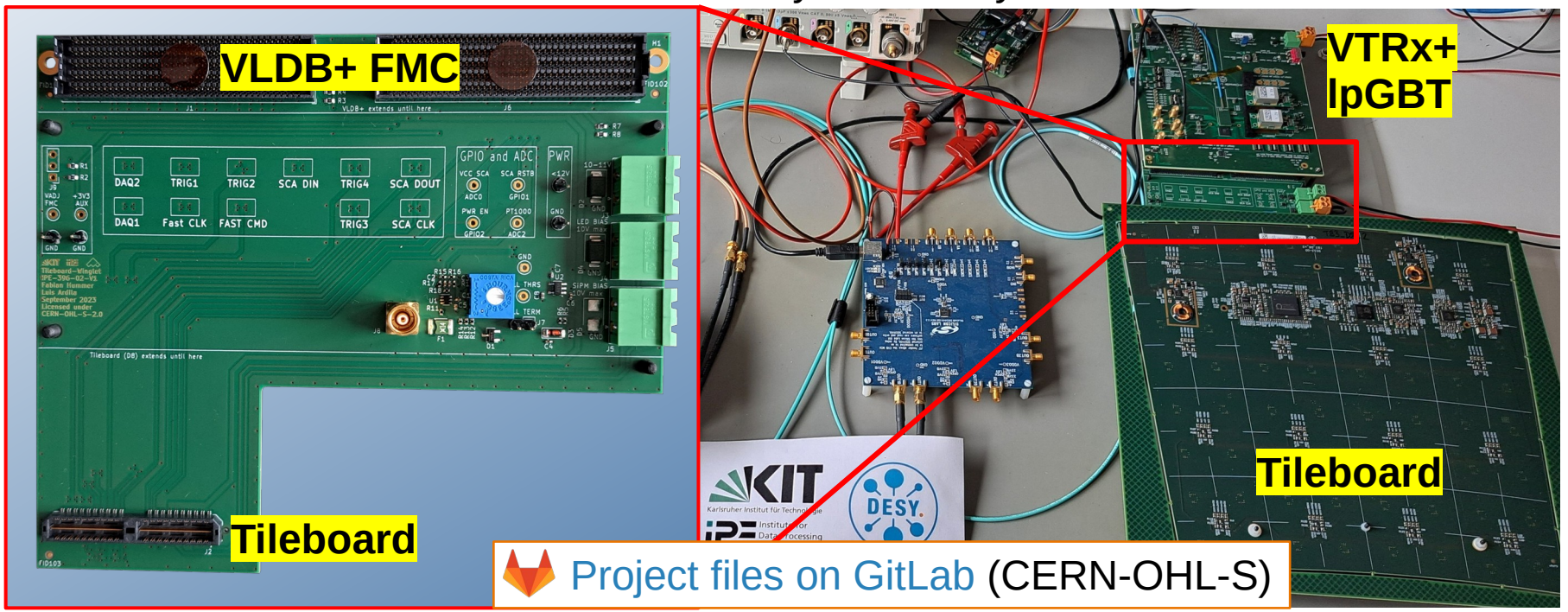
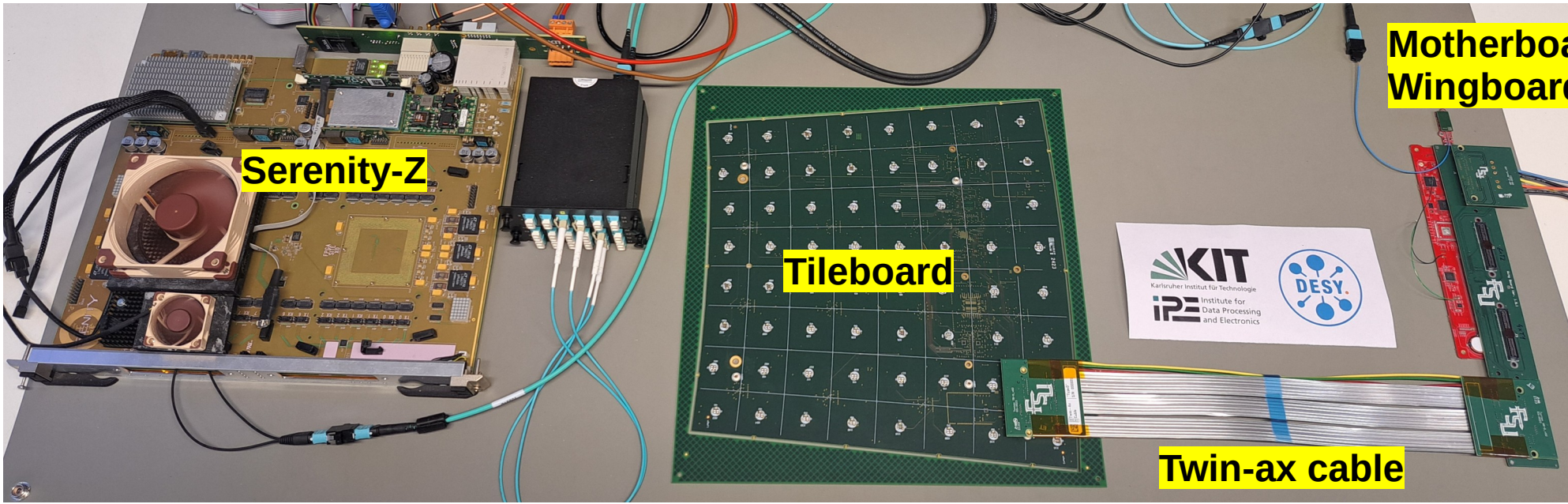


Tileboard → Serenity readout: Step 3

- Winter 2023: two pre-series motherboards assembled at KIT
- Motherboard with two ECON-T's, but no ECON-D (additional lpGBT instead)
- Characterization of full vertical stack with Serenity-Z1.1



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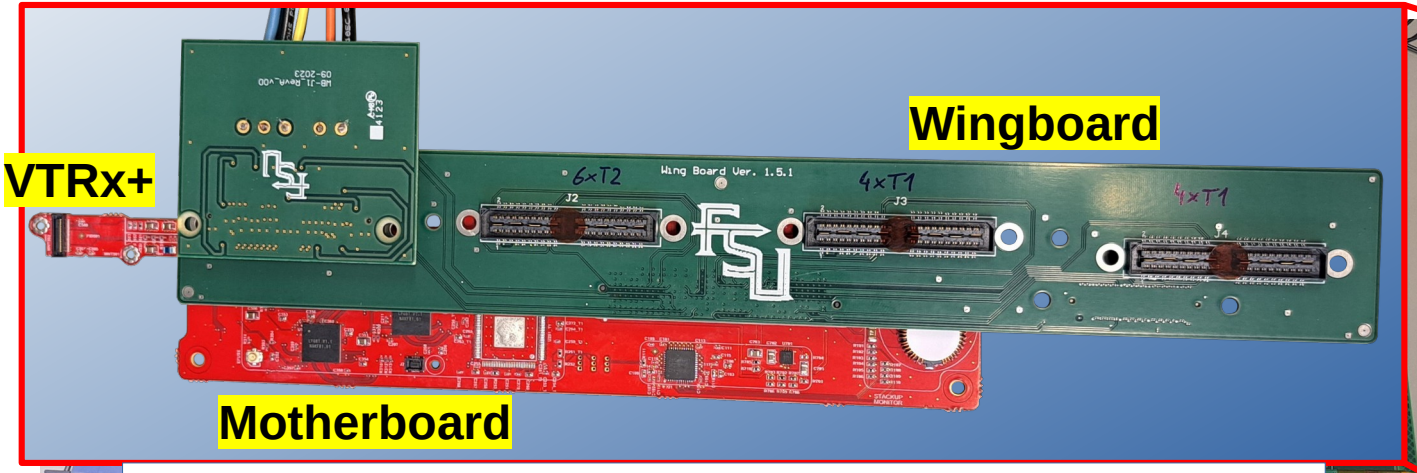
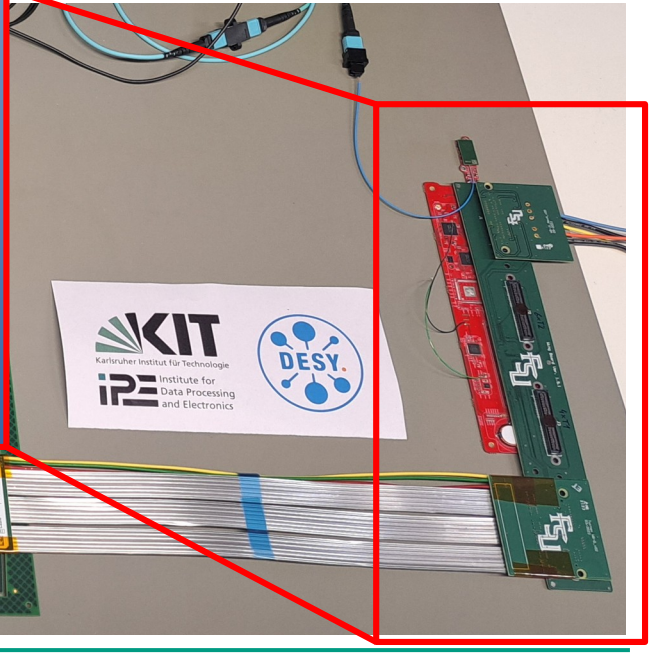
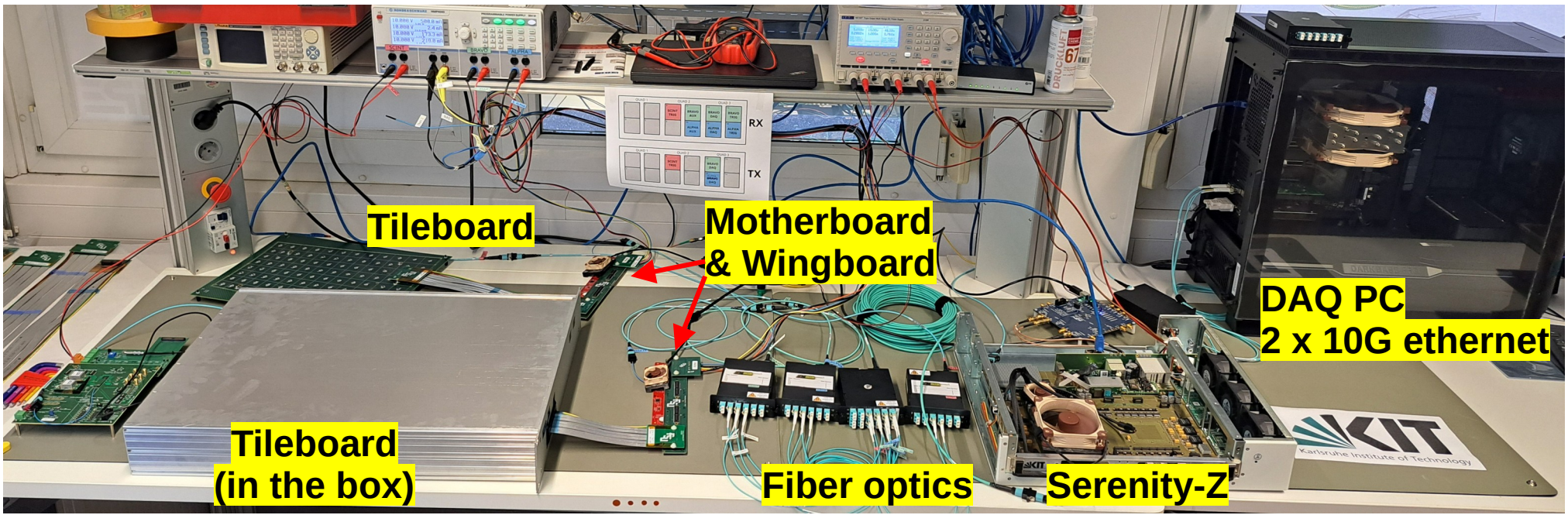




Many thanks to:
University of Minnesota
University of Notre Dame

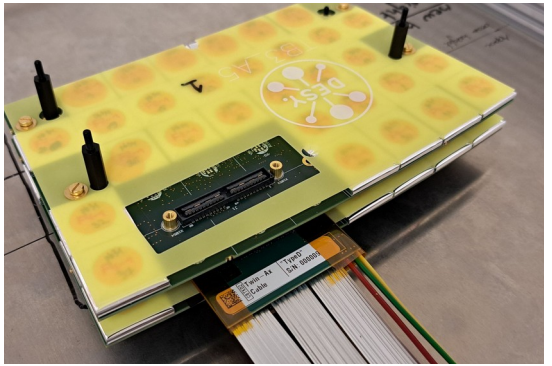
Tileboard → Serenity readout: Step 4

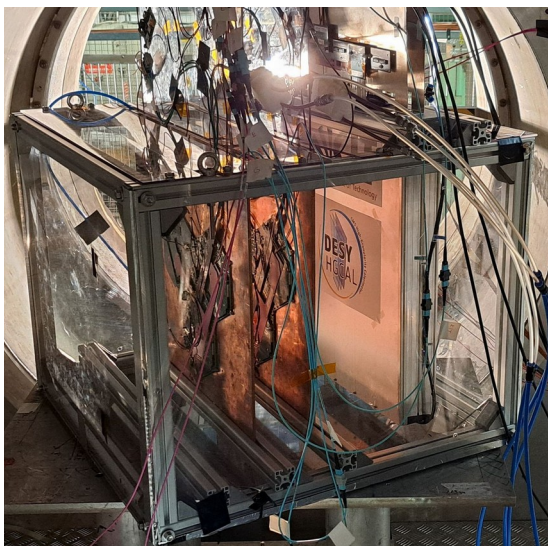
- Spring 2024: Validation of the full readout chain, getting ready for beam tests
- No ECON-D → direct readout of HGCROC frames to DAQ PC
- No DTH prototype at KIT → 1 x 10G ethernet from Serenity to DAQ PC



First Beam Test: July/August this year

- Beam test at SPS H2
- 3T superconducting magnet
- 120 – 200 GeV electrons and muons
- *Separate* readout systems for silicon sensors and tile modules
- Two layers of 3 silicon sensors
  - Serenity-Z1.2 with VU7P
  - DTH-p1-v2 → DAQ PC
- Two tile modules
  - Serenity-Z1.1 with KU15P
  - DAQ PC via 10G ethernet





Highlights from the July/August Beam Test

- Stable operation in 3T magnetic field
  - Tested 3 different field orientations
- Synchronous readout of tile modules on
  - the same motherboard
  - two different motherboards
- Readout of ECON-T data with tileboards
- All measurements with
  - HGCROC version 3a
  - ECON-T-p1

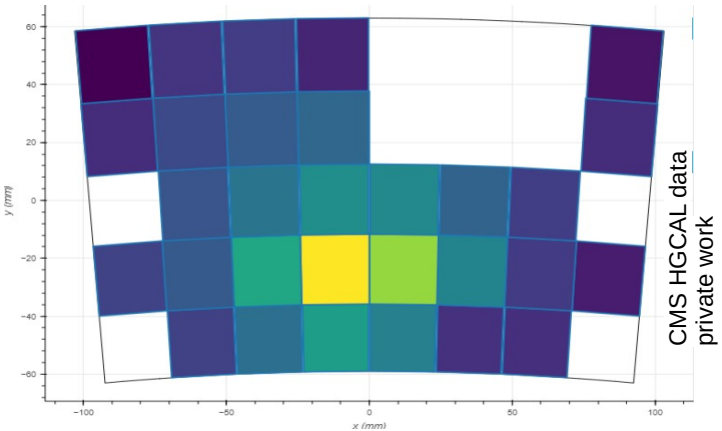
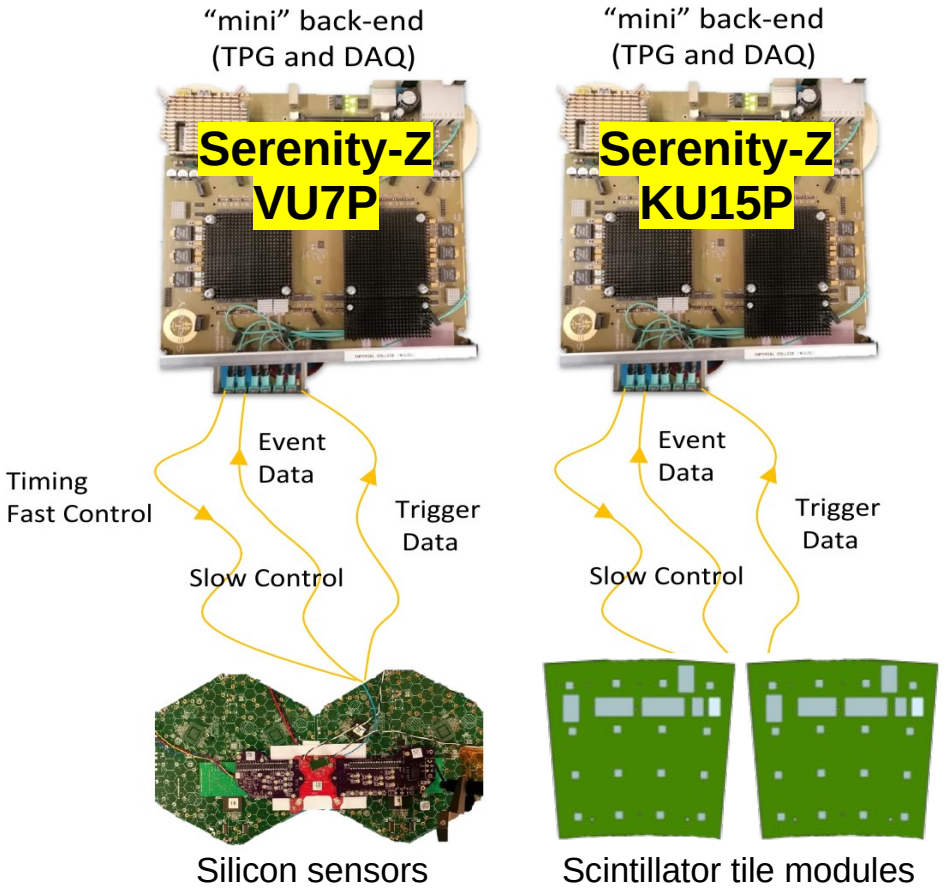


Figure: average ToT per sensor cell for EM shower (200 GeV electrons)

Now we have this...



[Figure by M. Voijnovic]

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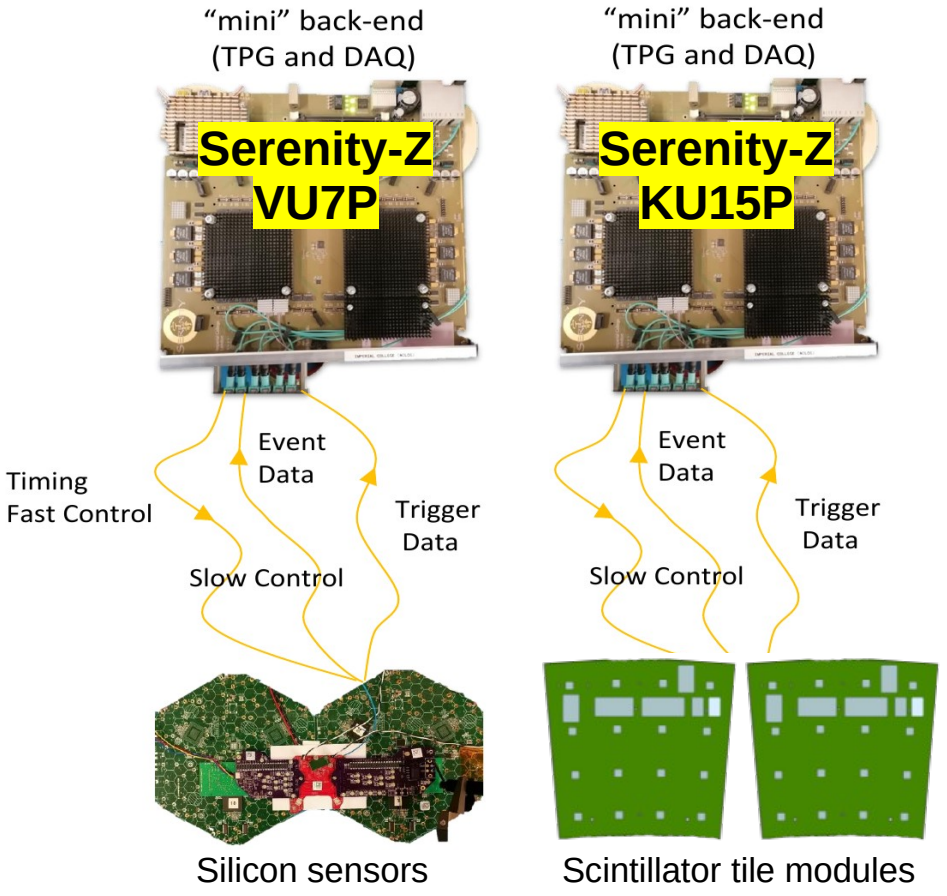
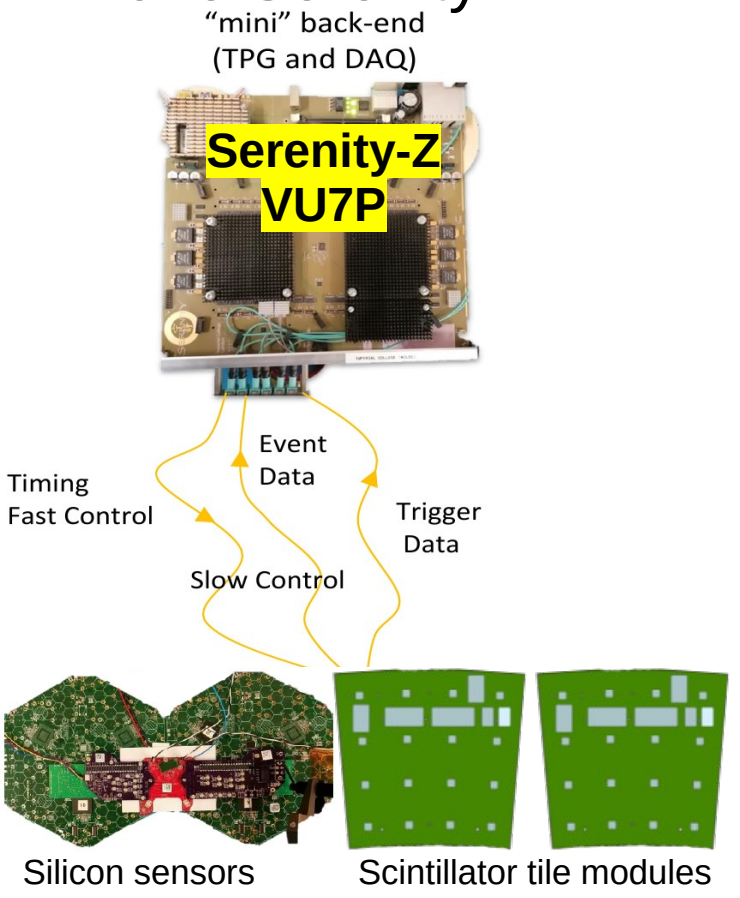


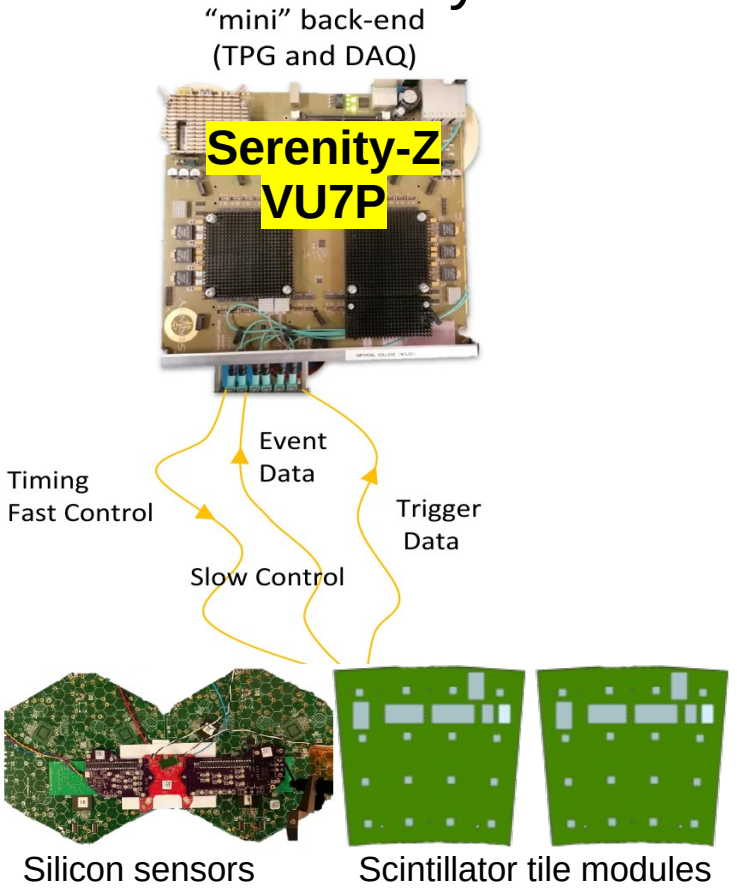
… but can we have both in one Serenity?



[Figure by M. Voijnovic]

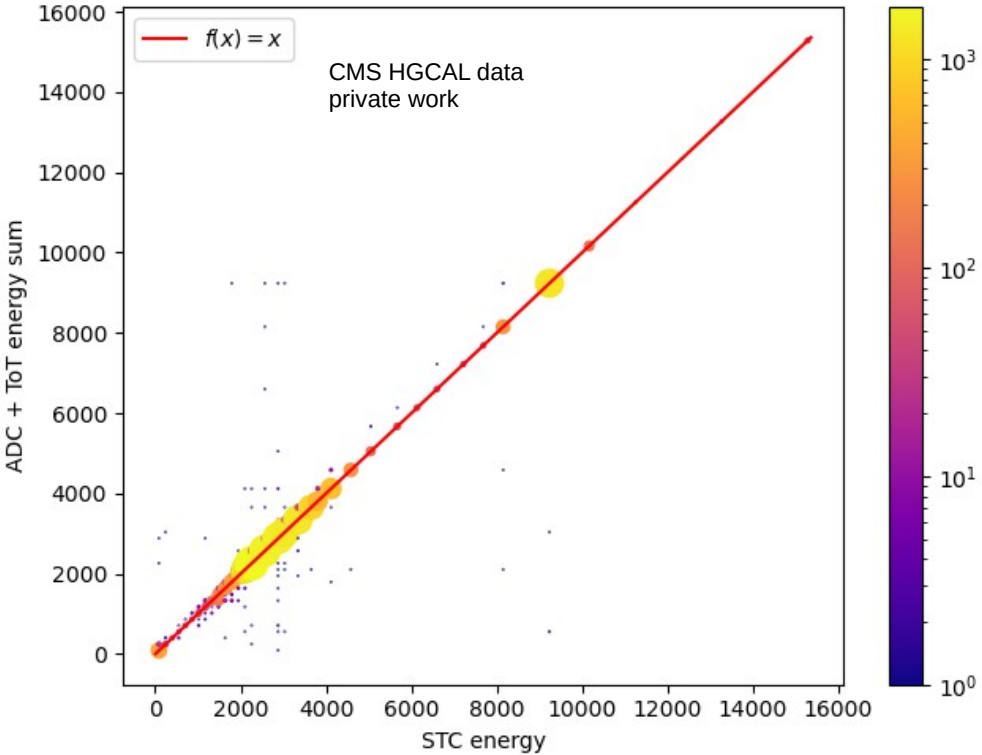
… but can we have both in one Serenity?

- New motherboard with ECON-D not yet available
- Common beam test firmware expects ECON-D packets
- Only trigger readout possible for now
- Need to understand DAQ/trigger correlation first



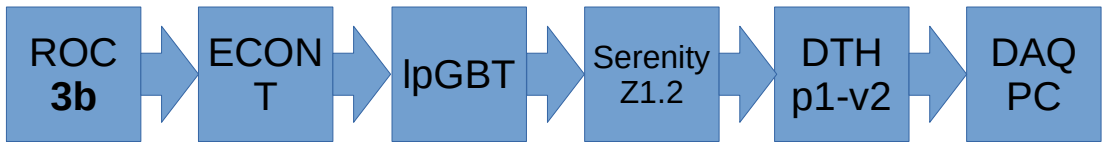
September Beam Test: DAQ/trigger correlation

- First week: commissioning of new tile modules using our Serenity-Z1.1 setup
  - Two modules with HGCROC v3b
  - Determine values for thresholds and calibration parameters (ADC, ToA, ToT)
  - Extensive datasets with muons and EM showers
- Understanding of DAQ and trigger correlation
  - **Figure:** energy in a super trigger cell vs. Sum of ADC and ToT of DAQ channels

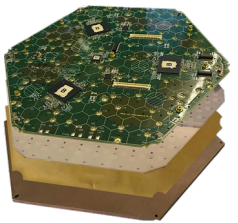


September beam test: unified readout

- Second week: connect tile modules *and* silicon modules to Serenity-Z1.2 (VU7P)
- Full readout chain for both sensor types:



- **Simultaneous** readout of trigger data for silicon sensors and scintillator tileboards
- No DAQ readout for tileboards (no ECON-D → different data format)



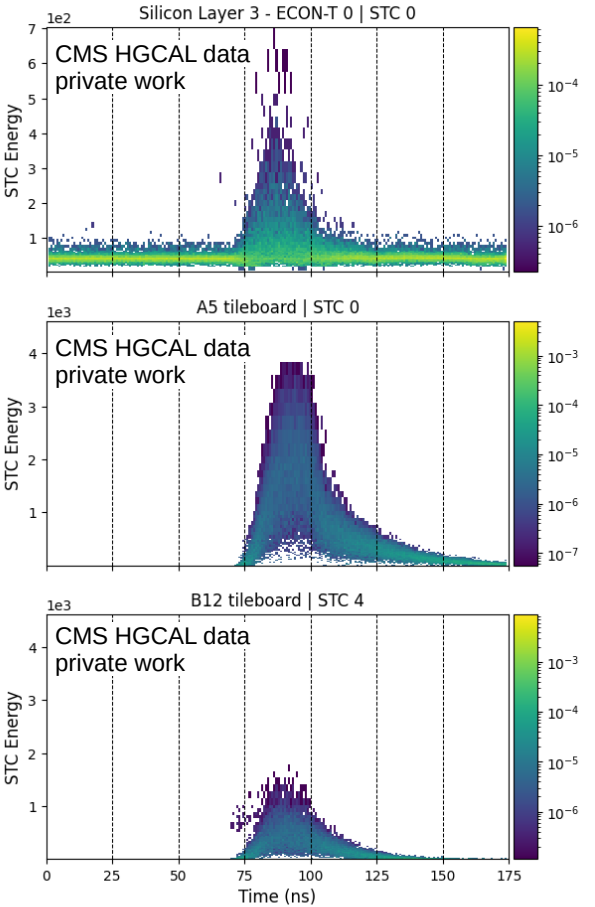


Figure: Time response to EM showers of super trigger cells from 3 different layers

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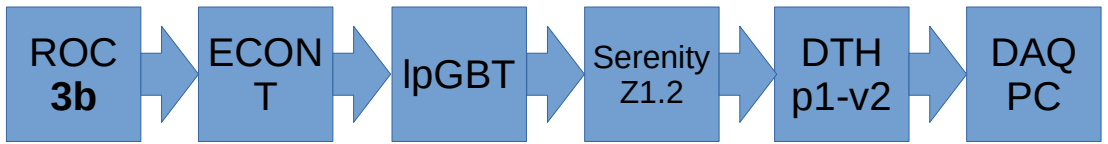

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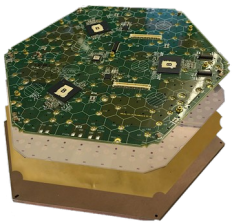
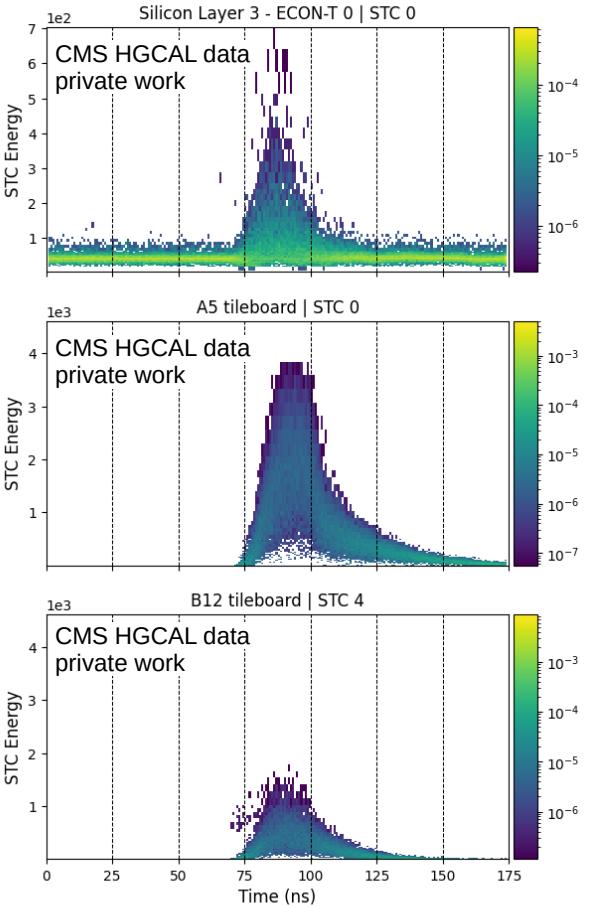
Info on HGCAL DAQ Firmware and some more beam test results:

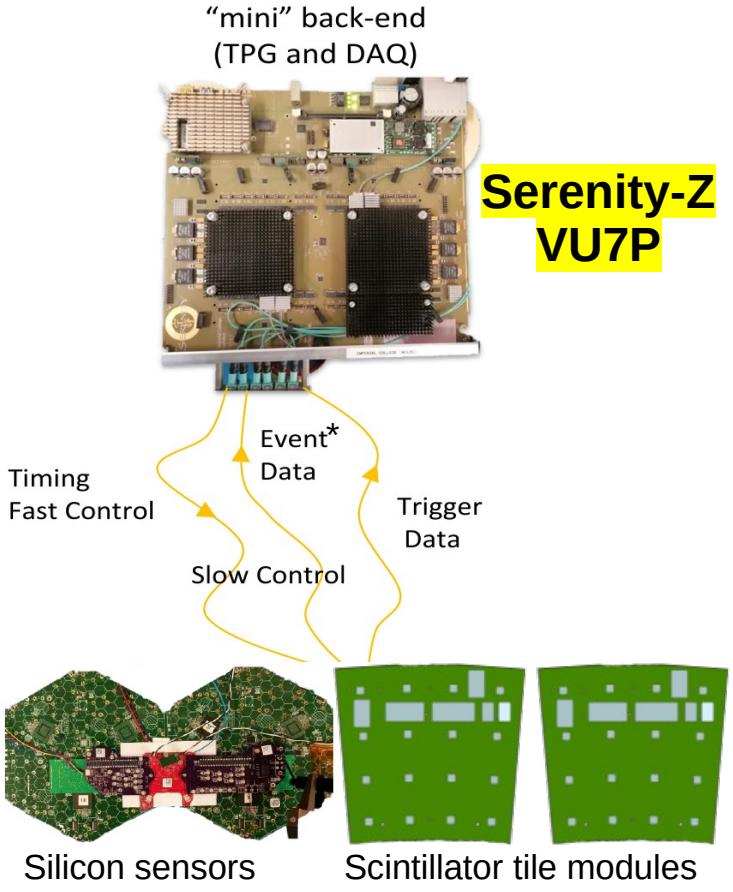
TWEPP 2024

[Poster] M. Rosado: Back-end DAQ system prototype testing and integration on a full detector test system for the CMS HGCAL detector





Now we have this...



* event data soon also for tileboards

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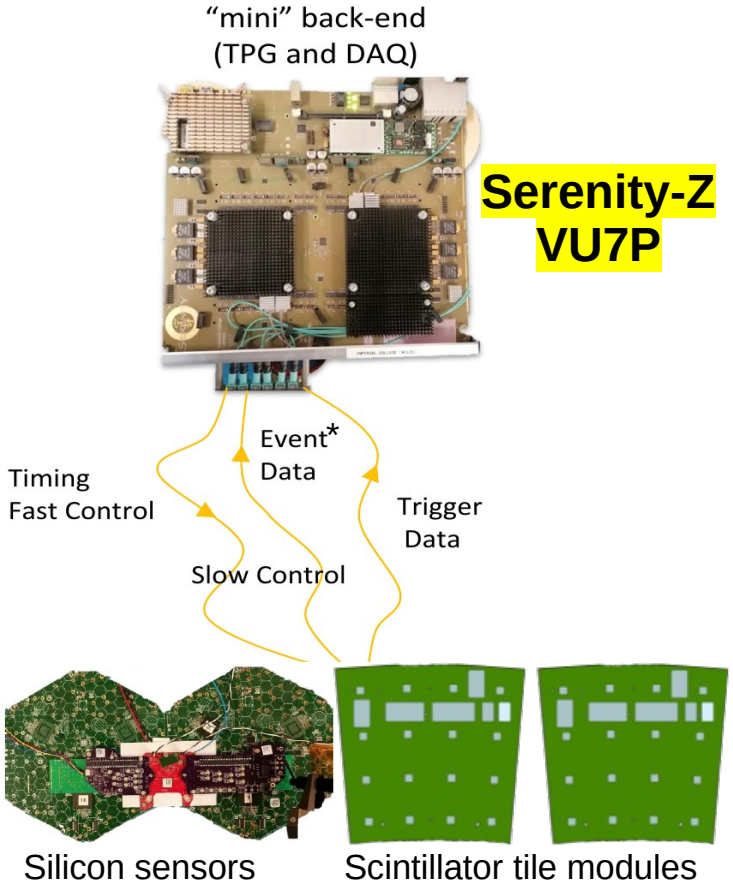
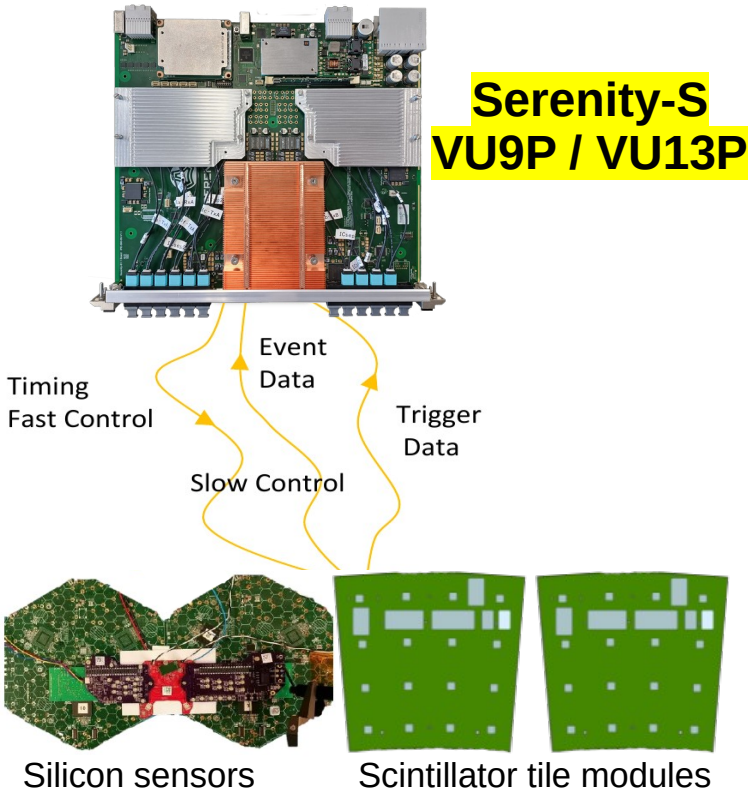


… but can we have that with Serenity-S?

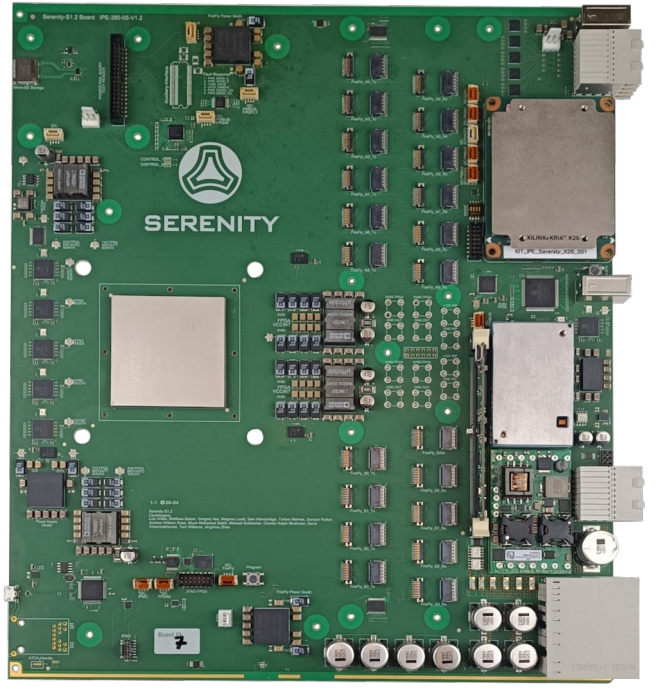


* event data soon also for tileboards

But what about Serenity-S?

A lot happend since last year’s TWEPP...

- 12 boards assambled so far
  - 6x Serenity-S1.1 → initial run with "teething issues"
  - 6x Serenity-S1.2 → fixed FireFly footprint 🥳
- Integration in firm-/software frameworks almost done
- Commissioning ongoing but cards are close to becomming usable by detector groups
- Next step: pre-series with 50 Serenity-S1.3 boards
  - PCB optimisations targeting the manifacturing process



TWEPP 2023 [Talk] T. Mehner: Lessons from integrating CMS Phase-2 back-end electronics and first results from Serenity-S1, a production optimised ATCA blade

Integration of HGCAL FE + Serenity-S

Summer 2024: Efforts started at KIT to bring HGCAL to Serenity-S

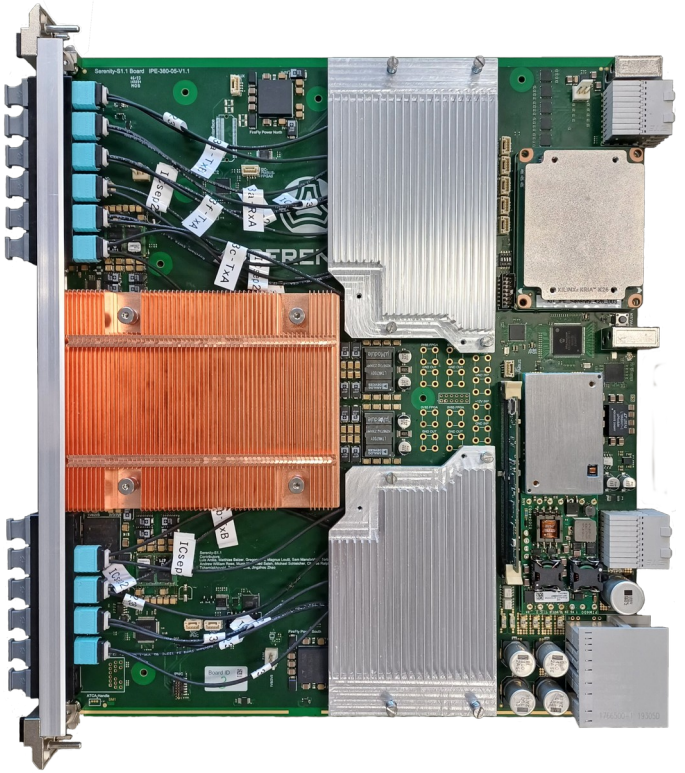
- Beam Test Firmware successfully ported from Serenity-Z1.2 *VU7P* to Serenity-S1.2 *VU9P*

Front-end Tests

- Successfull IC and EC communication with the SiPM-on-tile front-end

Back-end Tests

- No DTH prototype at KIT → Test still pending



Conclusions and Summary

- HGCAL SiPM-on-Tile readout chain validated with Serenity-Z
  - Iterative integration of tile modules with Serenity, using custom adapter hardware
  - Currently using pre-series motherboard
- Successful beam test of SiPM-on-tile system using Serenity-Z
  - Stable operation in 3T magnetic field
  - Readout of DAQ and trigger data from HGCROC versions 3a and 3b
- *Simultaneous* readout of scintillator tileboards and silicon sensors using Serenity-Z
  - Currently only trigger readout possible
  - Next step: production version motherboard with ECON-D
- Commissioning of Serenity-S ongoing, first tests with HGCAL front-end modules

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THE BACKEND BOYS

„I want it DAQ way“

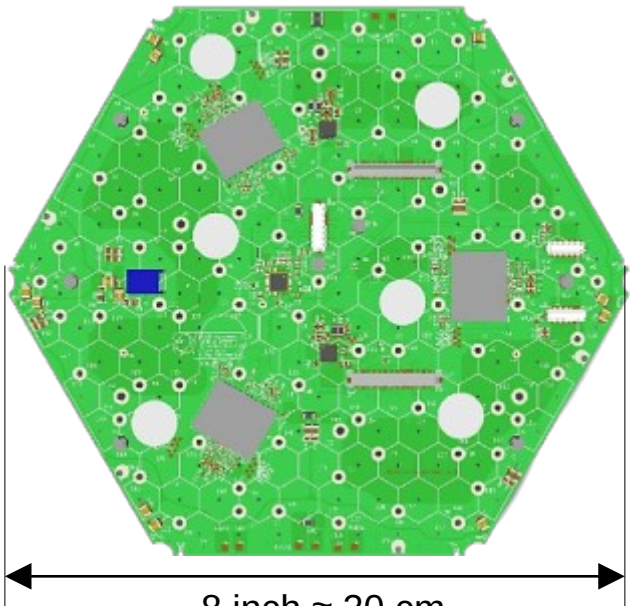

WANTED
REWARD $350

Backup

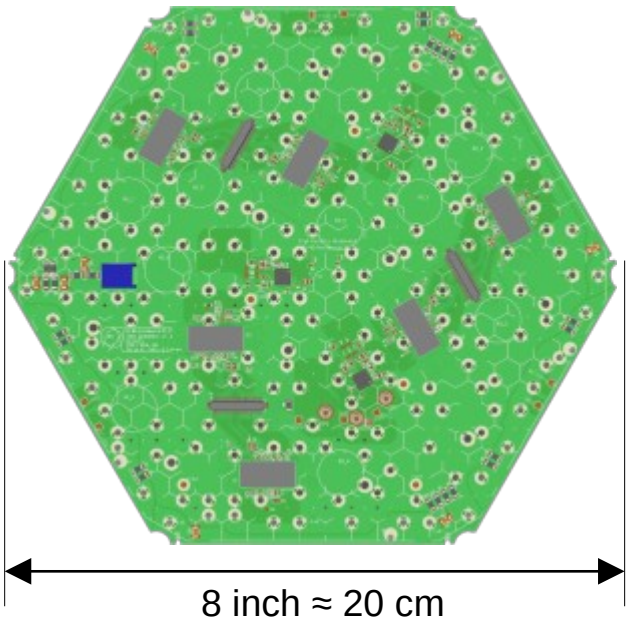
Silicon Modules – Hexaboards

- For areas with high radiation
- 620 m² of active area
- Front-end ASICS: HGCROC, LDO and RAFAEL
- Low density and high density version
- Wire bonded to Si sensor (8 inch wafer)
- Readout electronics: engines (VL+, ECONs) and wagons (passive)
- 30k boards, 6M channels

Low Density Hexaboards
3 x HGCROC
192 Si cells (1.1 cm²)

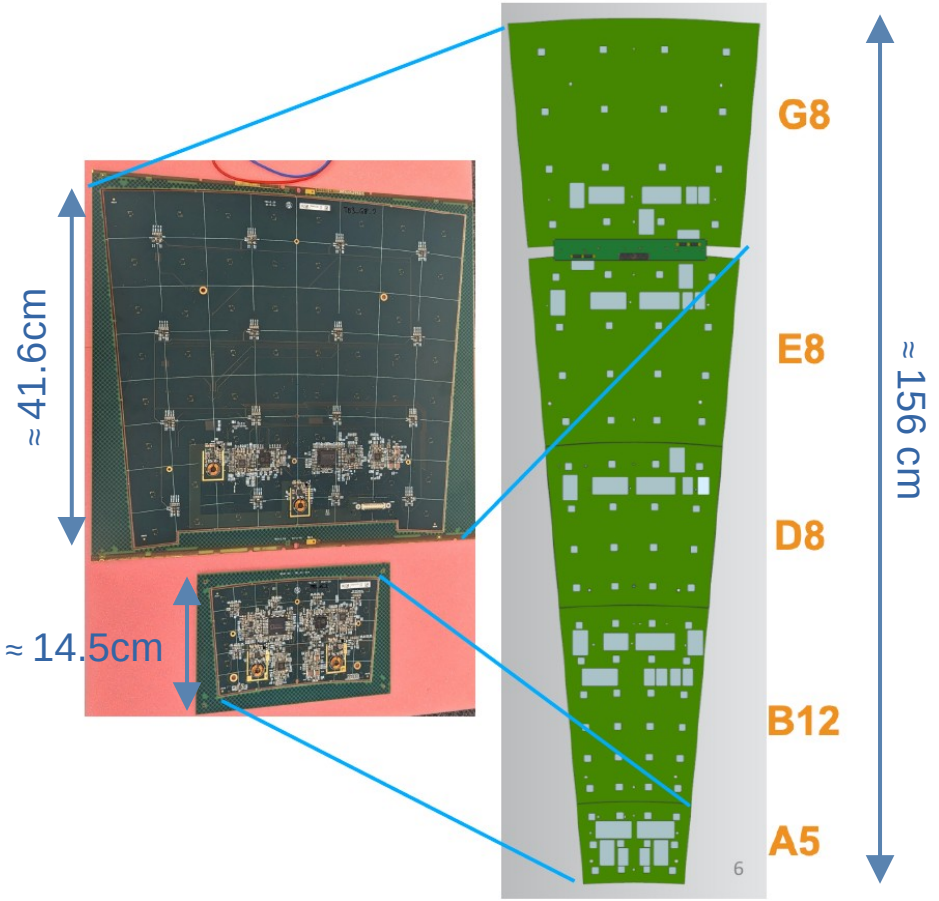


High Density Hexaboards
6 x HGCROC
432 Si cells (0.5 cm²)



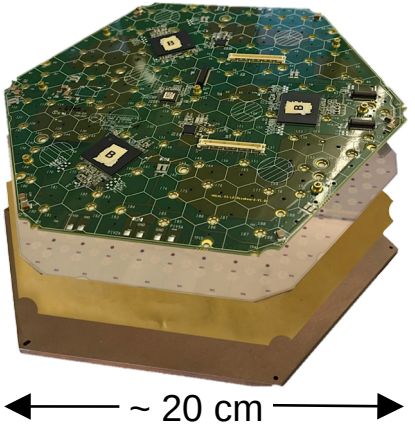
Tile Modules – Tileboards

- For areas with lower radiation
- 400 m² active area: scintillator + SiPM
- Front-end ASICS: 1-2 x HGCROC, GBT-SCA, 1-2 x ALDO
- Scintillator tiles placed directly on PCB, 4-30 cm² per tile
- LED system for calibration
- High density version with smaller tiles under consideration
- Readout electronics: Motherboard (VL+, ECONs, RAFAEL) and wingboards (passive)
- 4k boards, 240k channels



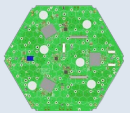
HGCAL's sensors in a nutshell

- Scintillator tile modules:
  - Plastic scintillator tiles read out by SiPMs
  - For lower-radiation environment
  - Sensor cell size 4 cm² … 30 cm²
  - 370 m² active area, 4k modules, 240k channels
- Silicon modules:
  - Silicon sensors wire-bonded to readout PCB („hexaboard“)
  - For high-radiation regions of HGCAL
  - Sensor cell size 0.5 cm² … 1 cm²
  - 620 m² active area, 26k modules, 6M readout channels



TWEPP 2024 [Poster] P. Antoszczuk: On-detector power distribution for CMS-HGCAL: a busbar-based approach

Silicon / SiPM-on-Tile FE Differences

	LD Hexaboard 	HD Hexaboard	Tileboard / Motherboard / WB 
HGCROC	3 per LD Hexaboard	6 per HD Hexaboard	1 for most Geometries / 2 for B12 Tileboard
GBT-SCA	N/A	N/A	1 GBT-SCA per Tileboard
ECONs	ECON Mezzanine on the Hexaboard		2 ECON-T + 1 ECON-D on the Motherboard
RAFAEL	1 per Hexaboard		1 per Motherboard
lpGBT	3 per LD Engine	6 per HD Engine	2 per Motherboard (DAQ + Trigger)
VTRx+	1 per LD Engine	2 per HD Engine	1 per Motherboard
linPol12	Engine		Motherboard
LDO	Hexaboard and Engine		1 on Motherboard, 2 per Tileboard
bPol12	DCDC mezzanine on the Hexaboard		1 per Motherboard, 2 per Tileboard
ALDO	N/A	N/A	2 per Tileboard

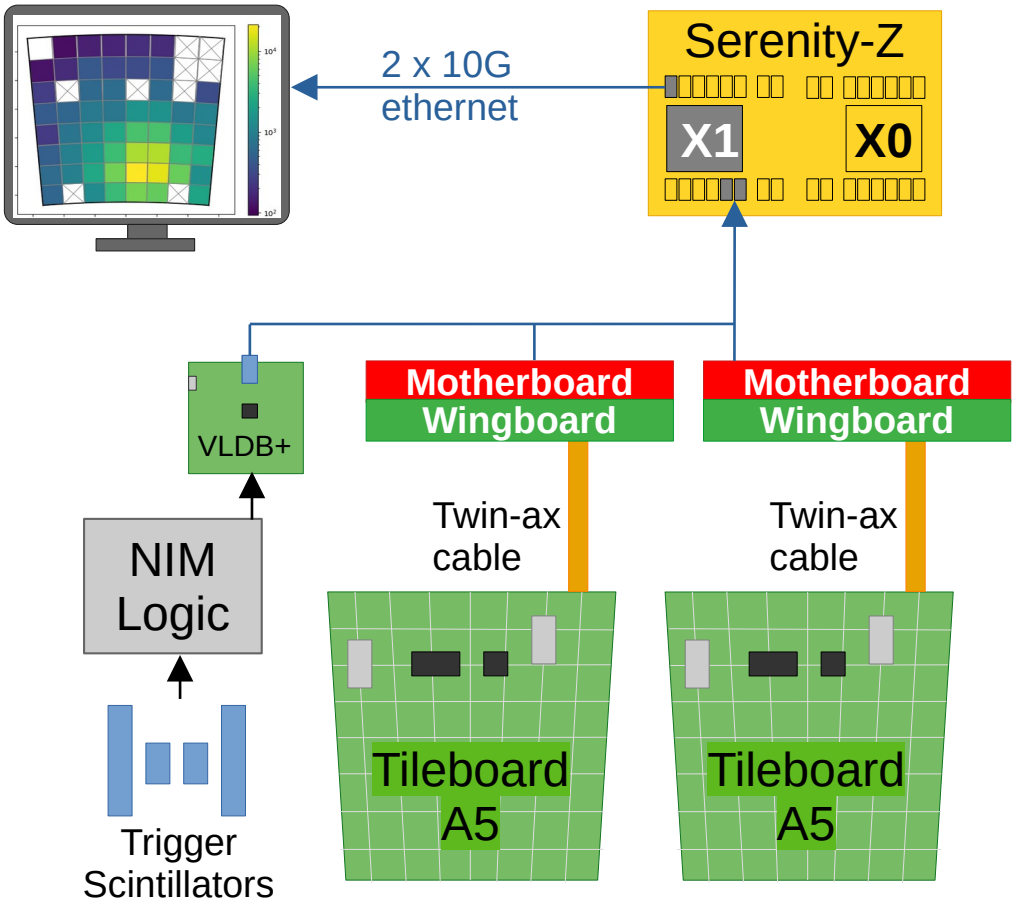
Step-by-step to Tileboard readout: “What can we test when?“

	Step 1: Serenity → VLDB+ and SCA on VLDB	Step 2: Serenity → VLDB+ and Tileboard (via adapter)	Step 3: Serenity → MB → Wingboard → Tileboard
Slow control tests	☑ lpGBT + SCA only	☑ lpGBT, SCA, HGCROC, ALDO	☑ 2-3x lpGBT, ECON-T, 1-5x SCA, 1-5x HGCROC
Fast commands	NO	☑ YES, directly to HGCROC	☑ YES, via RAFAEL
40MHz clock jitter measurement	NO	☑ YES, jitter of tileboard only	☑ YES, clock jitter of full readout chain
Bit error rate measurement	NO	☑ YES, tileboard only	☑ YES, full readout chain → System validation
Trigger readout	NO	☑ Raw trigger stream from HGCROC	☑ YES
DAQ readout	NO	☑ Raw data stream from HGCROC	☑ Raw data stream from HGCROC
Multiple Tileboards	NO	NO	☑ YES

Setup for July/August beam test

Pre-series motherboards: no ECON-D

- Can’t use miniDAQ firmware block from common beam test FW
- Direct streaming of ROC-DAQ packets to the DAQ PC
- 10G ethernet links



Serenity-S1 FPGA Card

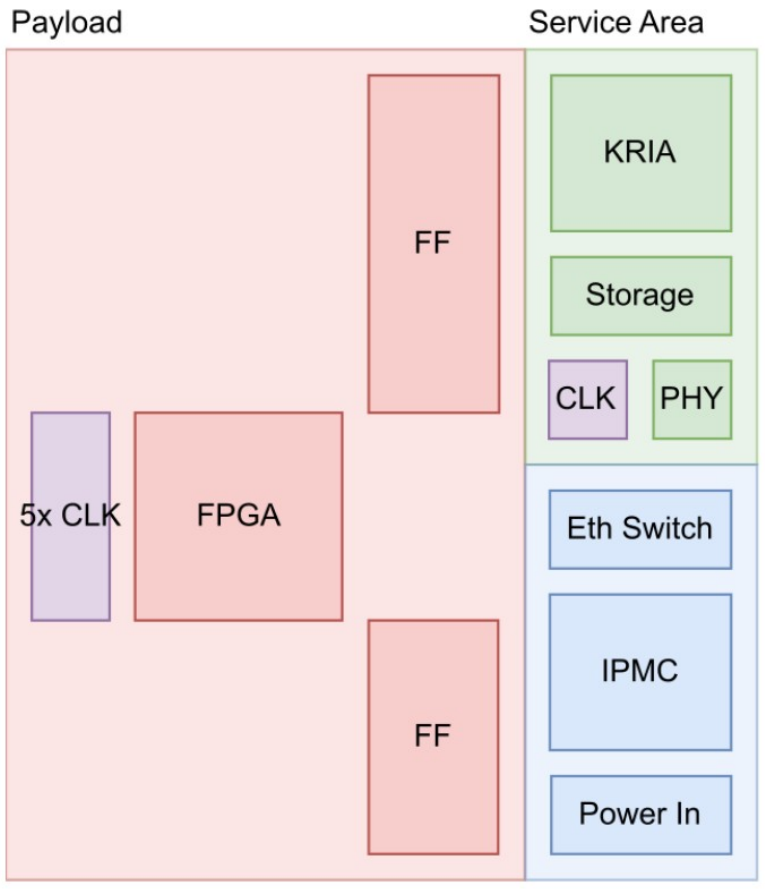


Figure by Torben Mehner

- Board Infrastructure
  - Xilinx KRIA SoM
  - Clock, power, PHY
  - SD, SSD
- ATCA Infrastructure
  - Backplane connectors
  - IPMC (OpenIPMC DIMM module)
  - Power input
  - Ethernet switch
- Payload
  - FireFly optical transceivers
  - VU13P FPGA
  - Clocks