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HGCAL SiPM-on-Tile Full-Stack Integration with the Serenity-S Phase-2 DAQ Hardware

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For the upcoming high-luminosity LHC, the endcap calorimeters of the CMS experiment will be replaced by the high-granularity calorimeter (HGCAL), a sampling calorimeter using both silicon and scintillator as active materials in different regions depending on the radiation dose. This contribution describes the integration details of the scintillator-based front-end into the DAQ readout chain of HGCAL. For the first time, both sensor technologies are integrated into a single system utilizing the Serenity-S FPGA cards. Initial results from a beam test at CERN showcase both detector technologies of HGCAL, validating the vertical integration stack of the latest available front-end prototype hardware.

Summary (500 words)

The CMS high-granularity calorimeter is a sampling calorimeter that uses two different sensor technologies. Hexagonal silicon sensors are used in areas exposed to high radiation and pile-up, and the outer parts of the calorimeter endcap are instrumented with plastic scintillator tiles read out with SiPMs. Each endcap will contain roughly 200 m² of active area instrumented with plastic scintillators and 300 m² of silicon sensors, with more than 3 million readout channels per endcap. The configuration, control, and readout of the HGCAL front-end is based on the Serenity FPGA boards.

In this contribution, we will present the vertical integration of scintillator modules with the latest available front-end prototype hardware. The scintillator region has functionalities that are not present in the silicon part of HGCAL, such as an LED calibration system. Moreover, the scintillator modules are significantly larger, requiring high-speed cables of up to 1 m in length. These unique features require detailed system-wide tests of the readout chain.

Previous efforts were based on the Serenity-Z board with a Xilinx KU15P FPGA and a “Com-Express” module for board control. Its successor, the Serenity-S, houses an FPGA from the Virtex Ultrascale+ family and a KRIA System-on-Module (SoM). Multiple Serenity prototypes have been assembled and are now becoming available for the first tests with detector hardware. We will show the first results of the scintillator tile modules read out with the Serenity-S platform assembled with a Xilinx VU13P FPGA.

Both the scintillator and silicon sections of HGCAL share a common readout scheme with the same set of front-end ASICs. However, the configuration and arrangement of these components vary between scintillator and silicon and between the “high-density”and “low-density”variants of both sensor types. Both the FPGA firmware and the online software running on the data acquisition Serenity-S boards need to support this variety of hardware configuration since both detector types are read out by the same board. To reduce maintenance efforts, it is foreseen that a single firmware version is needed.

A common DAQ firmware and software will be tested in a beam test campaign at SPS at CERN in summer 2024. The test setup utilizes multiple sensors, including low-density and high-density silicon hexaboards and low-density scintillator tileboards, allowing both sensor types to co-exist for the first time. We will present the initial outcomes of these tests, along with the integration experiences of the latest available front-end prototype hardware.

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